A Low Voltage to High Voltage Level Shifter Circuit for MEMS Application

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Abstract— High voltage (>15V) drivers are integrated into the VLSI chip for MEMS application with the development of SOC technology. The pre-driver circuit, which generates the pull-up and pull-down signal, is mainly a voltage level shifter circuit. It converts the low voltage control signal to high voltage control signal. Conventional voltage level shifter circuit using high voltage NMOS and high voltage PMOS operates well on 0.8 um process. However, with the continuous process shrinking, conventional voltage level shifter circuit is not suitable for high voltage power supply due to the reduced breakdown voltage of the high voltage devices. Although stacked high voltage devices can be applied to solve this issue, the circuit will have DC leakage current and the internal high voltage swing problem.

This paper describes a new low voltage to high voltage converter circuit. By using all the low voltage devices, the DC leakage current and the high voltage swing node have been eliminated. This circuit is fabricated in 0.35 SOI process. Both simulation and test results validate its operations for controlling high voltage drivers.

I. Introduction

High voltage (>15V) drivers are integrated into the VLSI chip for MEMS application with the development of SOC technology. The high voltage drivers usually apply high voltage NMOS (HVNMOS) and high voltage PMOS (HVPMOS) as the pull-up and the pull-down device. The pre-driver circuit, which generates the pull-up and pull-down control signal, is mainly a voltage level shifter circuit. It generates the HVNMOS control signal and converts the low voltage control signal to high voltage HVPMOS control signal. Reliability, and the low power consumption, especially the low DC current are major concerns for a practical pre-driver circuit.

Previous research of the voltage shifter circuit [1] using high voltage NMOS and high voltage PMOS operates well on 0.8 um process. However, with the continuous process shrinking, breakdown voltage of those high voltage devices, especially the P device, also reduces. In order to maintain the high operation voltage, stacked devices can be used in the pre-driver [2][3]. The voltage shifter circuit using stacked HV devices, on the other hand, will experience DC leakage current and further increase the overall power consumption. At the same time, the internal nodes of the conventional voltage shift circuit have large voltage swing (changes from GND to the power supply). This large voltage swing will increase the complexity of the layout. It may even affect the reliability of the circuit due to the high electric field.

This paper describes a new low voltage to high voltage converter circuit without DC leakage current. It also reduces the voltage swing of the internal nodes.

II. HV Device Structure and the Driver Circuit

The high voltage devices can be manufactured using standard digital commercial process using special layout techniques [4]. Fig.1 shows the cross section of a high voltage device. The lightly doped N-well region (N-) creates a drift path. The breakdown voltage will be increased due to the reduced concentration level near the PN junction as shown in the follows [2]:

$$BV \cong \frac{\varepsilon_{si}(N_A + N_D)}{2qN_A N_D} E_{Max}^2 \quad (1)$$

Where ε_{si} is the dielectric permittivity of silicon, N_A is the doping concentration of the acceptors of P-type material, N_D is the doping concentration of the donors in the N-type material, q is the charge of an electron (1.602E-19 coulombs), and E_{Max} is the critical electric field for silicon.

At the same time, the field oxide is applied in the HV device to protect the gate from the high electrical field.

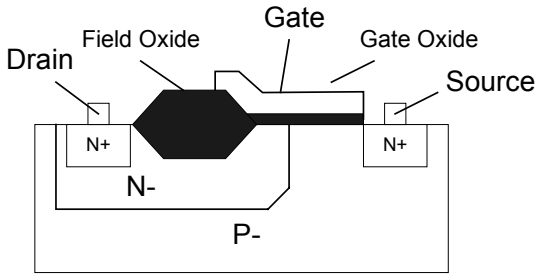

Fig.1. Cross section of a high voltage NMOS.

Fig.2 shows a high voltage driver circuit using a HVNMOS and a HVPMOS. The drain to source breakdown voltage (V_{ds}) is very high for these devices while the gate to source breakdown voltage (V_{gs}) is much lower. For the 0.35um process used in this research project, the V_{gs} breakdown voltage of HVNMOS is about 5V and the V_{ds} breakdown voltage is higher than 15V. Low voltage signal can be used to drive the HVNMOS directly. For the HVPMOS, the V_{sg} breakdown voltage of HVNMOS is also about 5V while the V_{sd} breakdown voltage is about 10V. In this project, the control signal for the HVNMOS varies from 0 and 3V. The control signal for HVPMOS should close to power supply (HVCC) to avoid high V_{sg} voltage. The control signal is design to vary from

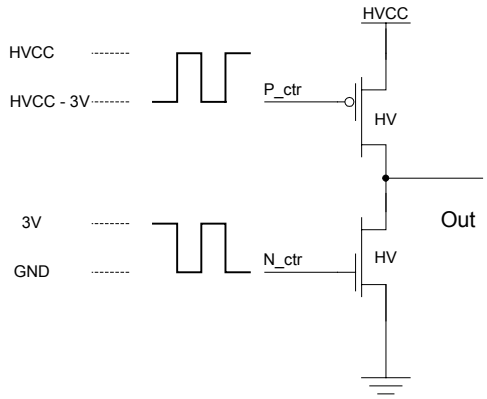

Fig.2. A high voltage driver circuit and its control signals.

HVCC-3V to HVCC. Thus, special pre-driver circuit must be used to generate the control signals.

III. A Conventional Voltage Level Shifter Circuit

A conventional voltage shifter circuit is shown in Fig.3. It applies two HVNMOS and two HVPMOS devices. Two bias voltages are used to limit the voltage swing of the Out_l1 and Out_h1 nodes. When the input is high, M2 turns on and pulls down the Out_l1 node to GND. The generated large V_{gs} of M4 will turn on the M4 and pull the node MID1 to GND. M6 and Bias_h will keep Out_h1 lower than biash+$|V_{thp}|$ (If Out_h1 is higher than biash+$|V_{thp}|$, M6 will turn on and pull the node Out_h1 down to biash+$|V_{thp}|$). The cross-coupled transistor M7 and M8 operate like a current sense circuit [5]. It will further pull down the voltage of out_h1 node to about Bias_h. On the contrary, when the input is low, the Out_h1 output will be high and the Out_l1 will be low.

The maximum voltages across the drain and source of the HVPMOS and the HVNMOS in Fig.3 are close to HVCC. If HVCC is higher than the breakdown voltage, normal HV devices cannot be used. Fig.4 shows the alternative configuration of the HV device by stacking them together. The voltage across the source and drain of each transistor is about one third V_{ds} of the entire stacked device. Replacing the normal high voltage devices in Fig.3 by the stacked devices, the maximum operation voltage HVCC can be higher than the breakdown voltage of the signal HV device.

The stacked HV device, on the other hand, will have DC leakage current from gate to drain through the resistors. Depended on the circuit configuration, the leakage current varies from 10uA to 500uA. At the same time, the node MID1 and MID0 will experience high voltage swing form GND to HVCC as shown in Fig.5. These high voltage swing node will increase the complexity of the layout. It may even affect the reliability of the circuit due to the high electric field.

IV. A Non High Voltage Swing LVHV circuit

A proposed low to high voltage shifter circuit is shown in Fig.6. Five bias voltages are applied in this circuit. All the transistors used in this level shifter circuit are normal low

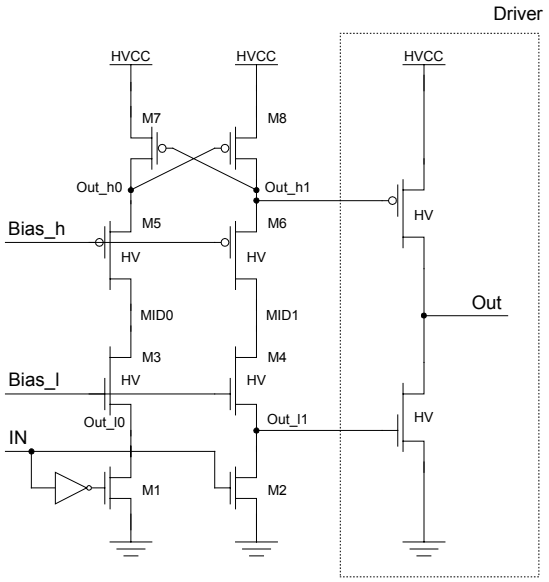

Fig.3. A conventional voltage level shifter circuit.

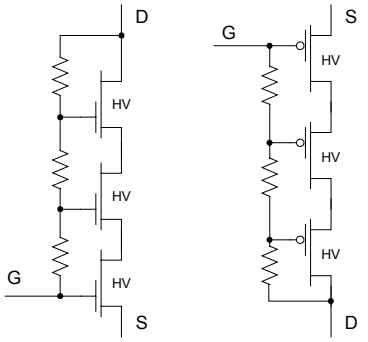

Fig.4. Stacked HVNMOS and Stacked HVPMOS.

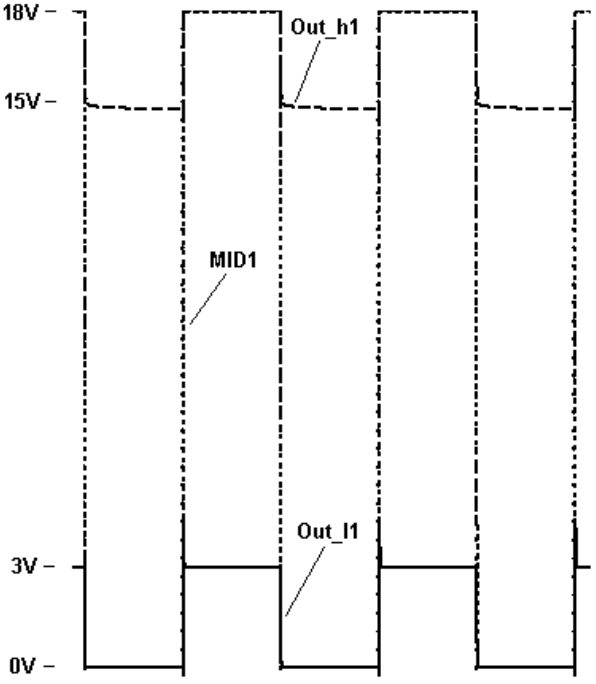

Fig.5. Output and internal nodes of the shifter circuit.

voltage devices. The operation of the new level shifter circuit is similar to the original circuit expect the drain connected PMOS and NMOS pairs. When input is high, transistor MN0B starts to conduct and voltage of node N1B will pull down to GND. Since V_{gs} of MN1B is larger than V_{th}, MN1B conducts and pulls node N2B to GND. If voltage of node N3B is larger than Vbias5 + $|V_{thp}|$, MP1B will conduct until the Voltage of node N3B is less than Vbias5 + $|V_{thp}|$. Similar to the operation of MN1B and MP1B pair, MN2B and MP2B, MN3B and MP3B, MN4B and MP4B, MN5B and MP5B transistor pairs will pull down the voltage of the node Out_h1 to less than Vbias1 + $|V_{thp}|$. The cross-coupled PMOS pair MP0A & MP0B will further stabilized the voltage of the Out_h0 and Out_h1 to about HVCC and Vbias1. Similarly, when the input is low, the Out_h1 will be HVCC and out _l1 will be around Vbias5.

The maximum V_{ds} across the transistor in the level shifter circuit is about the voltage difference between two bias voltages. In this project, 18V is chose for HVCC and 3V, 6V, 9V and 12V are picked for bias1, bias2, bias3, bias4 and bias5 respectively. Thus, the maximum V_{ds} of all the transistors is about 3V. At the same time, the maximum voltage swing for a particular node is reducing from 18V to about 6V.

V. Simulation Result and Circuit Fabrication

Simulation result of the proposed voltage level shifter circuit is shown in Fig.9. The low voltage input signal generates both the low voltage pull-down and the high voltage pull-up control signals through the voltage level shifter circuit. The pull-up and pull-down signals further generates the high voltage swing output signals through the final high voltage driver circuit.

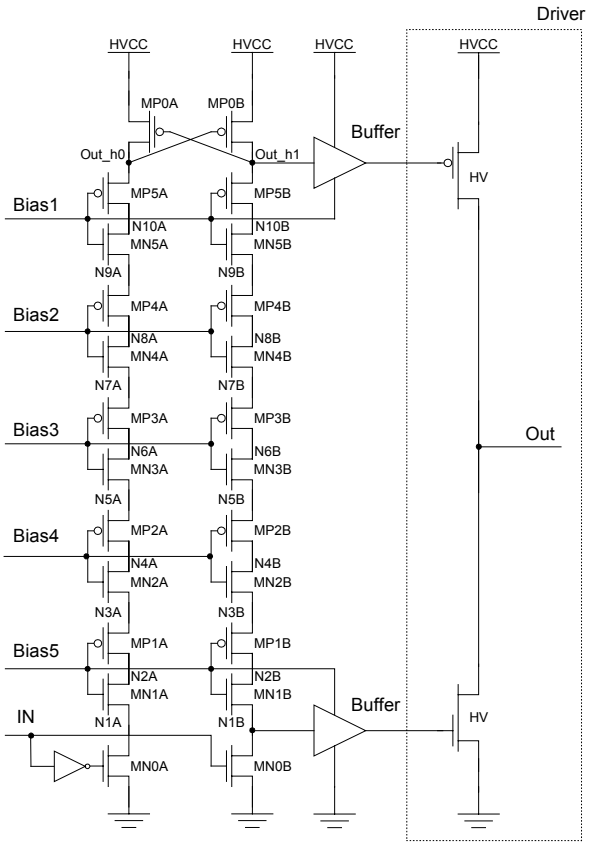

Fig.6. A proposed voltage level shift circuit.

The speed of the level shift circuit is limited by time need to charge and discharge the internal nodes such as M1A/M1B, M2A/M2B, etc. Simulation shows this circuit is able to operate under 1M Hz frequency.

Since all the devices used in the voltage shifter circuit are low voltage devices, the $|V_{ds}|$ and $|V_{gs}|$ of all the devices must below the breakdown voltage (both are 5V for this project). Fig.7 shows the simulation results of the $|V_{ds}|$ and $|V_{gs}|$ for all devices. The maximum $|V_{ds}|$ is about 3.5V while the maximum $|V_{gs}|$ is about 4.5V. Both are lower than the breakdown voltage.

The circuit is implemented in 0.35um SOI process (Fig.8). The silicon test result matches our simulation result.

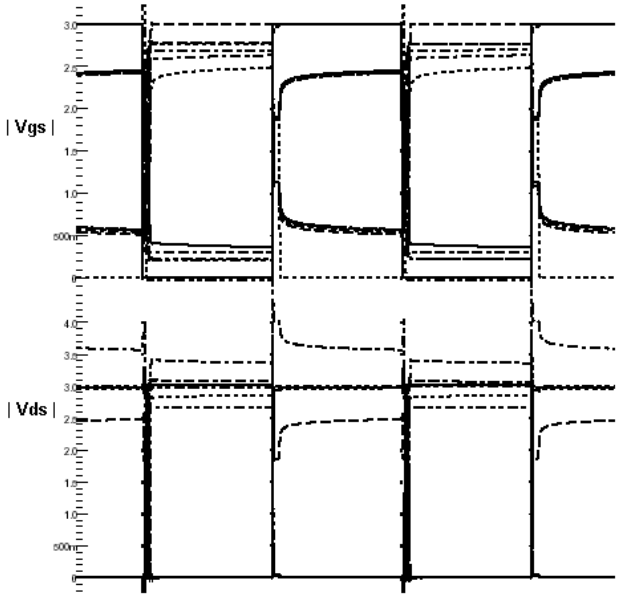

Fig.7. |Vgs| and |Vds| simulation results of all the devices.

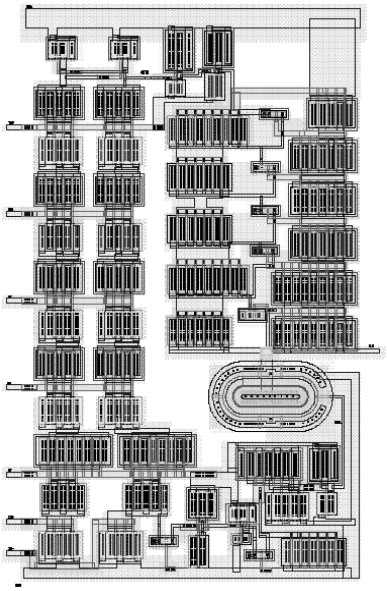

Fig.8. Circuit implementation on 0.35um SOI process.

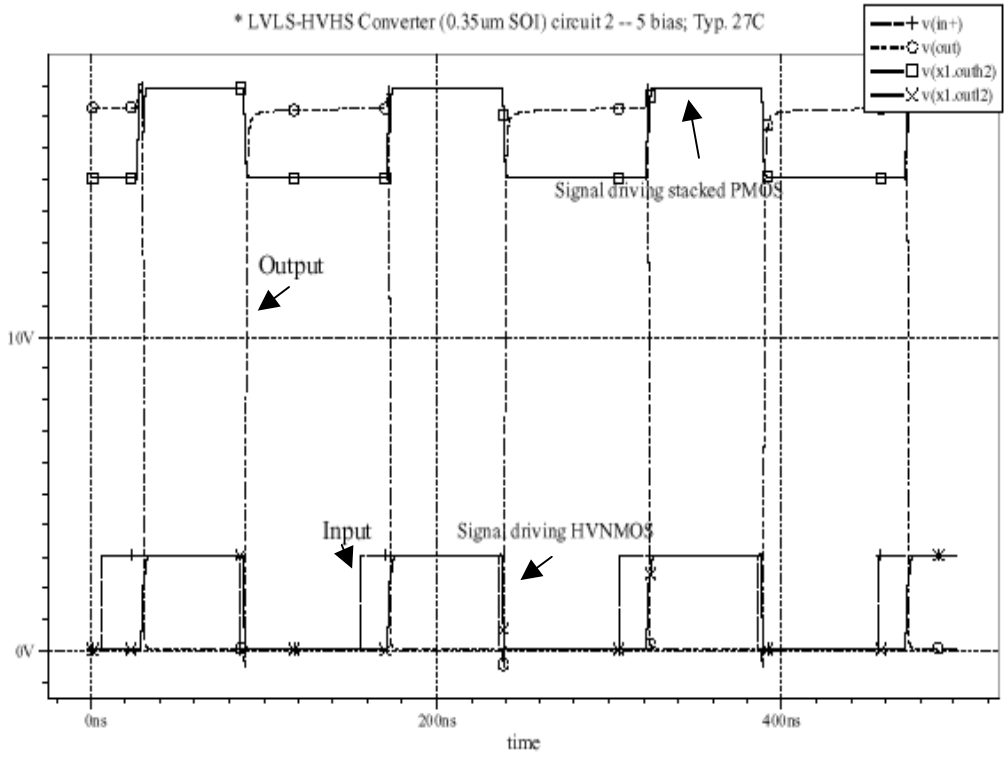

Fig.9. Simulation result of the proposed voltage level shifter circuit.

VI. CONCLUSION

A low voltage to high voltage level shifter circuit for MEMS application is designed using normal low voltage devices. It features zero DC current consumption while reduces internal voltage swing.

The simulation result indicates that the magnitude of the V_{gs} of all devices is less than 3.5V and the magnitude of the V_{ds} of all devices is less than 4.5V. The circuit is fabricated in 0.35 SOI process. The test result matches the simulation test.

VII. ACKNOWLEDGMENT

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