VLSI implementation of cross-coupled MOS resistor circuits

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Abstract – This paper presents the cross-coupled MOS resistor circuits. The circuits consist of two internal pairs of NMOS and PMOS transistors, and their critical width and length parameters regulate the drain current, transconductance, and output drain resistance. Consequently it determines the output resistance of the circuits. The cross-coupled MOS resistor circuits can be used in multiplication circuits and internal filter designs.

I. INTRODUCTION

With the advances in analog VLSI technology, IC design becomes more popular. In IC the resistors are one of its components. Resistors can be designed and fabricated in semiconductor processing. Resistors fabricated in IC's circuits as physical resistors occupy large chip areas. They have large sheet resistance and large parasitic capacitance, and that limits their applications for high frequency circuits [1], see equation (1). Resistors synthesis by using MOS transistors can have large resistance values, and they use smaller fraction of chip areas. The latter is more favorable for analog circuits.

$$f = \frac{1}{2\pi \cdot \tau} = \frac{1}{R^2}\left(\frac{R_{sq}}{2\pi W^2 C_j}\right) \qquad (1)$$

For MOS resistors, there are different circuit styles that have been invented by the researchers [2]-[6]. The CMOS floating resistor [7] and Voltage-controlled linear resistor by two MOS transistors [8] are only one of the few examples. In this paper, it presents the cross-couple MOS resistor circuits. The paper is divided into four sections. First, it reviews of the two current MOS resistor circuits. Second, it displays a resistor synthesis using drain-source output characteristics of NMOS and PMOS differential pairs. Third, it presents the cross-coupled MOS resistor circuits, which are the novelty of this paper. Finally, it shows an improved MOS resistor circuits with smaller leakage conductors and current controlled resistors.

II. REVIEW OF CURRENT MOS RESISTOR CIRCUITS

In this section, it reviews two current MOS resistor circuits. The first MOS resistor circuit is using the complementary NMOS and PMOS transistors [9], as shown in Fig. 1. Both PMOS M1 and M2 operate in triode region, and all the NMOS M3 to M6 operate in saturation region.

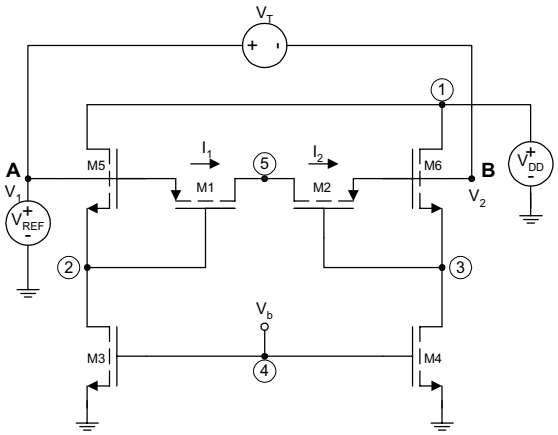

Fig. 1. Resistor synthesis using complementary NMOS and PMOS transistors

The equivalent resistance of the circuit between terminals A and B can be expressed as follow [2]:

$$R_{eq} = \frac{V_1 - V_2}{I} = \frac{2}{k(V_b - V_t)} \qquad (2)$$

Where k is the transconductance parameter and V_t is the threshold voltage. Figure 3 shows the SPICE simulation results of the circuit in Fig. 2 where V_b was varied from 3v to 7v.

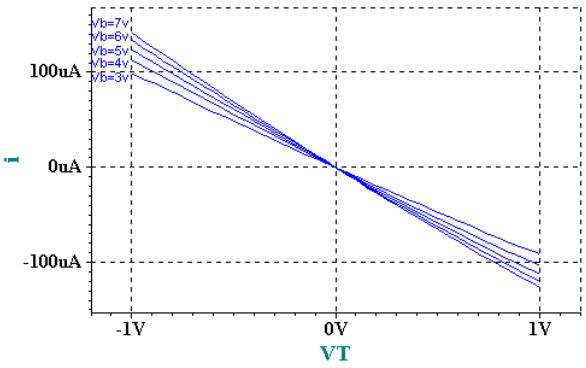

Fig. 2. I-V curves of the complementary NMOS and PMOS resistor circuit.

The second MOS resistor circuit [10] is shown in Fig. 3. It implements only NMOS transistors. This MOS resistor circuit is based on the two matched transistors M1 and M2 operating in the saturation region. In this circuit, I_{in} is equal to I_{out}. I_{in} and I_{out} are the same current flowing through the resistor between two terminals V_x and V_y. The drain current I_1 of M1 is also equal to the source current of M2 and vice versa for I_2.

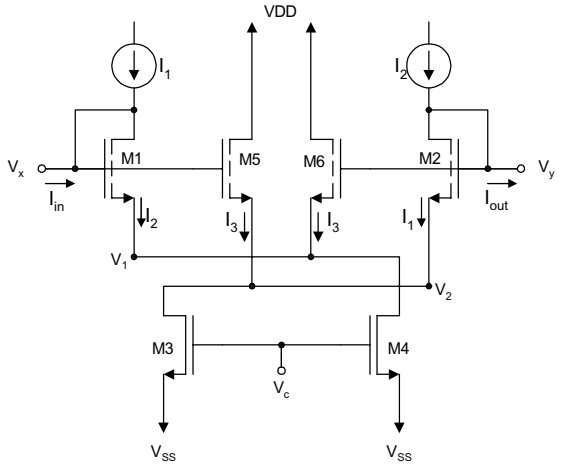

Fig. 3. Resistor synthesis using NMOS transistors only

The equivalent resistance of the circuit between two terminals V_x and V_y can be written as

$$R = \frac{1}{2k(V_c - V_{SS} - V_t)} \tag{3}$$

Figure 4 shows the SPICE simulation results for the circuit of Fig. 3 where V_c was varied from 0.8v to 1.15v.

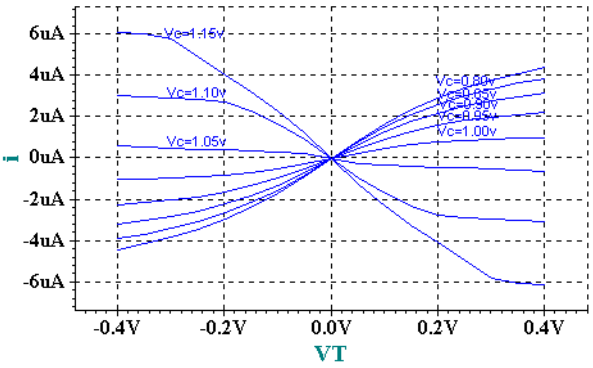

Fig. 4. I-V curves of the NMOS resistor circuit

The common fault of these circuits is that the maximum voltage applied to terminals A and B is very limited. In order to have a relatively large voltage swing, the MOS transistors must be biased with a large gate-source dc voltage, and this leads to large biasing currents and large power consumption. Moreover, the resistor values are relatively small.

In the following sections several concepts of resistors synthesis using the output characteristics of the MOS transistors are presented. Both smaller and larger resistances can be synthesized from these circuits. The power dissipations are also low.

III. SYNTHESIS OF RESISTOR USING DRAIN-SOURCE OUTPUT CHARACTERISTICS

The circuit in Fig. 5 is a differential pair with n-channel MOSFETs and a common-mode input signal. The resistance between nodes A and B can be used as a floating resistor, and its equivalent circuit diagram is shown in Fig. 6. This can be further reduced to the diagram shown in Fig. 7.

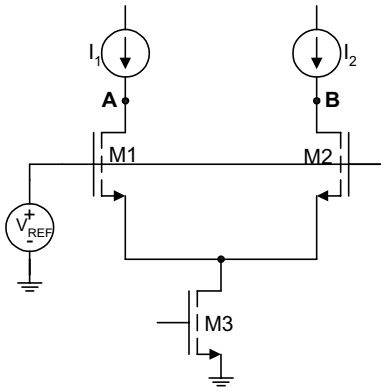

Fig. 5. An NMOS differential pair with a common-mode input signal

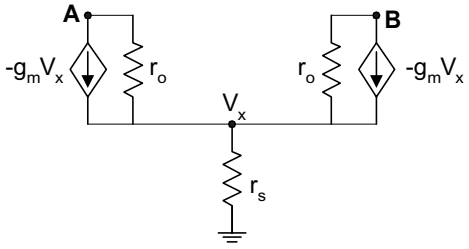

Fig. 6. The equivalent diagram of the circuit in Fig. 5

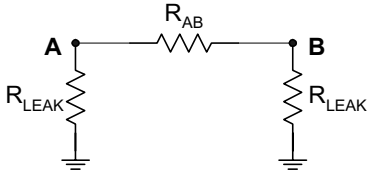

Fig. 7. The equivalent diagram of the circuit in Fig. 5

The resistance between nodes A and B is given as

$$R_{AB} = \frac{V_T}{I_T} = 2r_o \tag{4}$$

And its leakage resistances are expressed as follows:

$$R_{LEAK} = r_o(1+2r_s g_m)+2r_s \qquad (5)$$

Fig. 8 shows the SPICE simulation results for an NMOS differential pair where the channel length was 1.0um; W1 and W2 were changing from 5um to 25um.

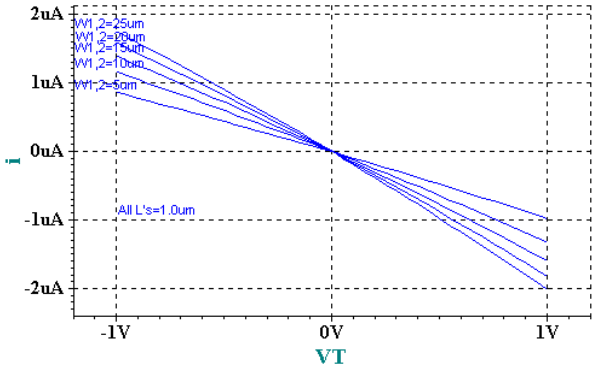

Fig. 8. I-V curves of an NMOS differential pair circuit.

One may notice that a complementary circuit with PMOS transistors (as shown in Fig. 9) can be also used for the resistor synthesis. Equations (4) and (5) of an NMOS differential pair circuit are also valid for a PMOS differential pair circuit. Its SPICE simulation results are shown in Fig 10 where W1,2=1.2um; L1 and L2 were changing from 7.5um to 17.5um.

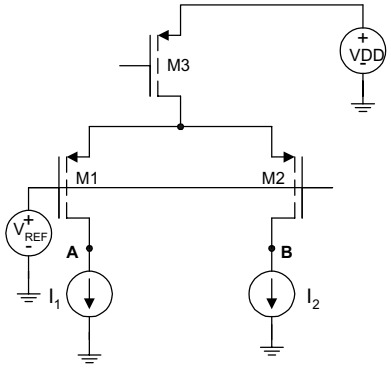

Fig. 9. The PMOS differential pair with a common-mode.

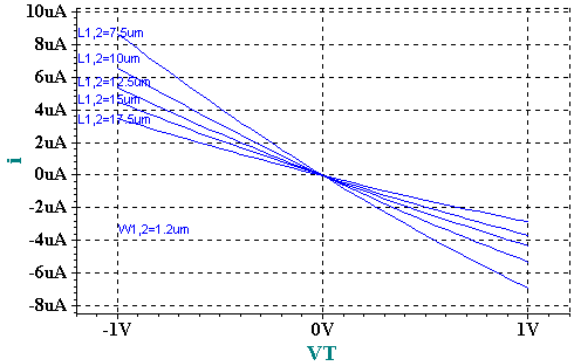

Fig. 10. I-V curves of a PMOS differential pair circuit.

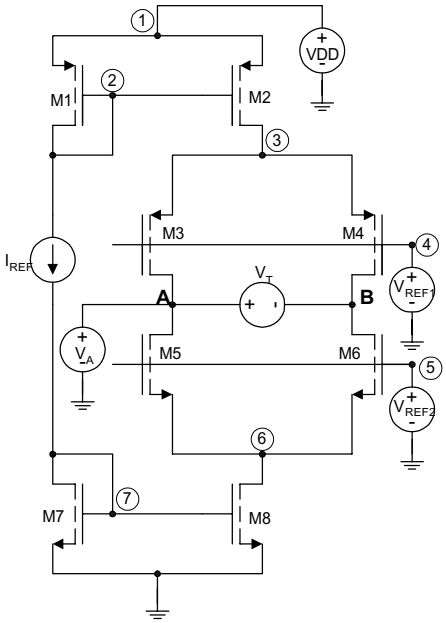

Fig. 11. A combination of NMOS and PMOS differential pairs

By analyzing the simulation results of the differential pairs in Fig. 5 and Fig. 9, one may observe that the existing non-linearity of both circuits can be partially compensated if they are combined together as shown in Fig. 11. This circuit also has a floating resistor between nodes A and B. Its SPICE simulation results are shown in Fig. 12 where L3 and L4 were changing from 7.5um to 17.5um; W3,W4=1.2um, L5,6=1um, W5,6=10um.

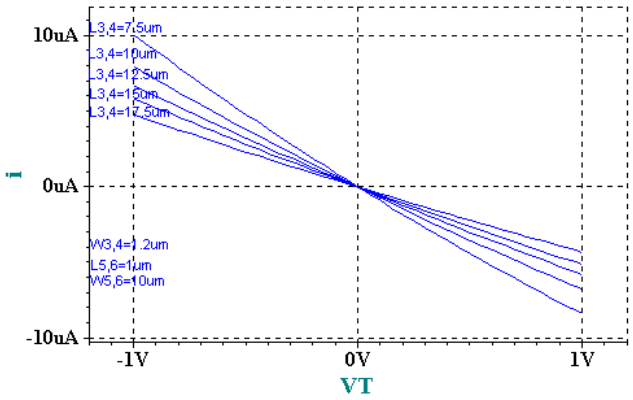

Fig. 12. I-V curves of a circuit in Fig. 11

IV. CROSS-COUPLED MOS RESISTOR CIRCUITS

In section III, the resistor values obtained from the circuits are relatively large. Those values can be reduced significantly if a flip-flop circuit, which is a positive feedback or a cross-coupled pair of MOSFETs, is added at the sources of the differential pair. This flip-flop circuit with a positive feedback introduces a small negative resistance into the circuit, and as result the resistance between nodes A an B is reduced. The NMOS implementation is shown in Fig. 13. All transistors are

designed to operate in saturation region. This circuit produces a wide range of output resistance between two terminals A and B, ranging from negative to positive values. Changing the W/L ratio of the transistors will change the resistance values.

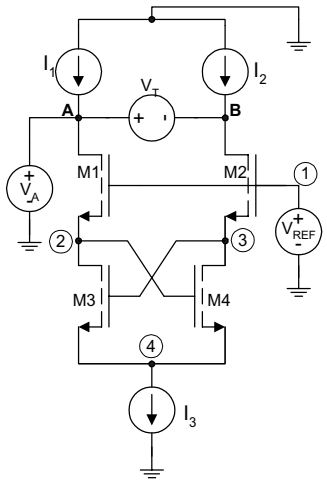

Fig. 13. A cross-coupled NMOS resistor circuit

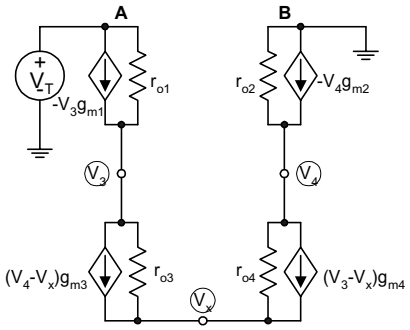

Fig. 14. An equivalent circuit diagram of a cross-coupled NMOS resistor circuit

The circuit diagram in Fig. 14 is equivalent to the circuit in Fig. 13. It's simplified for deriving the following equations. Both M1 and M2 characteristics are perfectly matched as well as M3 and M4. It is to provide a symmetrical circuit so the drain currents in both branches are exactly the same. Its equivalent resistance is given by:

$$R_{eq} = \underbrace{2r_o^{'}}_{A} + \underbrace{2r_o^{''}\left(\frac{1+g_m^{'}r_o^{'}}{1-g_m^{''}r_o^{''}}\right)}_{B} \tag{6}$$

Let assume

$$r_o = r_o^{'} = r_o^{''} \tag{7}$$

Equation (6) can be written as

$$R_{eq} = 2r_o\left\{1-\left(\frac{g_m^{'}r_o+1}{g_m^{''}r_o-1}\right)\right\} \tag{8}$$

The resistance can be reduced to a smaller value. This is true if the biasing conditions on one of the terms in equation (8) are chosen such as

$$\left(\frac{g_m^{'}r_o+1}{g_m^{''}r_o-1}\right)\approx 1 \tag{9}$$

Note that resultant resistance between terminals A and B may have both positive and negative values. The SPICE simulation results for the circuit of Fig. 13 are shown in Fig. 15 where L=1um, W3,4=5um, and W1 and W2 are changed from 2um to 6.5um.

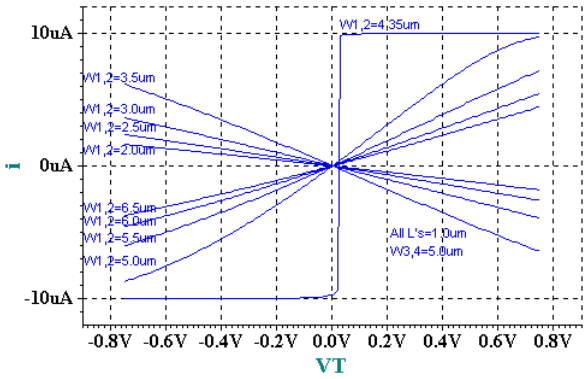

Fig. 15. I-V curves of a circuit in figure 13

The circuit in Fig. 16 is implementing only PMOS. It is complementary of the circuit in Fig. 13. Again, equations (6) to (9) of NMOS are valid for the PMOS circuit. Its SPICE simulation results are shown in Fig. 17 where L1,2=1um, W1,2=15um, W3,4=1.2um, and L3,4 were varied from 2um to 6um.

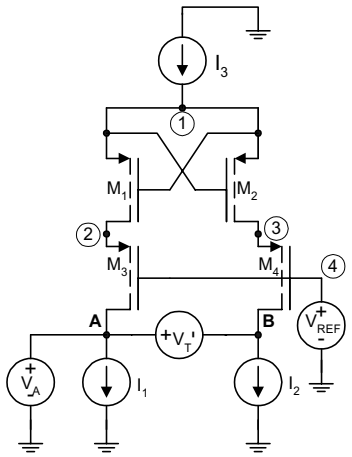

Fig. 16. A cross-coupled PMOS resistor circuit

Similarly, the cross-coupled NMOS and PMOS resistor circuits can be combined together as shown in Fig. 18. It has the same purpose of the circuit in Fig. 11, compensating the non-linearity of the two NMOS and PMOS circuits.

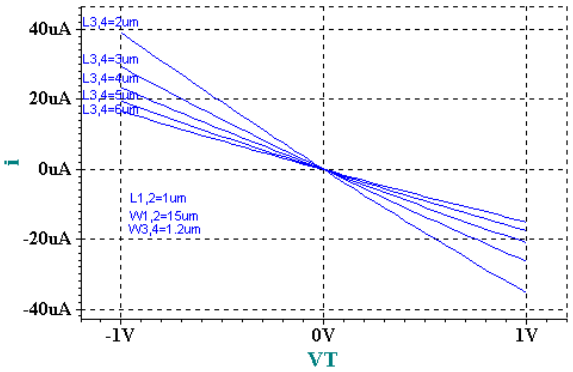

Fig. 17. I-V curves of a circuit in figure 13

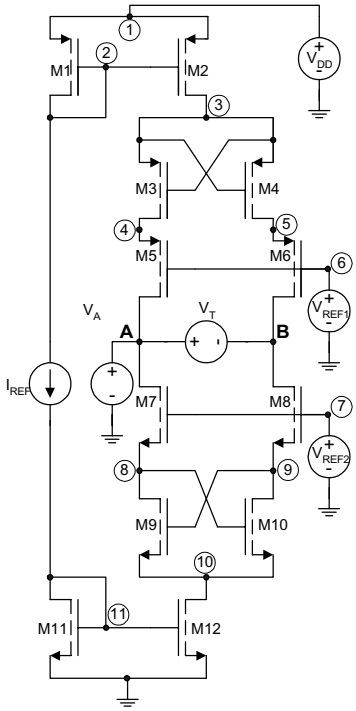

Fig. 18. A combination of NMOS and PMOS circuits

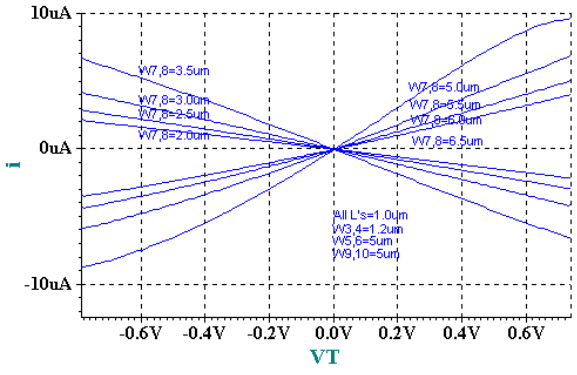

Fig. 19. I-V curves of a circuit in Fig. 18

V. IMPROVED MOS RESISTOR CIRCUITS WITH SMALLER LEAKAGE CONDUCTORS

To improve its leakage resistance, the cascode current mirror circuits can be used as shown in Figs. 20. The cascode current mirror circuits are better current sources because they have higher output resistance, $r_o(1+g_m r_o)$. So adding using the cascode current sources will make the leakage resistance smaller. Fig. 20 is shown as an example of this.

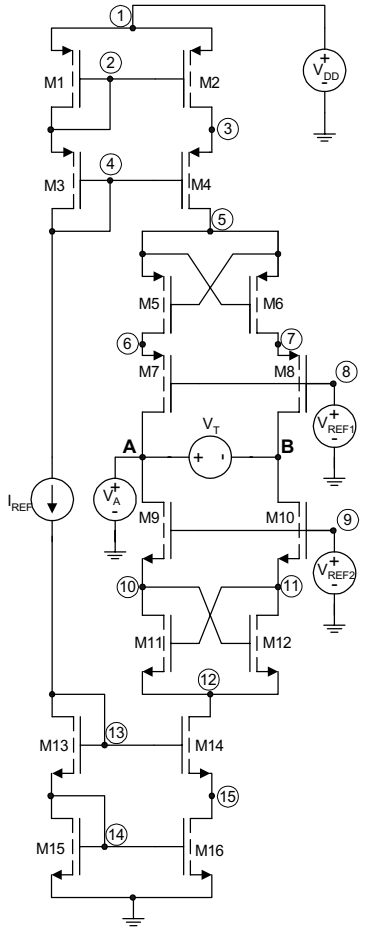

Fig. 20. A modified circuit from Fig. 18 resulting with a smaller leakage resistance

V. CURRENT CONTROLLED RESISTORS

This section is concluded with a brief discussion of a second method for finding a smaller output resistance between terminals A and B of an NMOS resistor circuit as shown in Fig. 21. The drain currents are being diverted from both M3 and M4. Once their drain currents are lessened, it reduces both g_m and r_o values, and R_{eq} becomes smaller. This can also be verified by recalling equation (6).

$$R_{eq} = \underbrace{2r_o^{'}}_{A} + \underbrace{2r_o^{"}\left(\frac{1+g_m^{'}r_o^{'}}{1-g_m^{"}r_o^{"}}\right)}_{B}$$

If $g_m^{"}r_o^{"} > 1$ and $(1-g_m^{"}r_o^{"}) > (1+g_m^{'}r_o^{'})$, the value of part B turns to a negative number and it subtracts that from part A. Therefore, R_{eq} becomes a smaller positive number. Fig. 22 shows the SPICE simulation results of a circuit in Fig. 21 where L=2um, W1,2=5um, and W3,4=10um.

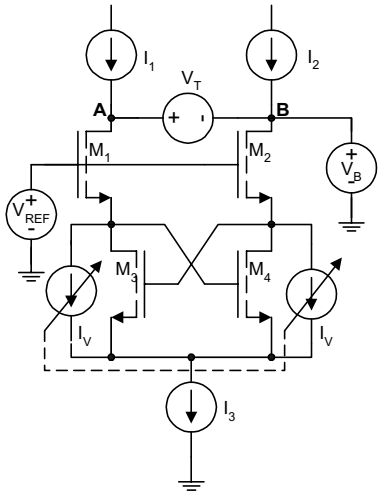

Fig. 21. The current controlled resistors circuit

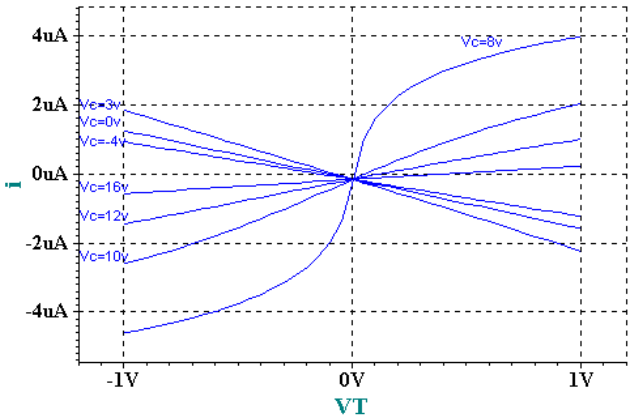

Fig. 22. I-V curves of a circuit in Fig. 21

IV. CONCLUSION

The paper presented the cross-coupled NMOS and PMOS resistor circuits, which were derived from the differential pair circuits. Both cross-coupled NMOS and PMOS circuits can also be combined to partially compensate the non-linearity that exists. The circuits utilize the characteristics of output drain resistance and transconductance. It has lower power dissipations. Adjusting the width and length of the MOSFETs or diverting the input drain currents can vary their resistance values. The circuits also have a relatively large voltage swing, a linear resistance, and a good range of resistance, which can be used in multiplication circuits, internal filter designs, and so on [11]-[13].

V. REFERENCES

[1] M. Ismail and Terri Feirz, "Analog VLSI Signal and Information Processing*"* McGraw-Hill Inc., 1994.

[2] Z. Wang, 2-MOSFET Transresistor with Extremely Low Distortion for Output Reaching Supply Voltage, *Electron. Lett*., 26, pp. 951-952, 1990.

[3] J. I. Osa, s. Porta, A. Carlosena, "The Most Resistive Model for the MOS Resistive Circuit," *Proceedings of the IEEE*, *ISCAS* 1998.

[4] Shigetaka Takagi, Zdzislaw Czarnul, and Nobuo Fujii, "A Synthesis of Highly Linear MOS Circuits and Their Application to Filter Realization," *IEICE Trans. Fundamentals*, vol. E77-A, no. 2, Feb. 1994.

[5] M. Banu and Y. Tsividis, "Floating Voltage-Controlled Resistors in CMOS Technology," *Electron. Lett.,* 18, 678-679, 1982.

[6] Z. Wang and W. GuggenBuhl, "A Voltage-Controllable MOS Transconductor Using Bias Offset Technique," *IEEE J. Solid-State Circuits* SC-25, pp. 315-318, 1990.

[7] S. P. Singh, J. V. Hanson, and J. Vlach, "A new floating resistor for CMOS technology," *IEEE Trans. Circuit Syst.,* vol. 36, pp. 1217-1220, Sept. 1989.

[8] I. Han and s. B. Park, "Voltage-Controlled Linear Resistor by Two MOS Transistors and its Applications to Active RC Filter MOS tntegration," *Proc. IEEE*, vol. 72, pp. 1655-1657, Nov. 1984

[9] T. Shimmi, H. Kobayhashi, T. Yagi, T. Sawaji, T. Matsumoto, and A. A. Abidi, "A Parallel Analog CMOS Signal Processor for Image Contrast Enhancement," *Proc. European solid State Circuits Conference*, pp. 163-166, Sept. 1992.

[10] S. Sakurai and M. Ismail, "A CMOS square-law programmable floating resistor independent of the threshold voltage," *IEEE Trans. Circuits Syst. II,* vol. 39, pp. 565-574, Aug. 1992.

[11] K. Bult and H. Wallinga, "CMOS Four-Quadrant Analog Multiplier," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 3, pp. 430-435, June 1986.

[12] Czarnul Z. "Novel MOS Resistive Circuit for Synthesis of Fully Integrated Continuous-Time Filters," *IEEE Transactions on Circuits and Systems*, vol. CAS-33, no. 7, pp. 718-721, 1986.

[13] Shigetaka Takagi, Zdzislaw Czarnul, and Nobuo Fujii, "A Synthesis of Highly Linear MOS Circuits and Their Application to Filter Realization," *IEICE Trans. Fundamentals*, vol. E77-A, no. 2, Feb. 1994.