Low Power Current Mode Loser-Take-All Circuit for Image Compression

B. M. Wilamowski
wilam@ieee.org
College of Engineering
University of Idaho at Boise
800 Park Blvd, Suite 200
Boise, ID 83712

D. L. Jordan
dljordan@uwyo.edu
Electrical Engineering Dept.
University of Wyoming
Laramie, WY 82071

O.Kaynak
kaynak@boun.edu.tr
Bogazici University
EEE Department
Bebek, 80815 Istanbul,
TURKEY

Abstract - *This paper presents a low power and accurate current mode synchronous Loser-Take-All circuit based on a two transistor regenerative pair. It achieves its high speed through regenerative feedback. The circuit does not require extra biasing since all required power is taken from input currents, which are being compared. This paper also includes simulation results for a single LTA circuit with two inputs, and for a sixty-four inputs, six layer, binary tree circuit. With power supply less than 2.5V it is possible to cascade up to 10 layers in the binary tree and as result 1048 inputs can be compared. With a larger power supply (about 0.2V per additional layer) the number of inputs to be compared are practically unlimited.*

1 Introduction

The MAX or Winner-Take-All (WTA) and MIN or Loser-Take-All (LTA) circuits are important parts of many neuro-fuzzy systems. MIN and MAX circuits are the prime components of fuzzy logic. WTA circuits are used in many neural layer architectures such as Learning Vector Quantization (LVQ), Adaptive Resonance Theory (ART), Kohonen feature maps, and many others.

Günay and Sánchez-Sinencio [1] provide a detailed overview and comparison of several CMOS WTA circuits. However, the overview [1] limits its consideration to asynchronous circuits neither does it mention several newer concepts [2-4] Asynchronous WTA circuits processing and comparing signals in continuous mode and finding the winner as the signals change. On the other hand, these circuits tend to have rather limited accuracy for multiple inputs due to signal interaction and the difficulty in matching transistors, which are not near to each other. In asynchronous circuits, to obtain acceptable resolution, the number of inputs are limited to ten or fewer.

Some applications, such as LVQ for graphics compression, require sorting out of hundreds of signals. Demosthenous, et al., [5] developed a binary tree approach that solves this problem with a circuit using three current mirrors and one latch per synchronous WTA stage. This design requires a circuit with sixteen transistors per cell, or twelve transistors (when complimentary design techniques are used). Current mirrors are also possible sources of additional errors. This paper proposes an alternative approach: take the DeMorgan transform of

the inputs, then compare them using synchronous LTA (Loser Take All) circuits and this leads to simple and more accurate design. Higher accuracy is possible since there is no requirement for high precision current mirrors. Even a design of such mirrors is simple their transistors must be of large size to secure adequate accuracy.

2 The LTA comparator circuit

The LTA comparator shown in Fig. 1 has behavior similar to that of flip-flops and of the sense amplifiers found in dynamic memories. In order to simplify the discussion and analysis all parasitic capacitances, C1 though C5, have been lumped into the equivalent capacitors C_{eq1} and C_{eq2}. This approximation is valid because grounded capacitances have dominant values and one can represent the much smaller coupling capacitances due to the Miller as grounded capacitors. These coupling capacitances have no effect on accuracy of comparison since the Miller effect enhancement takes place only during the latch up process, which occurs when currents are already compared.

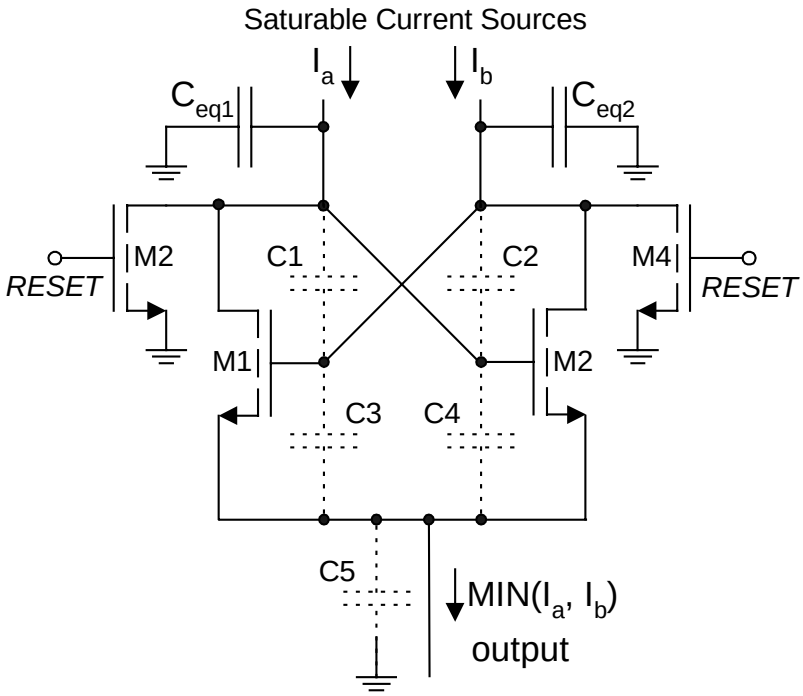

Fig. 1. Proposed LTA circuit showing the reset transistors and parasitic capacitances.

The input currents begin charging input capacitances C_{eq1} and C_{eq2} while transistors M3 and M4 turn off. The regenerative action starts when the closed-loop gain through transistors M1 and M2 becomes greater than one. This occurs while both transistors are still in deep subthreshold conduction.

$$g_{m1}R_{L1}g_{m2}R_{L2} > 1 \tag{1}$$

Note that the transconductance g_m for transistor operating in subthreshold mode is defined by

$$g_m = \frac{I_D}{\eta V_T} = \frac{I_D q}{\eta k T} \tag{2}$$

while the output resistances of input current sources dominate the load resistances R_L, which is given by:

$$R_L = \frac{1}{\lambda I_D} \tag{3}$$

Therefore equation (1) can be rewritten as:

$$\frac{I_{D1}}{\eta V_T} \cdot \frac{1}{\lambda I_{inp1}} \cdot \frac{I_{D2}}{\eta V_T} \cdot \frac{1}{\lambda I_{inp2}} > 1 \tag{4}$$

where $V_T \approx 25mV$ is the thermal potential, $\eta = 1.5 \sim 2$ and $\lambda = 0.02 \sim 0.04\ 1/V$ for a typical CMOS process. Rearranging equation (4), one may find that

$$\sqrt{\frac{I_{D1} I_{D2}}{I_{inp1} I_{inp2}}} > \lambda \eta V_T \approx 0.0017 \quad : \quad \begin{cases} \eta = 2, \\ \lambda = 1/30 \quad V^{-1}, \\ V_T = 25.8mV \end{cases} \tag{5}$$

This means that the regeneration process starts very early with the drain currents I_{D1} and I_{D2}, significantly smaller that input currents I_{inp1} and I_{inp2}:

$$I_{D1} I_{D2} > 3 \cdot 10^{-6} I_{inp1} I_{inp2} \tag{6}$$

Equation (6) validates earlier assumption that current comparison is done when transistors are still in subthreshold mode. The rest of the process is regenerative latch up where currents and voltages stabilizes in one of two possible states but this process has nor effect on accuracy of comparison. The input current comparison is done when transistors' currents are very small.

In the case of equal input currents, noise in the circuit sets the direction of the regenerative action, thus preventing both M1 and M2 from finishing in a conducting state. Eventually, the transistor carrying current from the minimum input becomes fully conductive while the transistor associated with the larger input current is turned off. Note that, as a result of the action, the LTA comparator shorts the input with smaller current to the output terminal while input with larger current is blocked. After comparison, the voltage on the smaller input drops nearly to zero while the other input nearly reaches the level of the positive power supply.

Figure 2 shows an example SPICE simulation for such a pair from Fig. 1. Note that the regenerative action starts when transistor are operating in a subthreshold conduction mode. The latch up process is relatively fast resulting with clear selection of winner and loser. After that transients in the circuits persist for some time when parasitic capacitances on the rejected branch (with larger input current) are being charged up. This undesirable effect does not affect comparison accuracy but leads to longer time to reach the steady state.

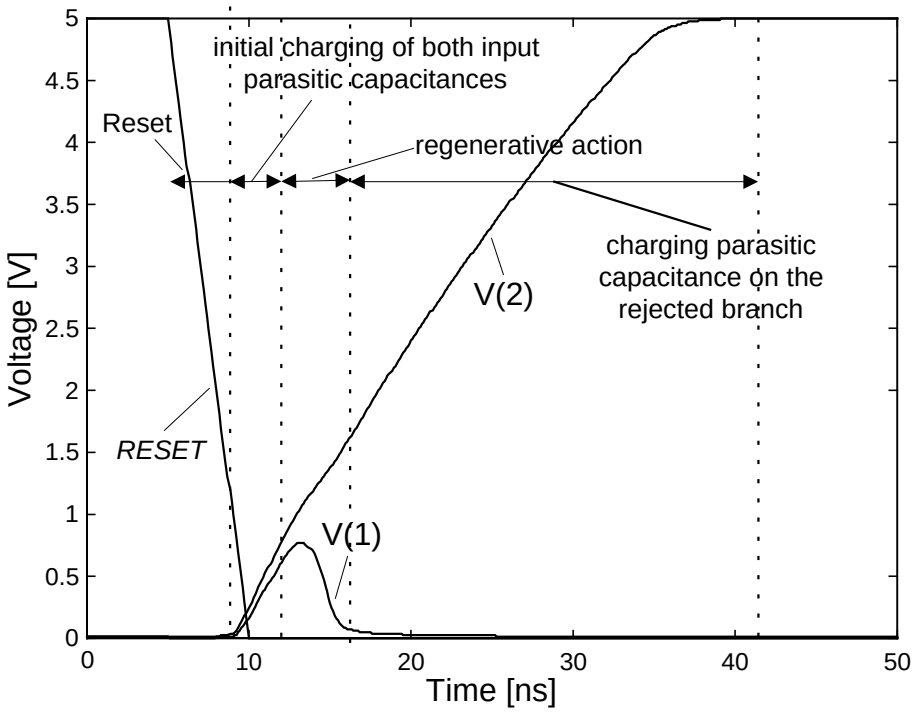

Fig. 2. Voltage Waveforms for the LTA Cell obtained with SPICE simulation for I_a=7.5uA, I_b=10uA.

.

After comparison on the rejected input voltage is equal to supply voltage, a very small voltage drop exists on the conduction branch:

$$\Delta V = I_{MIN} \cdot R_{ON} \approx I_{MIN} \cdot \frac{1}{K' \frac{W}{L}\left(V_{BB} - V_{TH}\right)} \tag{3}$$

where K' is transconductance parameter V_{TH} is the threshold voltage for M1 and M2, and V_{BB} is supply voltage. If current to be compared are smaller than 100uA then for typical MOS transistors the maximum voltage drop on the comparator is lest then 0.1V. This way many comparator circuits can be connected in cascade even if supply voltage is low. Such solution is discussed with details in section 5.

3 Booster Circuit

Please note that the settling time as shown in Fig 2 is determinate by a time of charging parasitic capacitances by the larger of two input currents. In the case of Figure 2 this current is 10uA and steeling time is about 30 ns. But for smaller currents this time increases significantly and for example if the larger current is 0.1uA then it may reach an unacceptably large value of 3us. In order to eliminate this undesirable effect, in addition to reset transistors, a special booster circuit must be added to each input node of the current comparator as shown in Fig. 3. When RESET signal is high transistor M3 is on and LTA circuit is in the precharge state at the same time PMOS transistor M7 is off and the booster circuit is inactive. When RESET signal goes low then transistor M3 is turned off and transistor M7 is turned on and all current flows initially through

transistor M5 the gate of which has initially close to zero voltage and the gate of M6 is biased with a potential slightly larger then threshold voltage ($V_{REF} \approx 1.0V$). This condition (M5 is on and M6 is off) persists during the initial latching process. When voltage on input LTA node exceeds the reference voltage, all current from M7 will be driven to the input node charging it very fast. In our design the W/L ratio of M7 was set in such way that the charging current was around 100uA and the setting time is below 5ns.

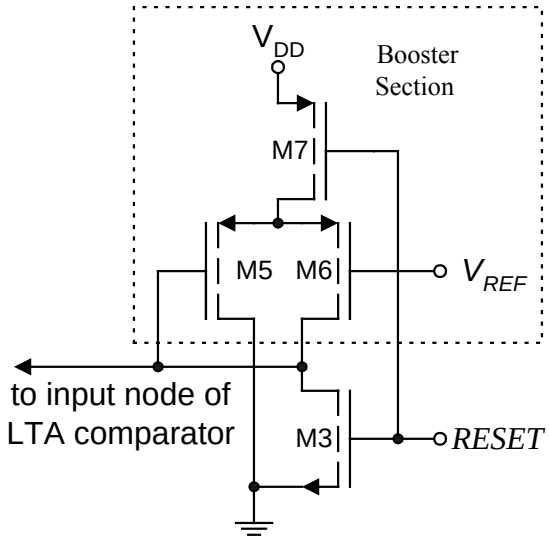

Fig. 3. Booster circuit

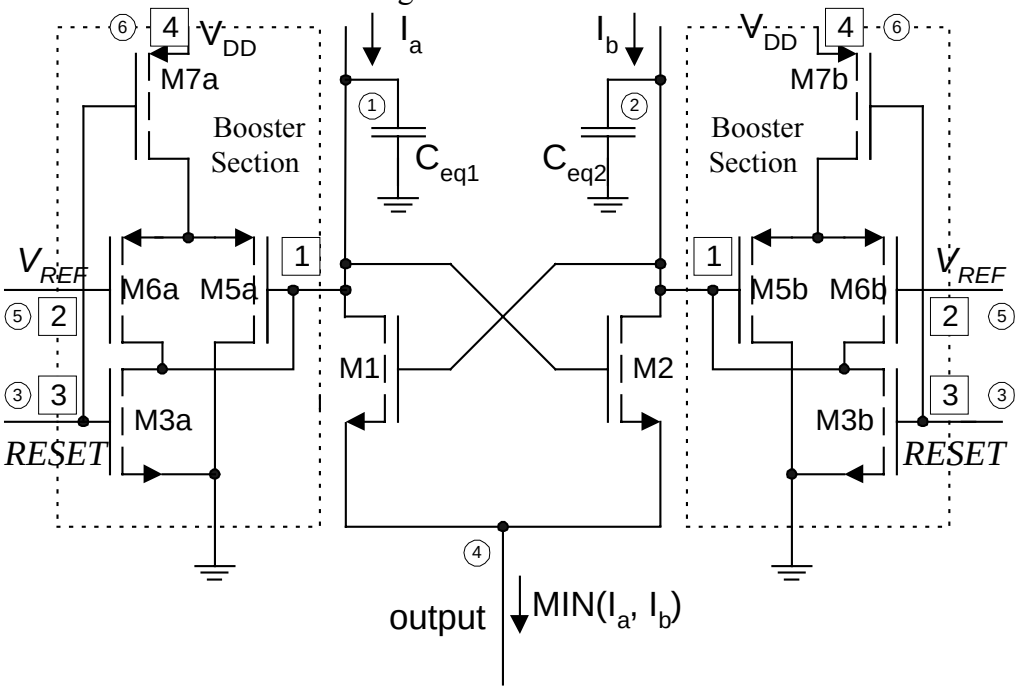

Fig. 4. Comparator circuit with boosters

Boosters do not affect the accuracy of the binary tree since they only activate in branches rejected by lower layers. The value of the reference voltage V_{REF} should correspond to the voltage level that only rejected input can reach. For example, one may conclude from Fig. 1 that it should be around 1V. For the subsequent, upper layers, due to extra ohmic drop the reference voltage should be properly increased, let say 0.1V per layer.

4 Extending the LTA Design for Multiple Inputs

The basic LTA comparator can be used in a binary tree structure, as shown in Fig. 5, in order to compare many input currents. Such an approach leads to a high comparison since the comparison is done always only for two signals and by a subcircuit with well-matched transistors fabricated close to each other. The concept shown in Fig. 5 works correctly for practically unlimited number of inputs since each additional layer introduces only the ohmic voltage drop of a highly conductive transistor. Fig. 6 shows simulation results for six layer system with 64 inputs. Note that two smallest currents were on node 1 (44.2uA) and node 63 (44.6uA). As the result of comparisons on six subsequent layers all large current were rejected and only the smallest current of 44.2uA was delivered to the output. The entire circuit was supplied with 2.5V and such "large" voltage was primarily enforced not be the multilayer comparator circuit but more by the sensing high quality current mirror on the output

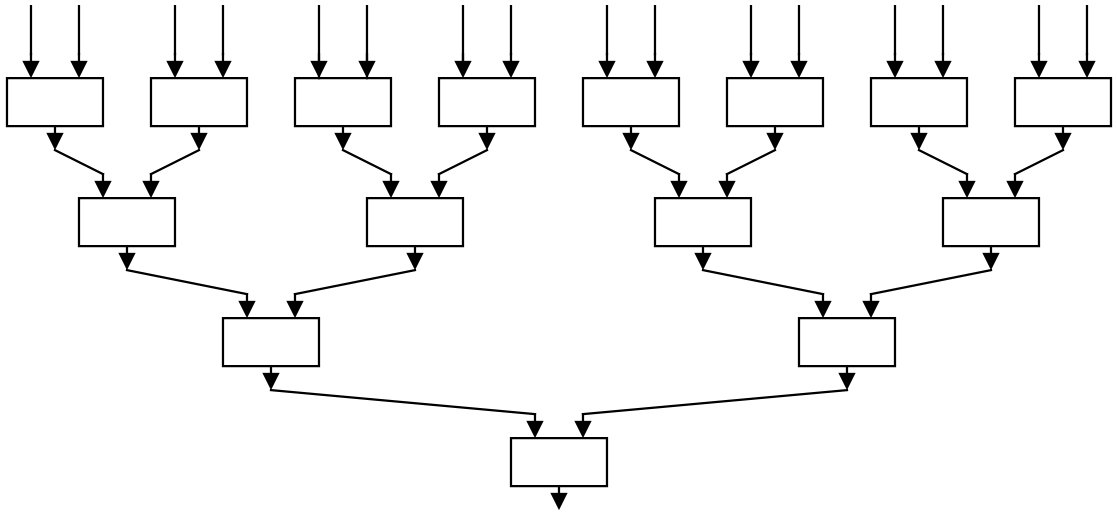

Fig. 5. Four layer LTA circuit for 16 inputs.

In our simulation experiments with six-layer circuit (which consists about 320 transistors) with randomly chosen input currents we always received a correct selection. Even all layers were triggered at the same time. But this is not always true especially when more layers were added. In such a complex circuit the propagation time on different path could be different and this may affect comparison accuracy. This possible difficulty can be solved by triggering (RESET goes low) of subsequent layers with delays. To speed up the process not one but couple neighboring layers may be triggered and the same time.

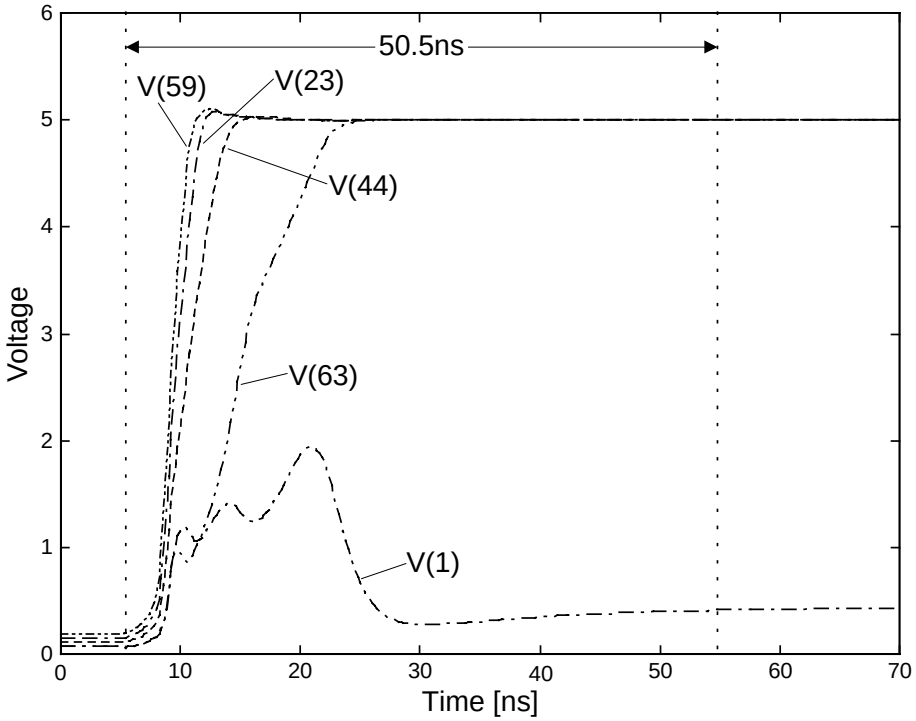

Fig. 4. Simulation Results for the 64-Input Binary Tree.(only waveforms on selected nodes are shown)

One can easily extend the concept to rank incoming currents by successive elimination of the losers. Simply detect the input with a voltage near ground, then supply that input with a large current during the next selection cycle.

6 Conclusion

The LTA circuit presented here appears to achieve the objectives of high speed and high accuracy. It accomplishes its high accuracy by eliminating current mirrors in the circuit and with relatively simple and compact designs with the transistors residing in close proximity to each other. The circuit can process a large number of inputs using a binary tree structure. Its high speed comes from regenerative feedback, small parasitic capacitances resulting from the simple design, and the existence of booster circuits for rapid charging of rejected inputs.

In our simulation experiments using six-layer circuit with randomly chosen input currents we always received a correct selection. In [5] special “backward-pass” circuit was proposed to identify the winning input. This is not necessary using the approach proposed here. The loser, (the input with the smallest current) will always have voltage near ground while all other inputs will have voltages near the positive rail.

One can easily extend the concept to rank incoming currents by successive elimination of the losers. Simply detect the input with a voltage near ground, then supply that input with a large current during the next selection cycle.

Parasitic capacitances and the maximum input current levels usually dominate the speed of the LTA, indicating the use of the smallest gates possible in the regenerative pair. On the other

hand in order to increase comparison accuracy transistors with larger dimensions (smaller relative errors) should be fabricated. Ohmic voltage drops and the supply voltage limit the maximum number of layers.

One may conclude that if input currents are small ($I_{IN} < 10$ uA => 0.05V drop per layer) and a 3V power supply, it should be possible to set more than 20 layers in cascade for comparing up to 2^{20} inputs. In other words, chip size limits the practical number of inputs more than the supply voltage.

References

[1] Z. S. Günay and E. Sánchez-Sinencio, "CMOS Winner-Take-All Circuits: A Detail Comparison," 1997 IEEE International Symposium on Circuits and Systems, June 9-12, 1997, Hong Kong, pp. 41-44.

[2] S. Siskos, S. Vlassis, I. Pitas, "Analog Implementation of Fast Min/Max Filtering," *IEEE Trans. Circuits Syst.II*, vol 45, no. 7, July 1998, pp. 913-918.

[3] T. Serrano, B. Linares-Barranco, "A Modular Current-Mode High-Precision Winner-Take-All Circuit," *IEEE Trans. Circuits Syst.II*, vol 42, no. 2, February 1995, pp. 132-134.

[4] B. Şekerkiran, U. Çilingiroğlu, "Precision Improvement in Current-Mode Winner-Take-All Circuits Using Gain-Boosted Regulated-Cascade CMOS Stages," *IEEE IJCNN*, 1998, pp. 553-556.

[5] A. Demosthenous, S. Smedley, J. Taylor, "A CMOS Analog Winner-Take-All Network for Large-Scale Applications," *IEEE Trans. Circuits Syst. I*, vol. 45, no. 3, March 1998, pp. 300-304.