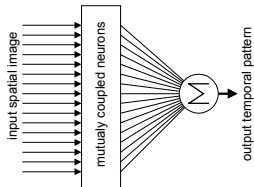
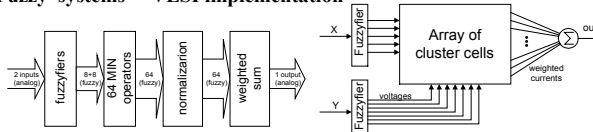


Figure 1 displays eight grayscale images arranged in a 2x4 grid, illustrating the evolution of a square wave pattern. The top row shows the pattern becoming increasingly blurred from left to right. The bottom row shows the pattern becoming increasingly noisy and fragmented from left to right.

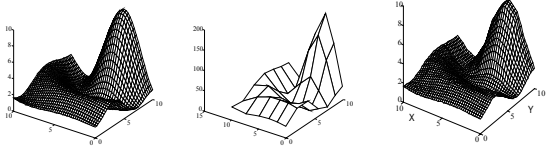
The diagram shows a CMOS inverter circuit. The PMOS transistor's source is connected to V_{DD} and its gate is connected to the input. The NMOS transistor's source is connected to ground and its gate is also connected to the input. The output of the inverter is taken from the common drain connection. Parasitic elements are modeled as follows: the input node has a parasitic capacitance C_1 to ground and a parasitic resistance R_1 to the PMOS gate; the output node has a parasitic capacitance C_2 to ground and a parasitic resistance R_2 to the NMOS gate. Both input and output nodes are also connected to a network of resistors representing coupling to neighboring circuit elements.



Fuzzy systems VLSI implementation

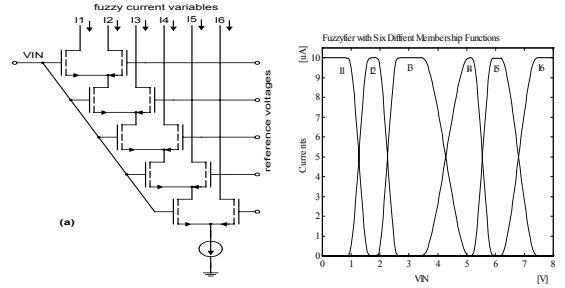


Block diagrams of the fuzzy VLSI chip



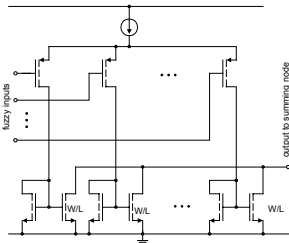
Control surfaces: (a) desired control surface, (b) information stored in defuzzifier as weights, and (c) measured control surface of VLSI chip

Fuzzy systems VLSI implementation 2

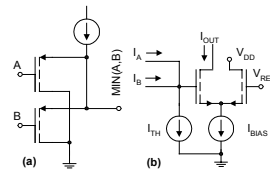


Fuzzifier (a) circuit diagram of fuzzifier, (b) example of the SPICE simulation

Fuzzy systems VLSI implementation 3

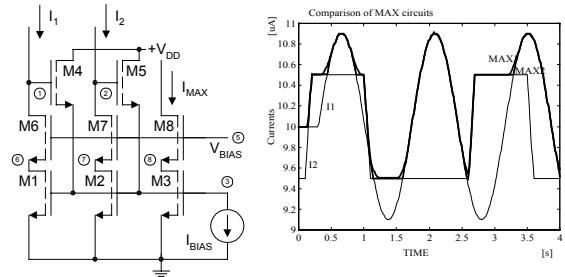


Defuzzifier using normalization and weighted sum



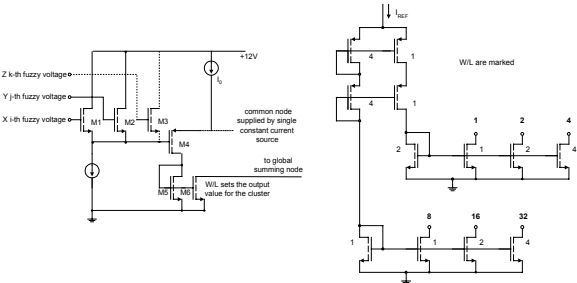
Selection circuits (a) MIN circuit in voltage mode (b) neuron circuit with threshold in the current mode

Fuzzy systems VLSI implementation 4



MAX operators (a) concept diagram and (b) simulation results for MAX1 and for the proposed MAX2.

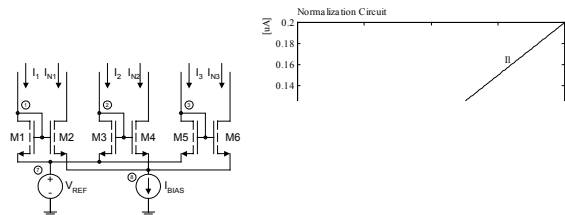
Fuzzy systems VLSI implementation 5



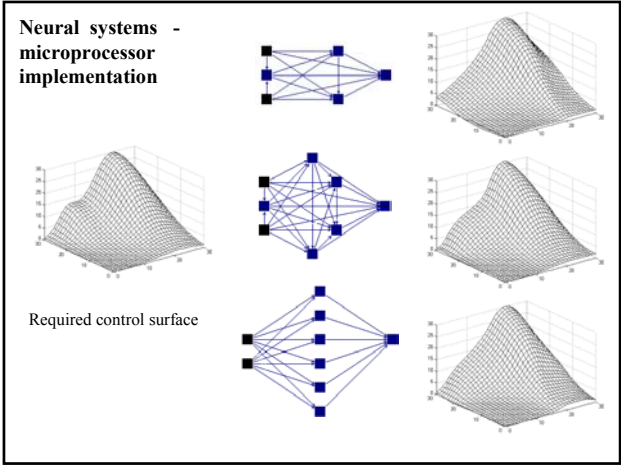
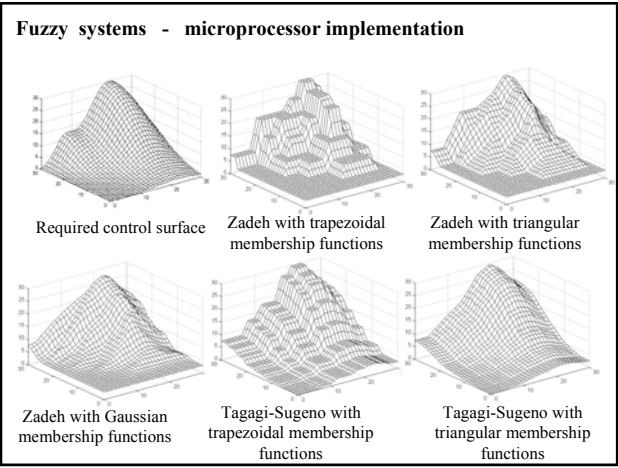
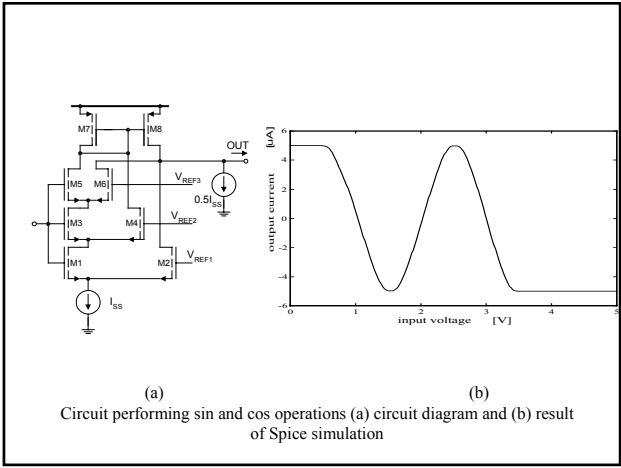
The cluster cell with rule selection (transistors M1-M4) and defuzzification (source I_0 and transistors M4-M6)

Six bit programmable current sources

Fuzzy systems VLSI implementation 6



Normalization circuit (a) circuit diagram and (b) characteristics



Comparison of various fuzzy and neural controllers

Type of controller	Error MSE
Zadeh with trapezoidal	0.945
Zadeh with triangular	0.671
Zadeh with Gaussian	0.585
Tagagi-Sugeno with trapezoidal	0.309
Tagagi-Sugeno with triangular	0.219
Tagagi-Sugeno with Gaussian	0.306
Neural network with 3 neurons in cascade	0.00057
Neural network with 5 neurons in cascade	0.00009
Neural network with 6 neurons in one hidden layer	0.00030