Simple way of teaching transistor amplifiers

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Abstract

For small signal analysis a simple change from commonly used tranconductance g_m to transresistance $r_m=1/g_m$ leads to a significant simplification of all equations. Moreover these equations are much easier to memorize since they have a form of resistor ratio for CE (CS) and CB (CG) configurations and the form or resistor divider for CC (CD) configuration.

With presented approach most of students are able to read diagrams and to understand the effect of each element change on the circuit performance. Students are not lost with messy equations, but they are in control of their design and they know which parameters they have to change in order to change behavioral characteristics.

I. Introduction

Students usually have significant difficulties in memorizing all the equations for calculation of gain, input and output resistances for transistor amplifiers [1][2][3][4]. They do relatively well if a common source (emitter) is used, but they are lost when other configurations are considered. In the paper, a simple way for analysis of transistor amplifiers is introduced. At first, approximate and accurate methods for circuit biasing are discussed including both BJT and FET amplifiers. All transistor circuit analysis should be always performed in the following order:

1. Biasing point calculation
2. Calculation of small signal parameters
3. Gain, input and output resistance calculation

This paper is also organized in that way.

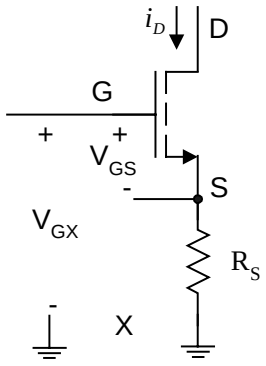


Fig. 1 Biasing calculation for FET transistor with series of resistor R_S

II. Biasing calculation

Calculation of the biasing point for bipolar transistor circuits are relatively straightforward and usually students do not have a problem with that. If it would be possible one should

recommended using a simplified approach instead of using the full Thevenin equivalent circuit. In the case of CMOS circuits it is usually relatively easy to figure out all transistor currents. There is, however one difficult exception in the MOS circuitry. This is the case for JFETs and MOS transistors, shown in Fig. 1, where a resistor is connected with the series in the source.

Usually to find a biasing point a quadratic equation should be solved. It is however much easier to use the following approach.

For n-channel FET transistor

$$V_{GS} = \frac{1}{R_S K}\left[\sqrt{2R_S K(V_{GX} - V_{TH})+1} - 1\right] + V_{TH} \quad . \tag{1}$$

For n-channel FET transistor

$$V_{GS} = \frac{1}{R_S K}\left[\sqrt{-2R_S K(V_{GX} - V_{TH})+1} - 1\right] + V_{TH} \tag{2}$$

and the drain current is

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 \tag{3}$$

where K is transconductance parameter, V_{TH} is threshold voltage. The direct formula for drain current is

$$I_D = \pm \frac{V_{GX} - V_{TH} - \frac{1}{R_S K}\left[\sqrt{\pm 2R_S K(V_{GX} - V_{TH})+1} - 1\right]}{R_S} \tag{4}$$

where the minus sign should be used for p-channel devices.

Example 1

The circuit of Fig. 1 has V_{GX}=2V, R_S=10kΩ, V_{TH}=0.8V, and K=0.5mA/V^2.
Find the transistor current.

Solution

$R_S K = 5V^{-1}$

From (1) $V_{GS} = \frac{1}{R_S K}\left[\sqrt{2R_S K(V_{GX} - V_{TH})+1} - 1\right] + V_{TH} = \frac{1}{5}\left[\sqrt{2 \cdot 5(2-0.8)+1} - 1\right] + 0.8 = 1.52V$

and from (3)

$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 = \frac{0.5}{2}(1.52 - 0.8)^2 = 0.13mA$

III. Small signal transistor parameters

The usage of *h* parameters is quite common for describing the small signal model of transistors. Unfortunately these parameters confuse students. In the case of bipolar transistor only three $r_m = 1/g_m$, r_o, and β but not four *h* parameters are needed. Since β changes about 1% per

^{o}C and there is large β spread between elements the acceptable assumption is that $\beta \approx \beta + 1$ and this leads to further simplification. The small signal equivalent model of bipolar transistor is shown in Fig. 2 and 3. In the presented approach small signal model of Fig. 3 will be used.

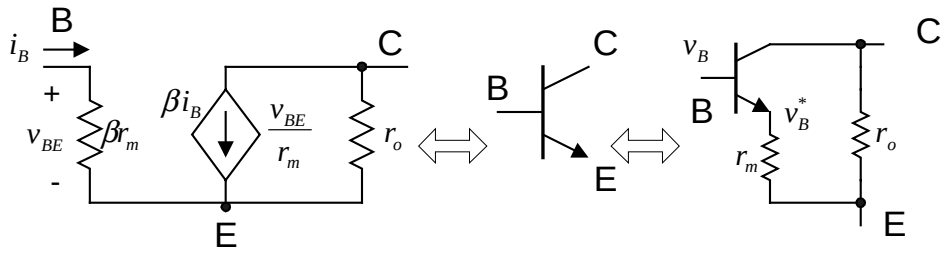


Fig. 2. Small signal equivalent model of bipolar transistor. For small signal analysis $v_B = v_B^*$.

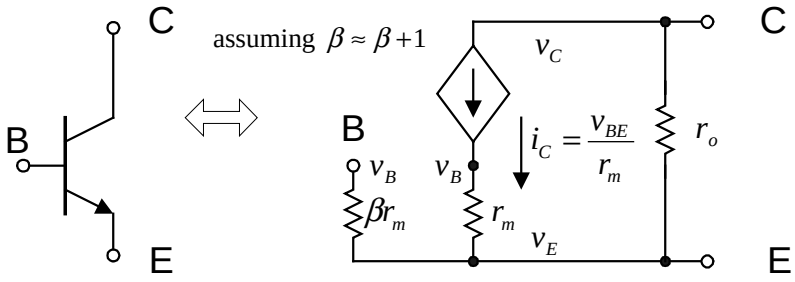


Fig. 3. Small signal equivalent model of bipolar transistor used in analysis.

Small signal parameters for bipolar transistor are:

$$r_m = \frac{h_{11}}{\beta+1} = \frac{1}{g_m} = \frac{V_T}{I_C} \quad , \quad r_o = \frac{1}{h_{22}} = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C} \quad , \quad \beta = h_{21}, \text{ and } \; h_{12} = 0 \tag{5}$$

where thermal potential $V_T = \frac{kT}{q} \approx 25\text{mV}$ and Early voltage $V_A \approx 50 \div 200\text{V}$

When substrate effects are neglected MOS linear model is described only by two parameters $r_m = 1/g_m$ and r_o.Equivalent diagrams of FET transistors are shown in Fig. 4 and 5. In the presented approach small signal model of Fig. 5 will be used. Small signal parameters for FETs are:

$$r_m = \frac{1}{g_m} = \frac{V_{GS} - V_{TH}}{2I_D} = \frac{1}{K(V_{GS} - V_{TH})} = \frac{1}{\sqrt{2KI_D}} \qquad r_o = \frac{V_A + V_{DS}}{I_D} = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \approx \frac{V_A}{I_D} = \frac{1}{\lambda I_D} \tag{6}$$

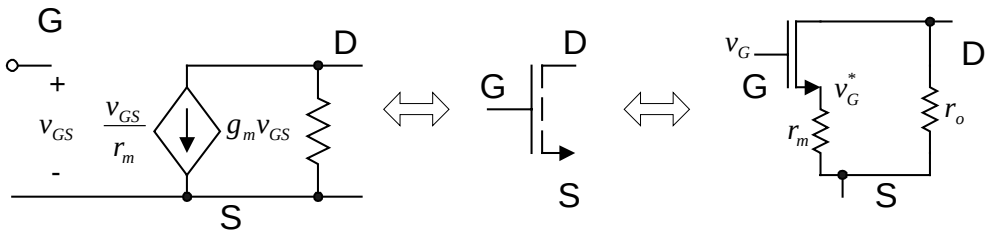


Fig. 4. Small signal equivalent model of MOS transistor. For small signal analysis $v_G = v_G^*$.

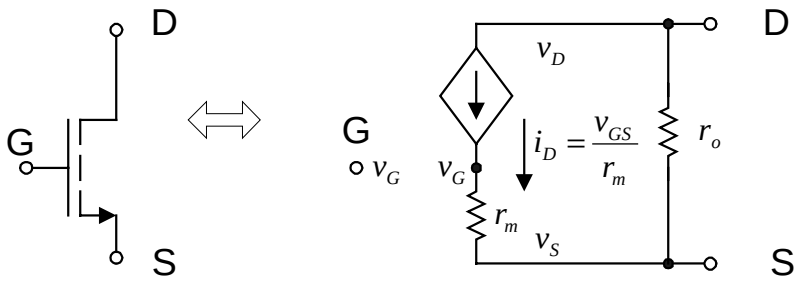
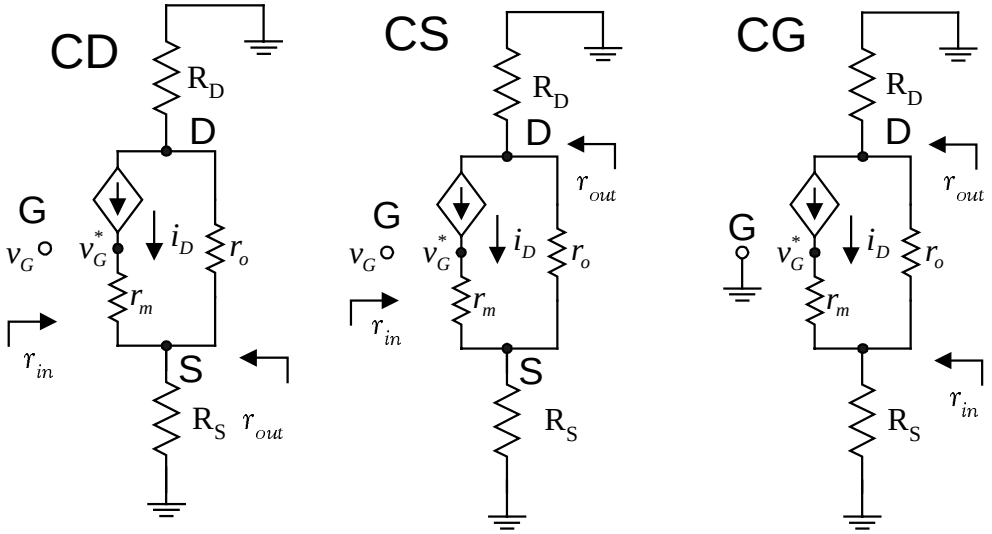


Fig. 5. Small signal equivalent model of MOS transistor used in analysis.

IV. Gain calculation

There are three basic circuit configurations for single transistor amplifier. Larger circuits can be almost always considered as a composition of these single-transistor amplifiers. Example 3 in the end of this presentation illustrates this type of approach. For bipolar transistors there are common collector CC, common emitter CE, and common base CB configurations. For FETs there are common drain CD, common source CS, and common gate CG configurations. Diagrams for all three FET configurations are shown in Fig. 6.



(a) (b) (c)

Fig. 6. Basic configurations of single transistor amplifiers with idealized transistor models: (a) common drain (voltage follower), (b) common source, and (c) common gate.

In the case of the common drain configuration shown in Fig. 6(a), the voltage gain can be found by inspecting the diagram and using resistor divider formula. For $v_G = v_G^*$ and $r_o >> r_m$

$$v_{out} = \frac{R_S}{R_S + r_m} v_G \qquad \text{or voltage gain} \qquad A_v = \frac{v_{out}}{v_G} = \frac{R_S}{R_S + r_m} \tag{7}$$

The input resistance is $r_{in} \approx \infty$ and output resistance is $r_{out} = R_S \parallel r_m = \frac{R_S r_m}{R_S + r_m}$

In the case of the common source configuration shown in Fig. 6(b) also we have to note that the small signal voltage on *x* node follows the gate voltage. For $v_G = v_G^*$ and $r_o >> r_m$ the drain current is:

$$i_D = \frac{v_G}{R_S + r_m} \tag{8}$$

and from the ohms law the output voltage is:

$$v_{out} = -i_D R_D = -\frac{R_D}{R_S + r_m} v_G \quad \text{and the voltage gain} \quad A_v = \frac{v_{out}}{v_G} = -\frac{R_D}{R_S + r_m} \tag{9}$$

The minus sign in equation above comes from the different directions (in respect to ground) of currents through resistor r_m and R_D. The input resistance is $r_{in} \approx \infty$ and output resistance is $r_{out} = R_D$. Note that the resistance of idealized transistor seen from the drain side is equal to infinity and the resistance seen from the source side is equal to zero.

In the case of the common gate configuration shown in Fig. 6(c) $v_G = 0$, assuming that the input voltage source is ideal (has no series resistance) the small signal drain current is:

$$i_D = \frac{v_{in} - v_G}{r_m} = \frac{v_{in}}{r_m} \tag{10}$$

and from the ohms law the output voltage is:

$$v_{out} = i_D R_D = \frac{R_D}{r_m} v_{in} \quad \text{and the voltage gain} \quad A_v = \frac{v_{out}}{v_{in}} = \frac{R_D}{r_m} \tag{11}$$

There is no minus sign in above equation because the small signal current through r_m is excited from a different direction. The input resistance is $r_{in} = R_S \,||\, r_m$ and output resistance is $r_{out} = R_D$.

The presented above approach with idealized transistors allows us a fast calculation of basic parameters of transistor amplifiers. This simplified approach is good enough for students to understand how each circuit parameter affects the circuits performance. They learn if the value of resistance should increase or decrease to obtain required parameters.

Example 1

Find voltage gain, input and output resistance for the amplifier with PMOS transistor shown in the Fig 7, and in this problem do not ignore r_o. Assume that K= 200 μA/V^2, λ=0.03V^{-1}, I_D= 10μA, R_1=1MΩ, R_2=5MΩ, R_D=0.3MΩ,

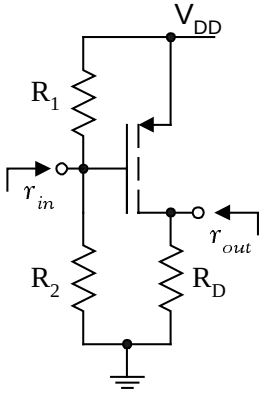


Fig. 6. Circuit of Example 1

Solution

The small signal parameters r_o and r_m of the PMOS transistor must be found at first. Using (6)

$$r_m = \frac{1}{g_m} = \frac{1}{\sqrt{2KI_D}} = 15.8\text{k}\Omega \quad r_o \approx \frac{1}{\lambda I_D} = 3.33\text{M}\Omega$$

The small signal diagram of the circuit using equivalent PMOS model with idealized is shown in Fig. 8. Note that both diagrams on Fig. 8(a) and Fig. 8(b) are identical, somehow drawn differently. An experienced student can use the diagram from Fig. 8(a), while a less experienced one has to redraw the diagram to the form shown in Fig. 8(b)

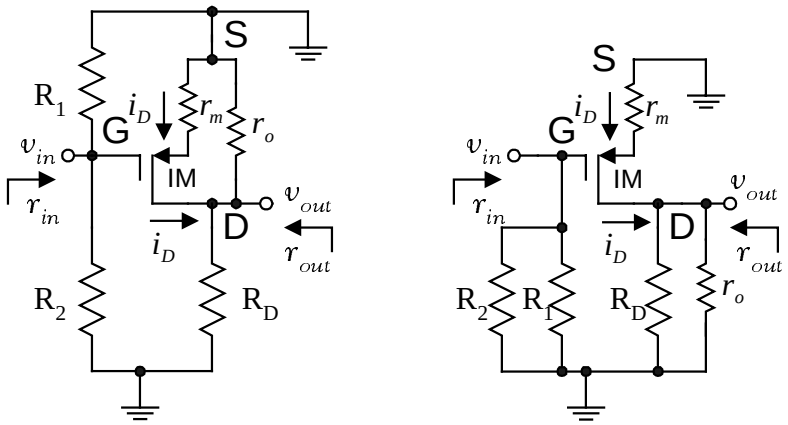


Fig.8. Small signal equivalent diagrams of circuit of Fig. 7.

By inspecting diagrams on Fig. 8(a) or Fig. 8(b) one can find that:

$$i_D = -\frac{v_{in}}{r_m}$$

and from the ohms law the output voltage is:

$$v_{out} = i_D R_D \,||\, r_o = -\frac{R_D \,||\, r_o}{r_m} v_{in}$$

and the voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{R_D \,||\, r_o}{r_m} = -\frac{0.3\text{M}\Omega \,||\, 3.33\text{M}\Omega}{15.8\text{k}\Omega} = -17.4$$

The input resistance is $r_{in} = R_1 \,||\, R_2 = 0.83\text{M}\Omega$

and output resistance is $r_{out} = R_D \,||\, r_o = 275\text{k}\Omega$

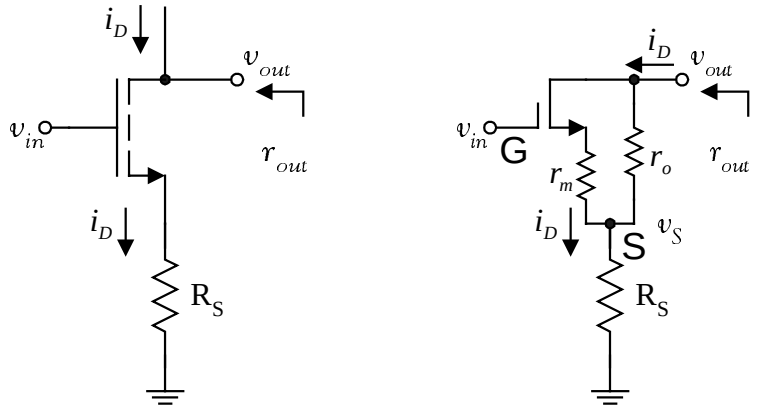
If both R_S and r_o are included in the transistor model computations are usually more complicated than in the Example 1. Let us consider a very important case shown in Fig. 9.

The out resistance (assuming $v_{in} = 0$) is:

$$r_{out} == r_o + R_S\left(1 + \frac{r_o}{r_m}\right) \tag{12}$$

Effective transconductance (assume $v_{out} = 0$)

$$r_m^* = \frac{1}{g_m^*} = \frac{r_m R_S}{r_o} + r_m + R_S \approx r_m + R_S \tag{13}$$



(a) (b)

Fig. 9. Common source configurations of single transistor amplifier: (a) circuit diagram and (b) equivalent small signal model with idealized transistor including r_o parameter

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Example 3

Find Q-points and the differential-mode voltage gain of the opamp of in Figure 10 if $V_{DD}=V_{SS}=7.5V$, $I_{REF}=250\mu A$, $K'_n=25\mu A/V^2$, $V_{TN}=0.75V$, $\lambda_n=0.017V^{-1}$, $K'_p=10\mu A/V^2$, $\lambda_p=0.017V^{-1}$, and $V_{TP}=-0.75V$.

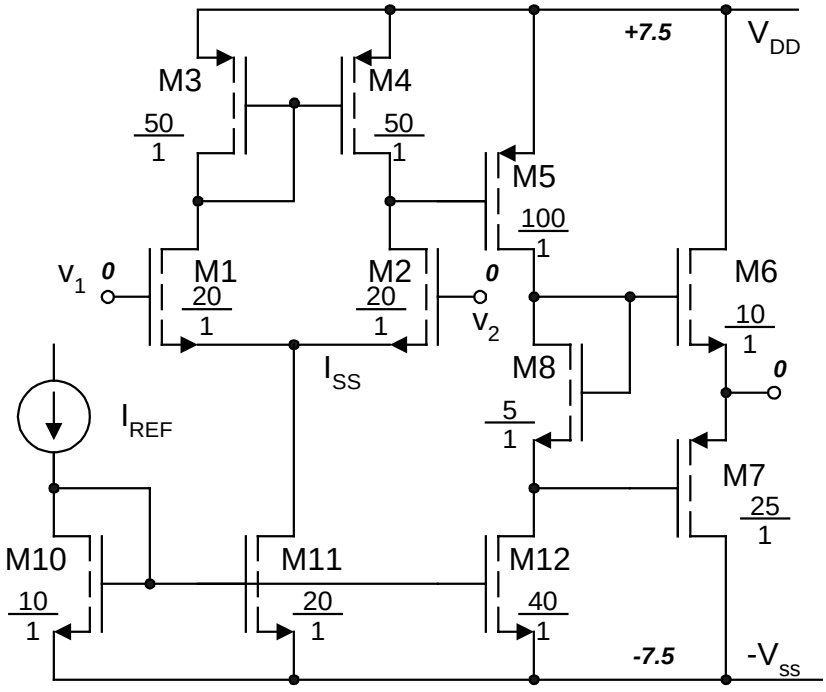

Fig. 10 Simple operational amplifier

Solution

(a) Find the biasing currents first. By circuit inspection one may find that:
$I_{D11}=0.5mA;\ I_{D12}=1mA;\ I_{D1}=0.25mA;\ I_{D2}=0.25mA;\ I_{D1}=0.25mA;\ I_{D6}=I_{D7}=330\mu A$
Note that at this point effect of channel length modulation was ignored.
(b) Find small signal transistor parameters. Using (6) one may find that

$$r_m=\frac{1}{\sqrt{2K,\frac{W}{L}I_D}} \qquad r_o=\frac{1}{\lambda I_D}$$

Note that an approximate formula without V_{DS} was used and the small signal parameters are calculated only when required.
$r_{o1}=r_{o2}=235k\Omega;\ r_{o3}=r_{o4}=235k\Omega;\ r_{o5}=58.7k\Omega;\ r_{o12}=58.7k\Omega;$
$r_{m1}=r_{m2}=2\text{k}\Omega;\ r_{m5}=0.707\text{k}\Omega;$
(c) Gain calculation. For the differential stage there are two signal paths M1,M3, M4 and M1,M2.
In the first path M1 can be considered as CS configuration (9) and M3 and M4 as a current mirror

$$A_{11}=\frac{r_{o2}\,||\,r_{o4}}{r_{m1}+r_{m2}}=29.375;$$

In the second path there are two stages: M1 can be considered as CD configuration (7) and M2 as CG configuration (11).

$$A_{12}=\frac{r_{m2}}{r_{m1}+r_{m2}}\frac{r_{o2}\,||\,r_{o4}}{r_{m2}}=29.375;$$

Using the concept of superposition the total gain of the first stage is $A_1=A_{11}+A_{12}=58$
The gain of the second stage composed of transistors M5 and M12 is (9)

$$A_2=\frac{r_{o12}\,||\,r_{o5}}{r_{m5}}=41.51$$

The last stage composed of M6 and M7 works as a voltage follower and has gain $A_3\approx 1$. For accurate calculation a value of load resistance must be specified. The total gain is $A_1\,A_2\,A_3$=2,439 V/V

IV. Conclusion

For small signal analysis we usually have to calculate input and output resistance and gain (seldom input or output conductance). Therefore, it is more natural to use r_m instead of g_m. Note that with the presented approach (use r_m instead of g_m) the gain of amplifiers is expressed as a ratio of resistances instead of the commonly used formulas with g_m.

For the common emitter/source the gain is the ratio of two resistances

$$A_V = \frac{R_L}{r_m + R_S} \qquad \text{instead of} \qquad A_V = \frac{g_m R_L}{1 + g_m R_S}$$

When transistor is driven by source with resistance R_{IN} than

$$A_V = \frac{R_L}{r_m + R_S + \frac{R_{IN}}{\beta}} \qquad \text{instead of} \qquad A_V = \frac{g_m R_L}{1 + g_m R_S + g_m \frac{R_{IN}}{\beta}}$$

For common collector/drain configuration I would rather see a resistor divider

$$A_V = \frac{R_S}{r_m + R_S} \qquad \text{instead of} \qquad A_V = \frac{g_m R_S}{1 + g_m R_S}$$

All equations for frequency responses seems to be more complicated if g_m is used instead r_m

With this approach students are able to find the proper solution for basic single stage amplifiers within a couple of minutes [5][6]. For example, most of them are able to analyze 20 different circuits during a 50 minute exam. The described method has an even more significant advantage during the design of analog integrated circuits such as OPAMP. More importantly the students are able to read diagrams and to understand the effect of each element change on the circuit performance. Students are not lost with messy equations, but they are in control of their design and they know which parameters they have to change in order to change behavioral characteristics. With limited space of this presentation only MOS examples were used, but circuits with bipolar transistors can be analyzed in a similar way.

Bibliography

1. Jaeger, R, *Microelectronic Circuit Design*, McGraw Hill 1997
2. Sedra S. S. and K. C. Smith, *Microelectronic Circuits*, Oxford University Press 1998, 4-th edition.
3. Johns D. A. and K. Martin, *Analog Integrated Circuit Design*, JohnWiley & Sons 1997
4. Neamen D. *Electronic Circuit Analysis and Design*, Irwin 1996
5. http://nn.uwyo.edu/ee3310/../../DYDA/98S3310/HWBIP.doc
6. http://nn.uwyo.edu/ee3310/../..//DYDA/98S3310/HWFET.doc

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