High Speed, High Voltage, and Energy Efficient Static Induction Devices

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Abstract

Several devices from the static induction family such as: Static Induction Transistor (SIT), Static Induction Diode (SID), Static Induction Thyristor, Lateral Punch-Through Transistor (LPTT), Static Induction Transistor Logic (SITL), Static Induction MOS Transistor (SIMOS), and Space Charge Limiting Load (SCLL) are described. The theory of operation of static induction devices is given for both a current controlled by a potential barrier and a current controlled by space charge. The new concept of a Punch-Through Emitter (PTE), which operates with majority carrier transport, is presented. It is shown that by using the PTE it is possible to design fast, high power diodes with breakdown voltages above 1000V while the forward voltage drop can be on the order of 0.15V.

Introduction

Static induction devices were invented by J. Nishizawa [6]. The idea was so innovative that the current establishment in the solid state electronics community had difficulty understanding and accepting this discovery. The IEEE Transactions on Electron Devices the leading IEEE periodical had difficulty finding proper reviewers and as a result the reviewing process continued for years.

Japan was the only country where static induction family devices were successfully fabricated [14]. The number of devices in this family is growing with time. The static induction transistors can operate with power of 100kW at 100kHz or 10W at 10GHz. Static induction transistor logic had 100 time smaller switching energy than its I^2L competitor[8][9]. Static induction thyristor has many advantages over the traditional SCR, and Static induction diode exhibits high switching speed, large reverse voltage and low forward voltage drops.

Theory of Static Induction Devices

The derivations of formulas will be done for a n-channel device, but the obtained results, with a little modification can be also applied to p-channel devices. An induced electrostatically potential barrier controls the current in static induction devices. For a small electrical field existing in the vicinity of the potential barrier the drift and diffusion current can be approximated by

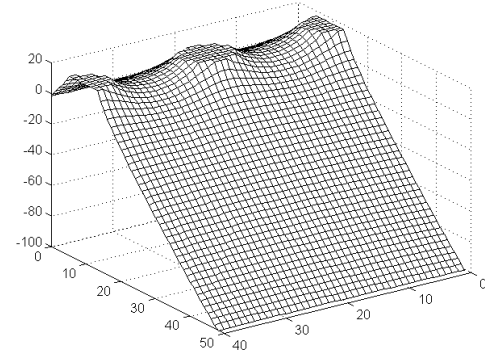$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx} \qquad (1)$$

where $D_n = \mu_n V_T$ and $V_T = \frac{kT}{q}$. By multiplying both sides of the equation by $\exp\left(-\frac{\varphi(x)}{V_T}\right)$ and rearranging

$$J_n \exp\left(-\frac{\varphi(x)}{V_T}\right) = qD_n \frac{d}{dx}\left[n(x)\exp\left(-\frac{\varphi(x)}{V_T}\right)\right] \qquad (2)$$
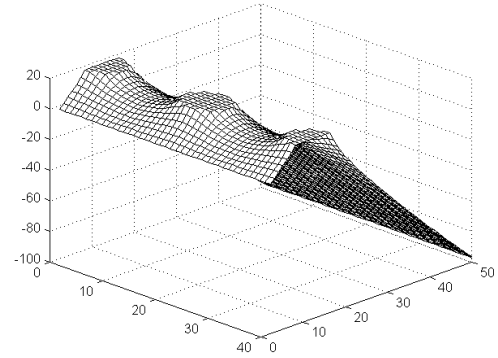
(a)

(b)

Fig. 1. Potential distribution in SIT (a) view from the source side and (b) view from the drain side.

Integrating from x_1 to x_2 one can obtain

$$J_n = qD_n \frac{n(x_2)\exp\left(-\frac{\varphi(x_2)}{V_T}\right) - n(x_1)\exp\left(-\frac{\varphi(x_1)}{V_T}\right)}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right)dx} \qquad (3)$$

With the following boundary conditions

$$\varphi(x_1) = 0; \quad n(x_1) = N_S;$$
$$\varphi(x_2) = V_D; \quad n(x_2) = N_D; \qquad (4)$$

equation (3) reduces to

$$J_n = \frac{qD_nN_S}{\int_{x_1}^{x_2}\exp\left(-\frac{\varphi(x)}{V_T}\right)dx} \tag{5}$$

Note that the above equations derived for SIT can be also used to find current in any devices controlled by a potential barrier, such as a bipolar transistor, MOS transistor operation in subthreshold mode, or in a Schottky diode.

Samples of the potential distribution in SI devices are shown in Fig. 3 [1][20]. The vicinity of the potential barrier were approximated by Plotka [11][12] using parabolic formulas (Fig. 2) along and across the channel.

$$\varphi(x) = \Phi\left[1 - \left(2\frac{x}{L} - 1\right)^2\right] \tag{6}$$

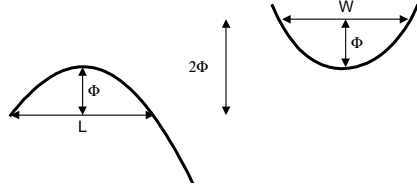$$\varphi(y) = \Phi\left[1 - \left(2\frac{y}{W} - 1\right)^2\right] \tag{7}$$

Fig. 2. Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

Integrating (5) first along the channel and then across the channel, yields a very simple formula for drain currents in p-channel SIT transistors

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(\frac{-\Phi}{V_T}\right) \tag{8}$$

where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, W/L ratio describes the shape of the potential saddle in vicinity of the barrier, and Z is the length of the source strip.

Since barrier height Φ can be a linear function of gate and drain voltages, therefore

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(-\frac{a(V_{GS} + bV_{DS} + \Phi_0)}{V_T}\right) \tag{9}$$

For large current levels the device current is controlled by the space charge of moving carriers. In the one-dimensional case the potential distribution is described by the Poisson equation:

$$\frac{d^2\varphi}{dx_2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{I_{DS}}{A\,v(x)} \tag{10}$$

Where A is the effective device cross section and $v(x)$ is carrier velocity. For a small electrical field $v(x) = \mu E(x)$

$$I_{DS} = \frac{9}{8}V_{DS}^2\mu\varepsilon_{Si}\varepsilon_0\frac{A}{L^3} \tag{11}$$

and for a large electrical field $v(x) = const$

$$I_{DS} = 2V_{DS}v_{sat}\varepsilon_{Si}\varepsilon_0\frac{A}{L^2} \tag{12}$$

where L is the channel length and $v_{sat} \approx 10^{11}\mu$m/s is the carrier saturation velocity. In practical devices the current-voltage relationship is described by an exponential relationship (12) for small currents, a quadratic relationship (14), and finally for large voltages by an almost linear relationship (15).
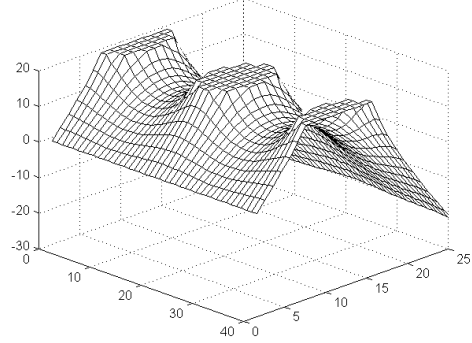
(a)
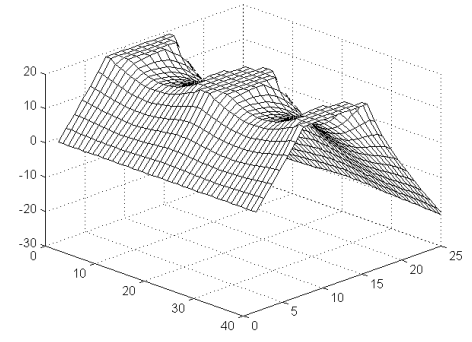
(b)

Fig. 3. Potential distributions in SIT (a) traditional and (b) with sharp potential barrier.

Static Induction Transistor (SIT)

One of the disadvantages of SIT is the relatively flat shape of the potential barrier (Fig. 3(a)). This leads to slow, diffusion based transport of carriers in the vicinity of the potential barrier. The carrier transit time can be estimated using the formula:

$$t_{transit} = \frac{l_{eff}^2}{D} \tag{13}$$

where l_{eff} is the effective length of the channel and $D = \mu V_T$ is the diffusion constant. In the case of a traditional SIT transistor this channel length is about 2μm while in the case of SIT transistors with sharper barriers (Fig. 3(b)) the channel length is reduced to about 0.2 μm. The corresponding transient times are 2ns and 20ps respectively.

Punch-Through Emitter

There are two well known emitters: (1) *p-n* junction (Fig. 4(a)) and (2) Schottky junction (Fig. 4(b)). For silicon devices *p-n* junctions have a forward voltage drop of 0.7-0.8 volts while Schottky emitters have 0.2-0.3 V only. Since the Schottky diode is a majority carrier device, the carrier storage effect is negligible.

Another interesting emitter structure is shown in Fig. 4(c). This emitter has all the advantages of the Schottky diode even though it is fabricated out of p-n junctions.
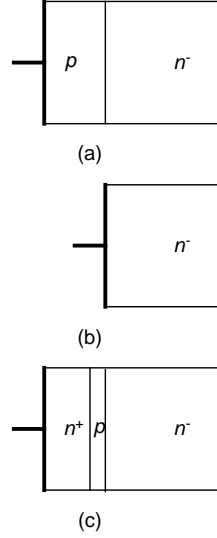

(a)

(b)

(c)

Fig. 4. Various structures of emitters: (a) *p-n* junction including heterostructure with SiGe materials, (b) Schottky junction, (c) punch-through emitter (in normal operation condition the p region is depleted from carriers).

The concept of static induction devices can be used independently of the type of emitter shown in Fig. 4. This way the quality of each emitter can be further enhanced by the static induction effect as shown in Fig. 5.

Bipolar Mode Operation of SI devices (BSIT)

The bipolar mode of operation of SIT was first reported in 1976 by Nishizawa and Wilamowski [8][9]. Several complex theories for the bipolar mode of operation were developed [2][5][6][10][23][24], but actually the simple formula (5) works well not only for the typical mode of SIT operation, but also for the bipolar mode of SIT operation. Furthermore, the same formula works very well for classical bipolar transistors.

For example, in the case of *npn* bipolar transistors the potential distribution across the base in reference to emitter potential at the reference impurity level $N_E=N_S$ is described by

$$\varphi(x) = V_T \ln\left(\frac{N_B(x)N_S}{n_i^2} \right) - V_{BE} \qquad (14)$$

After inserting (14) into (5) one can obtain the well-known equation for electron current injected into the base

$$J_n = \frac{qD_n n_i^2}{\displaystyle\int_{x_1}^{x_2} N_B(x)dx} \exp\left(\frac{V_{BE}}{V_T} \right) \qquad (15)$$

If equation (5) is valid for SIT and BJT then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor.

Static Induction Diode (SID)

The bipolar mode of operation of SIT can be also used to obtain diodes with low forward voltage drop and negligible carrier storage effect [2][5][13][23][24]. A static induction diode can be obtained by shorting a gate to the emitter of the static induction transistor. Such diode has all the advantages of the static induction transistor such as thermal stability, and short switching time. The cross section of such diode is shown in Fig. 5.
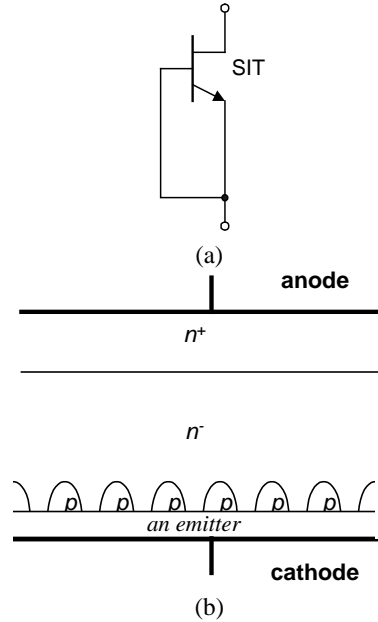

(a)

(b)

Fig. 5. Static Induction Diode: (a) circuit diagram and (b) cross section

The quality of the static induction diode can be further improved with more sophisticated emitters (Fig. 4(b) and 4(c)). The SI diode with Schottky emitter was described by Wilamowski in 1983 [17] (Fig. 6). An improved structure was later published by Baliga [1].

(a)

cathode

p   p   p   p   p

n^-

(b) n^+

anode

cathode

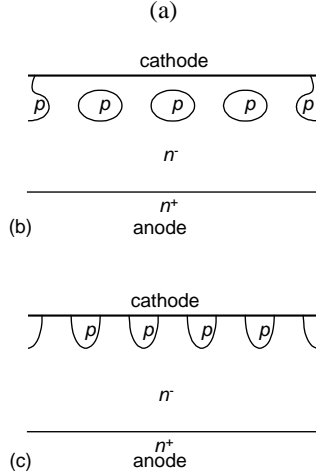p   p   p   p

n^-

(c) n^+

anode
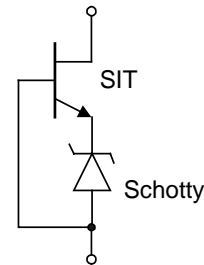
Fig. 6. Schottky diode with enlarged breakdown voltages: (a) circuit diagram, (b) and (c) two cross section of possible implementation
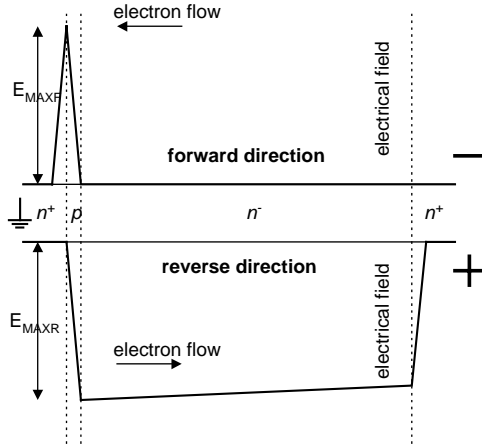

Fig. 7. Electrical field distribution in $n^+pn^-n^+$ diode for forward and reverse directions

$n^+pn^-n^+$ Diode

If the punch-through emitter is used (Fig. 4(c)) then a very interesting diode can be developed. Fig. 7 shows the electrical field distribution for forward and reverse directions using step junction approximation. The voltage drop on the device is proportional to the area under the curve and the ratio between forward and reverse directions can be very large. Let us assume the impurity concentration in p layer $N_A=10^{18}$; thickness of n^- layer $=100\mu m$, thickness of p layer $0.01\mu m$. The peak electrical field can be found as

$$E_{MAX} = \frac{qNx}{\varepsilon_{Si}\varepsilon_0} = \frac{1.6E-19 \cdot 1E18 \cdot 1E-6}{12 \cdot 8.86E-14} = 1.5E5\frac{V}{cm} = 15\frac{V}{\mu m}$$

and the forward and reverse voltages are

$$V_{FORWARD} \approx \frac{E_{MAX}\left(x_p + x_{n^+}\right)}{2} \approx 0.15\,V$$

$$V_{REVERSE} \approx E_{MAX}\,x_{n^-} = 1500\,V$$

If the p-layer has a uniform impurity distribution then E_{MAXF} and E_{MAXR} are equal. When, instead of the constant doping profile in the p region, the nonuniform doping is used then the value E_{MAXR} can be much larger than E_{MAXF}.

Another advantage of the $n^+pn^-n^+$ diode is the very fast switching time because this is basically a device with majority carrier transport. Since the current flow in both directions is controlled by a potential barrier in both directions, the current voltage characteristics can be described by equations (5) and (8).

Lateral Punch-Through Transistor (LPTT)

Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch through transistor, which operates on the same principle and has similar characteristics [15]. The cross section of the LPTT is shown in Fig. 8.
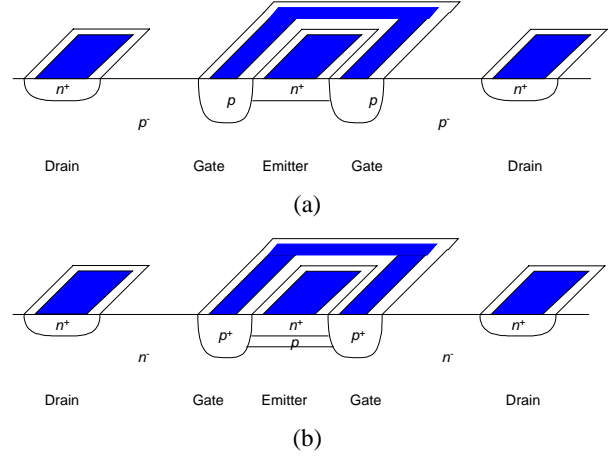

(a)

(b)

Fig. 8. Several structures of the lateral punch-through transistors: (a) simple and (b) with sharper potential barrier.
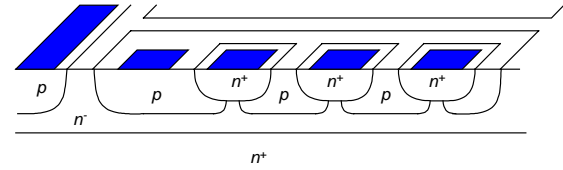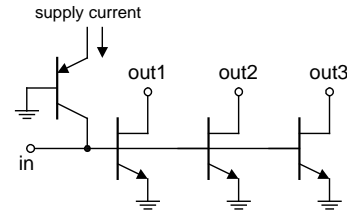

Fig. 9. Cross-section of SIT logic

Fig. 10. Diagrams of SIT logic

Static Induction Transistor Logic (SITL)

The SITL was proposed by Nishizawa and Wilamowski [8][9]. This logic circuit has almost 100

times better power-delay product than its I^2L competitor. Such drastic improvement of the power-delay product is possible because the SITL structure has significantly smaller junction parasitic capacitance and also the voltage swing was reduced by half. Fig. 9 and 10 illustrate the concept of SITL.

BJT Saturation Protected by SIT

The SI transistor can be also used instead of a Schottky diode to protect a bipolar junction transistor against saturation[20]. The concept is shown in Fig. 11 and 12.
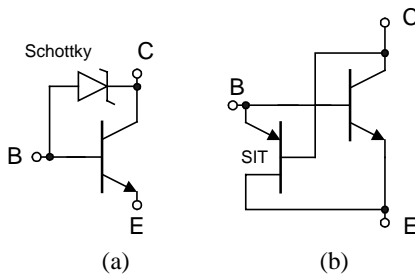

(a)   (b)

Fig. 11. Protection of bipolar transistor against deep saturation (a) using Schottky diode, and (b) using SIT.
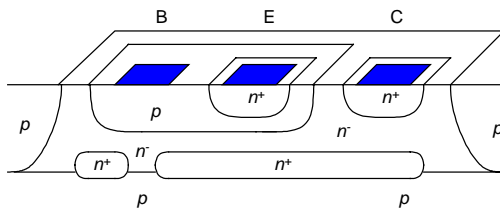

Fig. 12. Cross sections of bipolar transistors protected against deep saturation using SIT.
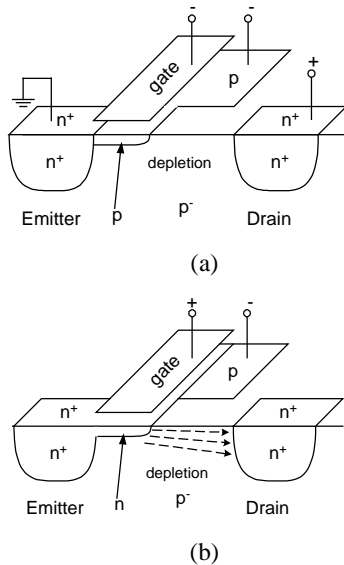

(a)

(b)

Fig. 13. MOS controlled punch-through transistor (a) transistor in the off state for the negative gate potential and (b) transistor in the on state for the positive gate potential.

Static Induction MOS Transistor (SIMOS)

The punch-through transistor with MOS Controlled Gate was described in 1983 [18][19]. In the structure in Fig. 13(a) current can flow in a similar fashion as in the lateral punch-through transistor[15]. In this mode of operation, carriers are moving far from the surface with a velocity close to the saturation velocity. The real advantage of such structure is the very low gate capacitance.
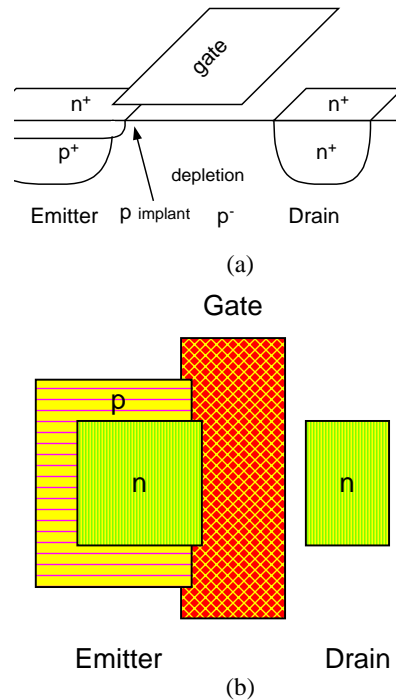

(a)

(b)

Fig. 14. Static Induction MOS structure (a) cross section and (b) top view

Another interesting structure is shown in Fig. 14. The buried p^+ layer is connected to the substrate, which has a large negative potential. As a result the potential barrier is high and the emitter-drain current cannot flow. The punch through current may start to flow when the positive voltage is applied to the gate and in this way the potential barrier is lowered. The p-implant layer is depleted and due to the high horizontal electrical field under the gate there is no charge accumulation under this gate. Such a transistor has several advantages over the traditional MOS transistor.
(1) The gate capacitance is very small, since there is no accumulation layer under the gate.
(2) Carriers are moving with a velocity close to saturation velocity.
(3) Much lower substrate doping and the existing depletion layer lead to much smaller drain capacitance.
The device operates in a similar fashion as MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such "bipolar mode"

of operation may have many advantages in VLSI applications.

Space Charge Limiting Load (SCLL)

Using the concept of the space-charge limited current flow (Eqs. (11) and (12)) it is possible to fabricate very large resistors on a very small area. Moreover these resistors have a very small parasitic capacitance. The $50k\Omega$ resistor requires only several square μm using 2μm technology [22].
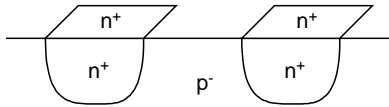

Fig. 16. Space Charge Limiting Load (SCLL)

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