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Technical Report No.25/99

WYDZIAŁ ELEKTRONIKI
TELEKOMUNIKACJI I INFORMATYKI

FACULTY OF ELECTRONICS
TELECOMMUNICATIONS AND INFORMATICS

G. Narutowicza 11/12, 80-952 Gdańsk, Poland

Politechnika Gdańska
Wydział Elektroniki, Telekomunikacji i Informatyki

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W znanych z literatury przedmiotu modelach pracy tranzystora MOSFET można zauważyć szereg istotnych błędów metodologicznych i wad wywołujących liczne trudności w próbach zastosowania tych modeli do praktyki inżynierskiej. Istniejące modele matematyczne tranzystora MOS mają wąski zakres stosowalności, charakteryzują się małą dokładnością opisu ilościowego pracy tranzystora, nie spełniają tzw. testu symetryczności zaproponowanego przez Gummela, nie odzwierciedlają odwrotnych efektów krótkokanałowych oraz występują w nich nierealistyczne pojęcia, takie jak odcięcie kanału i skracanie kanału.

W prezentowanym raporcie przedstawiano i zweryfikowano empirycznie nowy model zunifikowany tranzystora MOS, który nie ma wyżej wspomnianych wad. Model ten został wyprowadzony, min. na podstawie równania określającego wielkości ładunków w tranzystorze będącym w stanie nierównowagi.
Jedna formuła matematyczna opisuje pracę tranzystora MOS zarówno w zakresie przed - jak i nadprogowym i jest słuszne dla tranzystorów o dowolnej długości kanału.

An Analytical DC MOSFET Model Based on an Equation for Charges in Non-Equilibrium State

W. Kordalski
Faculty of Electronics, Tech. Univ. of Gdańsk, Gdańsk, Poland
kord@ue.eti.pg.gda.pl

S. Kozieł
Faculty of Electronics, Tech. Univ. of Gdańsk, Gdańsk, Poland
koziel@ue.eti.pg.gda.pl

B.M. Wilamowski
Dept. Of Electr. Eng., Univ. of Wyoming, Laramie, USA
wilam@uwyo.edu

Abstract

A new, fully analytical, physics-oriented, single-equation dc model for CMOS transistors with arbitrarily doped substrate and its experimental verification are presented. The model is valid for sub- and above threshold region of operation, satisfies the Gummel symmetry test, reflects reverse short-channel effect (RSCE), and equally well describes current-voltage characteristics of the transistors with both split and not split curves in the subthreshold region. Here presented model is valid for MOSFETs with any long channel, including sub-0.1-μm devices.

1. Introduction

The Gradual Channel Approximation (GCA), commonly used in analytical MOSFET modelling, amounts to the assumption that surface density of free carriers at any point in the transistor channel is defined by the transversal electric field acting on the semiconductor surface at the point. As a result, the use of GCA precludes derivation of any single-equation MOSFET model whose validity would be true for the entire range of biasing voltage variations.

In this work, we propose a new analytical, physically consistent, single-equation dc model of the enhancement-mode, arbitrarily doped MOSFET. The model is based on an equation for charges in non-equilibrium case, which was derived in [4].

2. An equation for charges

Let us consider an enhancement-mode MOSFET being in non-equilibrium state whose cross section is depicted in Fig.1.

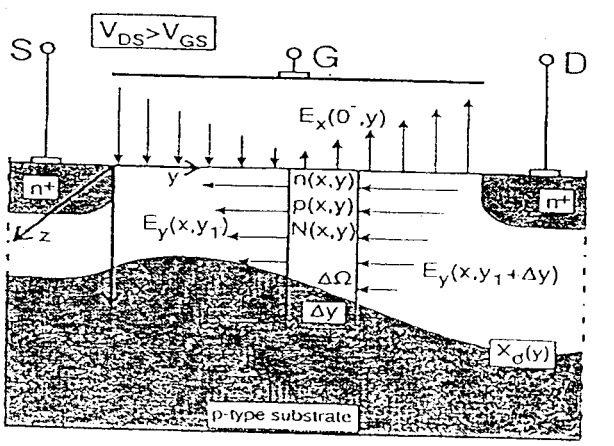

Figure 1. A MOSFET view

An electrically neutral part of the p-type semiconductor substrate is separated from the channel and depletion region of the transistor by a surface represented by $X_d(y)$.

Applying Gauss law to an element of volume $\Delta\Omega$ and using analysis as in [4] yields the following basic equation for charges in the MOSFET being in non-equilibrium case:

$$Q_s(y) = -\varepsilon_0\varepsilon_{ox}E_x(0^-,y) + \varepsilon_0\varepsilon_s\int_0^{X_d(y)}\frac{\partial E_y(x,y)}{\partial y}dx + \\ + \varepsilon_0\varepsilon_s\frac{dX_d(y)}{dy}E_y(X_d(y),y) \qquad (1)$$

where

$$Q_s(y) = q\int_0^{X_d(y)}\left[p(x,y) - n(x,y) - N(x,y)\right]dx$$

is the total surface charge density of ionised dopants N(x,y), electrons n(x,y) and holes p(x,y) in the depletion region.

Equation (1) states that for any point $y\in[0,L]$, L being the channel length, $Q_s(y)$ is determined not only by the transversal gate electric field but also by two terms depending, respectively, on divergence of the longitudinal electric field component and the rate of change of function $X_d(y)$ describing the shape of the depletion region. Eqn. (1) is valid in all regions of MOSFET operation: subthreshold, above threshold and breakdown.

3. Basic equation of the model

For the sake of brevity, the detailed derivation of the model will be given elsewhere. Here, we present the basic equation for the drain current of the enhancement-mode CMOS transistors with arbitrarily doped substrate:

$$I_D = \frac{\mu E_C BMWQ_{ch}V_{DS}}{LE_{Cef} + B|V_{DS}|} \qquad (2)$$

where, the channel charge Q_{ch} takes the form:

$$Q_{ch} = 2C_{ox}\gamma_1\ln\left\{1+\exp\left[|V_{GS}-V_T|(2\gamma_1)^{-1}\right]\right\}\times \\ \times\frac{1+\gamma_5|V_{GS}|\exp(-\gamma_6|V_{GS}|)}{1+2\gamma_1[\gamma_2+\gamma_3\exp(\gamma_4|V_{GS}|)]\exp\left[-\frac{|V_{GS}-V_T|}{2\gamma_1}\right]}$$

and

$$E_{Cef} = E_C(\beta + \alpha C_{ox}|V_{GS}|),$$

$$M = 1 + a|V_{DS}|\exp(-b|V_{GS}|)\cdot(1+c|V_{DS}|)^{-1},$$

$$B = \exp(H|V_{DS}|)\cdot(1+fH|V_{DS}|)^{-1},$$

$$H = h\exp(-k|V_{GS}|) + (m + r|V_{DS}|V_{GS}^2)^{-1}$$

with W, L, μ, C_{ox}, and V_T being, respectively, the channel length, the effective low-field mobility, the gate oxide capacitance per unit area, and the threshold voltage. The others symbols are parameters of the model. The sign of I_D is determined by the sign of the drain-source voltage V_{DS} occurring in the numerator of eqn. (2).

4. Conclusion

Some results of experimental verification of the model we have developed are presented in Figures 2 to 12.

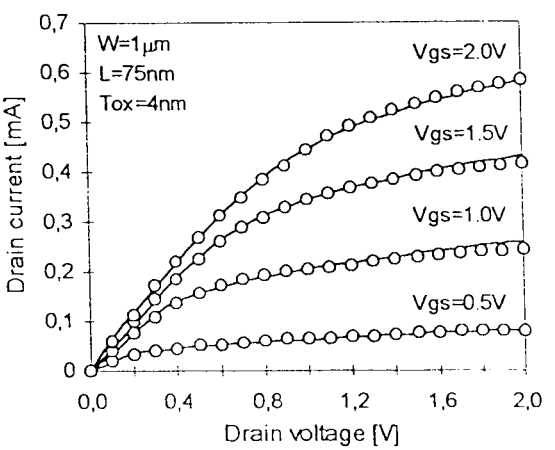

Figure 2. A PMOS, L=75nm [5]

The measured data for 75-nm channel-length transistor (Fig.2) and 0.6-μm devices (Figs.3 and 4) are taken from [1] and [2], respectively. Agreement between measured (circles) and theoretical characteristics (lines) as well as versatility

of the model can be seen from Figs. 2 to 12. Unlike the BSIM3v3 model [3] the one satisfies the Gummel symmetry test [5], comprises distinctly less parameters, is free from shortening channel effect, shows correct asymptotic behaviour, and is defined by one equation. There are no physical inconsistencies in the model.

The model is very useful for circuit analysis and simulation purposes. The model can be applied for CMOS transistors with any long channel down to sub-0.1μm.

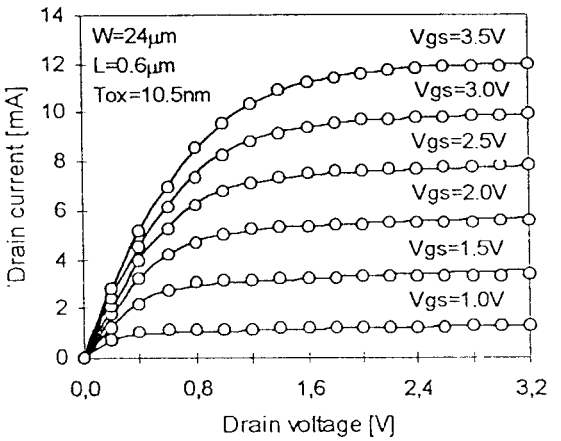

Figure 3. An NMOS, L=0.6μm [4]

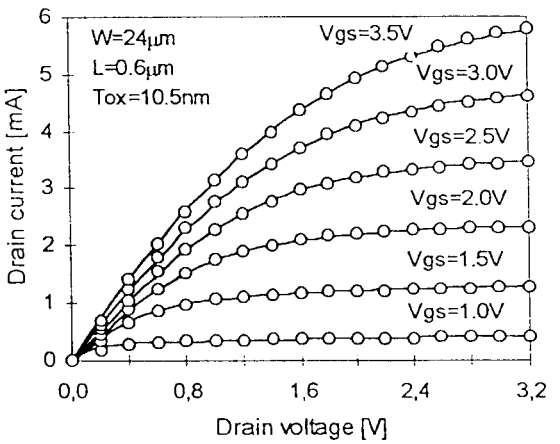

Figure 4. A PMOS, L=0.6μm [4]

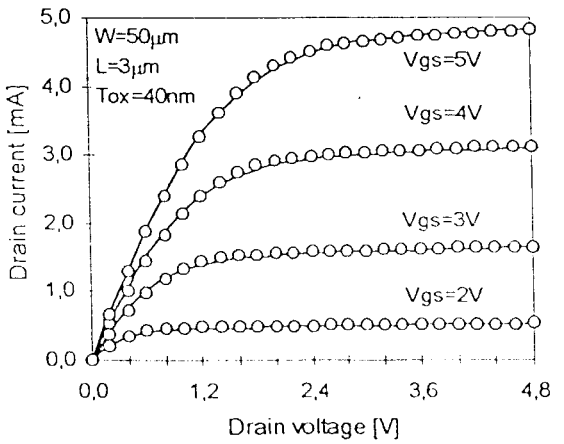

Figure 5. An NMOS, L=3μm (MOSIS)

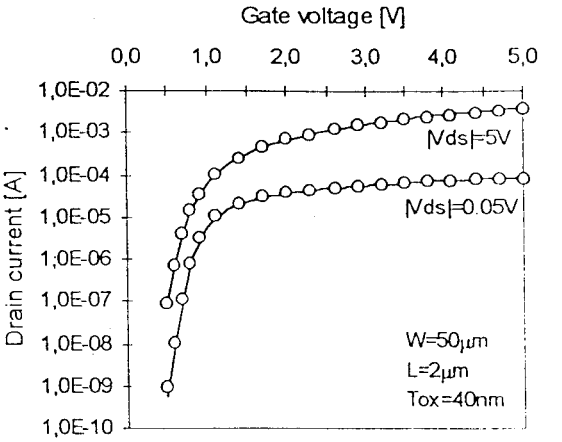

Figure 6. A PMOS, $|g|_D$ vs. V_{GS}, L=2μm

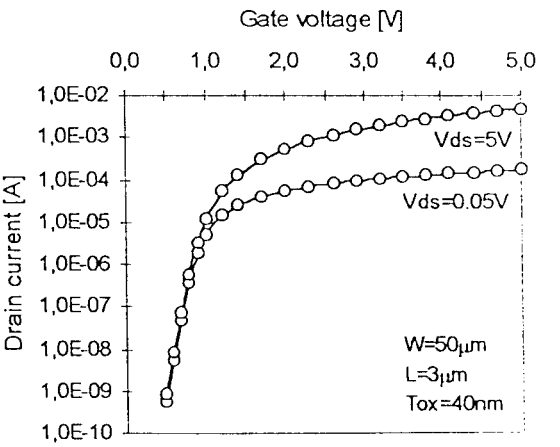

Figure 7. An NMOS, $|g|_D$ vs. V_{GS}

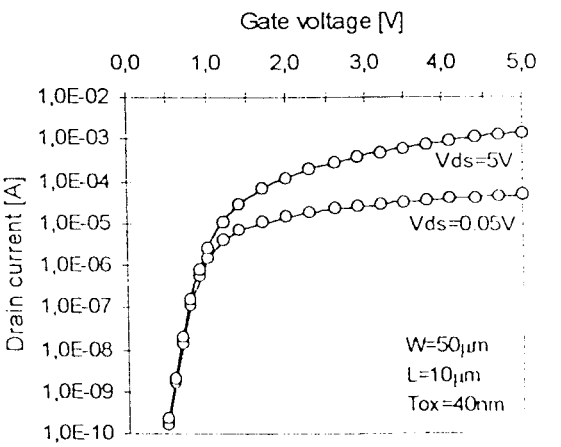

Figure 8. An NMOS, $|g|_D$ vs. V_{GS}

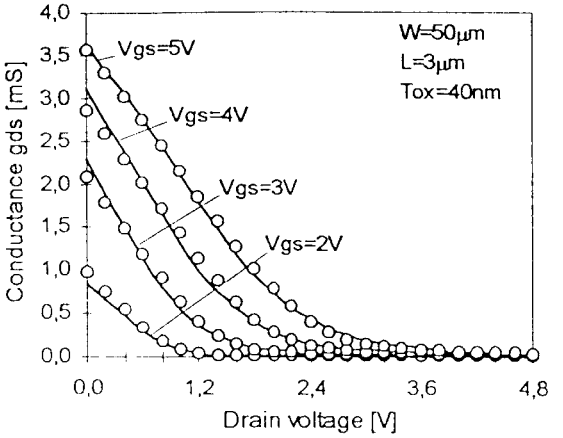

Figure 9. An NMOS, g_{ds} vs. V_{DS}, L=3μm.

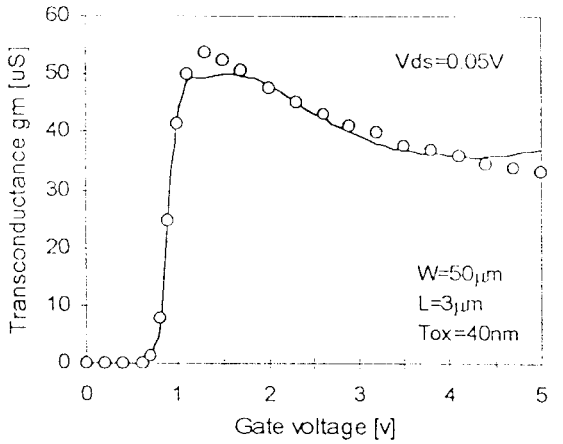

Figure 10. An NMOS, g_m vs. V_{GS}, L=3μm, V_{DS}=0.05V

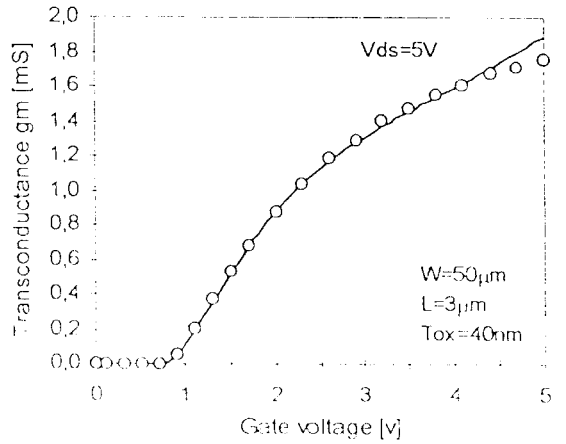

Figure 11. An NMOS, g_m vs. V_{GS}, L=3μm, V_{DS}=5V

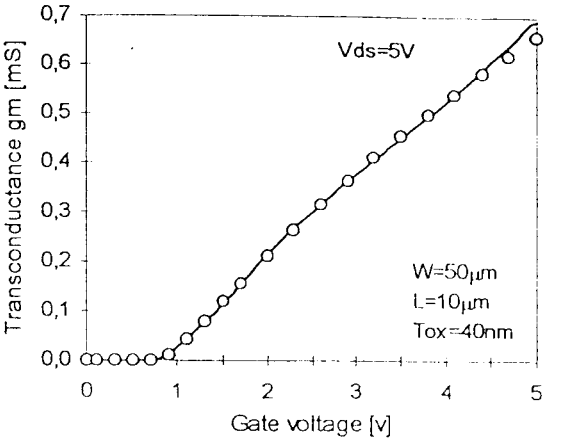

Figure 12. An NMOS, g_m vs. V_{GS}, L=10μm, V_{DS}=5V

5. References

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[4] W. Kordalski, „Two-Dimensional Effects in the MOSFET", Proc. of the 19th National Conference on Circuit Theory and Electronic Networks, Kraków-Krynica, Poland, Oct. 1996, pp.239-244.

[5] K. Joardar et al., „An Improved MOSFET Model for Circuit Simulation", *IEEE Trans. on Electron Devices*, Vol.45, No 1, 1998, pp.134-148.