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A Scalable I-V MOSFET Model for Analog/Digital Circuit Simulation

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ABSTRACT

A new, fully analytical, physics-oriented, single-equation, scalable dc model for CMOS transistors with arbitrarily doped substrate and its experimental verification are presented. The model describes current-voltage characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions with a single I-V equation, and guarantees the continuities of I_{DS}, differential conductance g_{ds} and transconductances throughout all V_{GS}, V_{DS}, and V_{BS} bias conditions. Unlike the BSIM3v3 model [1], implemented in HSPICE and other circuit simulators, the one satisfies the Gummel symmetry test, and reflects reverse short-channel effect (RSCE). Scalability of the model is demonstrated on the basis of measured characteristics of CMOSFETs fabricated in MOSIS technology.

Keywords: MOSFET models, MOSFET scaling, VLSI circuit design.

1. INTRODUCTION

As the development of MOS VLSI technology progresses, the circuit designers need analytical models for advanced MOSFETs for use them in circuit simulators such as SPICE. The continuity, accuracy, scalability and simulation performance are basic requirements for a MOSFET model to meet the needs of analog and mixed analog/digital circuit designs.

Although many models for MOSFETs have been published in the literature over the years, most of these models have drawbacks stemming from simplifying assumptions made during their development. For instance, the BSIM3v3 model from Berkeley (implemented in Spectre, Hspice, SmartSpice, Spice 3e2, etc.), the MM9 model from Philips, the PCIM model from DEC, and the EKV model developed by Enz *et al.* do not satisfy the Gummel symmetry test and attain poor accuracy in specific regions of device operation [2]. Some smoothing functions are used at the boundary between the linear and saturation regions or at the boundary between weak and strong inversion conditions in these models.

Furthermore, existing models do not explain either qualitatively or quantitatively the splitting of current-voltage characteristics of some transistors operating in the subthreshhold region (weak inversion). They also do not account for anomalous subthreshold characteristics of the MOSFET, reported in [3]. Thus, in some cases, these deficiencies of known models strongly affect exactness of simulation results. A better MOSFET model is therefore required that overcomes the problems mentioned above. What is more, as a result of continuous reduction of the channel length, new scaling methodologies are of great importance. Known scaling procedures such as constant-field scaling, constant-voltage scaling, quasi-constant-voltage scaling or generalised scaling are only useful as a straightforward guide [4]. So, to allow users to accurately model CMOS circuits over a wide range of channel lengths a scalable technology-oriented MOSFET model of sufficiently close accuracy is needed.

In work [5], we have proposed a new, fully analytical, physics-oriented, single-equation dc model of the MOSFET with arbitrarily doped substrate as well as its experimental verification. The model is valid for sub- and above threshold region of operation, satisfies the Gummel symmetry test, reflects reverse short-channel effect, and equally well describes I-V characteristics of CMOS transistors with both split and not split curves in the subthreshold region. Validity of the model has been experimentally confirmed for PMOS and NMOS transistors with any long channel, including sub-0.1-μm. devices. However, to appraise usefulness of the model for optimisation and integrated circuit design purposes we have developed a scaling procedure and derived semi-empirical relationships between the channel length and the model parameters. Some parameters of the model have been already scaled and reported in [6].

In this work, we present the model [4] along with completed scaling procedure and results of experimental verification of scalability of the model.

2. THE CHANNEL-LENGTH INDEPENDENT MODEL

The overall current equation of the model for the linear and saturation region and for weak and strong inversion can be described by the following single equation [5]:

$$I_D = \frac{\mu E_C B M W Q_{ch} V_{DS}}{L E_{Cef} + B|V_{DS}|} \tag{1}$$

where, Q_{ch} takes the form:

$$Q_{ch} = \frac{2C_{ox}\gamma_1 \ln\left\{1+\exp\left[|V_{GS}-V_T|(2\gamma_1)^{-1}\right]\right\}\cdot\left[1+\gamma_5|V_{GS}|\exp\left(-\gamma_6|V_{GS}|\right)\right]}{1+2\gamma_1\left[\gamma_2+\gamma_3\exp(\gamma_4|V_{GS}|)\right]\exp\left[-|V_{GS}-V_T|(2\gamma_1)^{-1}\right]}$$

and

$$E_{Cef} = E_C\left(\beta+\alpha C_{ox}|V_{GS}|\right), \qquad M = 1+a|V_{DS}|\exp\left(-b|V_{GS}|\right)\cdot\left(1+c|V_{DS}|\right)^{-1},$$

$$B = \exp\left(H|V_{DS}|\right)\cdot\left(1+fH|V_{DS}|\right)^{-1}, \qquad H = h\exp\left(-k|V_{GS}|\right)+\left(m+r|V_{DS}|V_{GS}^2\right)^{-1},$$

with W, L, μ, C_{ox}, and V_T being, respectively, the channel length, the effective low-field mobility, the gate oxide capacitance per unit area, and the threshold voltage. The others symbols are parameters of the model. The sign of I_D is determined by the sign of the drain-source voltage V_{DS} occurring in the numerator of eqn. (1).

To be able to model the electrical characteristics of MOSFETs over a wide range of the channel length it is necessary to make some of the parameters dependent on the channel length. In work [6], we have scaled the following parameters:

$$\mu(L) = \mu_1\exp(-\mu_2 L), \qquad \alpha(L) = (\alpha_1+\alpha_2 L)\ln(\alpha_3 L),$$

$$E_c(L) = E_1\exp(-E_2 L), \qquad V_T(L) = \sqrt{t_1+t_2 L}, \tag{2}$$

$$a(L) = a_1\exp(-a_2 L), \qquad b(L) = b_1+b_2 L,$$

and in this paper we propose a scaling procedure for other parameters as follows:

$$\gamma_1(L) = \gamma_{11}+\gamma_{12}L+\gamma_{13}\exp\left(\gamma_{14}L\right), \qquad \gamma_2(L) = \gamma_{21}+\gamma_{22}\exp\left(\gamma_{23}L\right),$$

$$\gamma_3(L) = \gamma_{31}+\frac{\gamma_{32}}{L}+\gamma_{33}\exp\left(\gamma_{34}L\right), \qquad \gamma_4(L) = \gamma_{41}+\frac{\gamma_{42}}{L^2}+\gamma_{43}\frac{\exp\left(\gamma_{44}L\right)}{L}, \tag{3}$$

$$\gamma_5(L) = \gamma_{51}+\gamma_{52}L+\gamma_{53}\exp\left(\gamma_{54}L\right), \qquad \gamma_6(L) = \gamma_{61}+\gamma_{62}L+\gamma_{63}\exp\left(\gamma_{64}L\right),$$

Finally, the closed set of equations (1)-(3) clearly defines the scalable I-V MOSFET model presented here.

3. EXPERIMENTAL VERIFICATION

The completed scaling procedure for the model we have developed was verified experimentally on the basis of measured data of CMOS transistors fabricated in the p-well MOSIS technology. Each of the transistors was of W=50μm and T_{ox}=40nm (gate oxide thickness) but the channel lengths were of L=2,3,4,5,6,7,8,10,15,20μm.

To fit parameters to the model we have developed a hybrid optimisation system, which contains a genetic algorithm as a global optimisation tool and local search procedures (based on gradient methods) for final tuning of parameter values [6,7].

Results of the experimental verification of the scalable dc MOSFET model presented in this paper are depicted in Figs. 1 to 10. It should be noticed that agreement between measured (circles) and theoretical characteristics (solid lines) is excellent. Equally close accuracy has been attained for all the measured transistors.

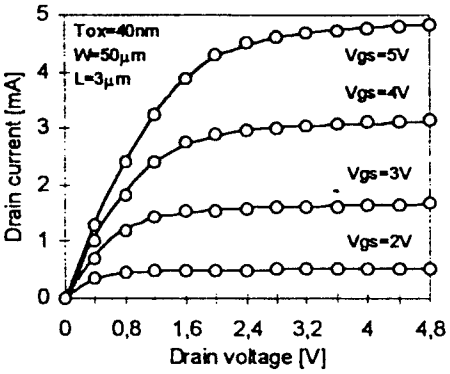

Fig. 1. An NMOS, L=3μm (MOSIS)

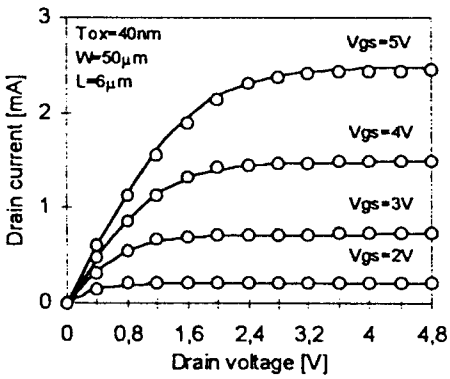

Fig. 2. An NMOS, L=6μm (MOSIS)

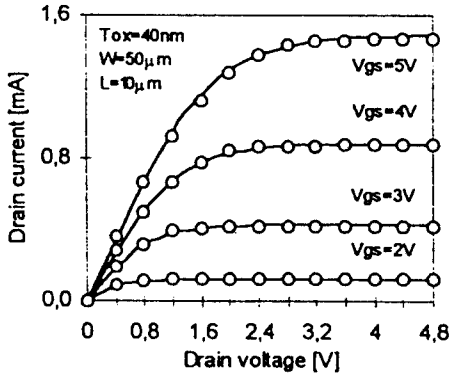

Fig. 3. An NMOS, L=10μm (MOSIS)

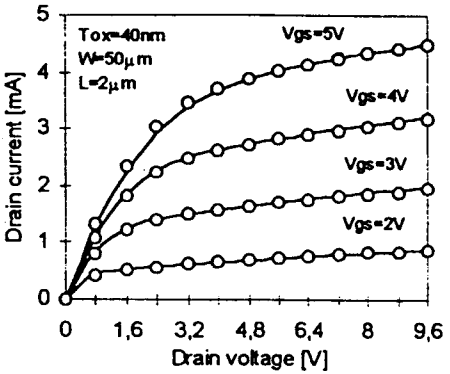

Fig. 4. A PMOS, L=2μm (MOSIS)

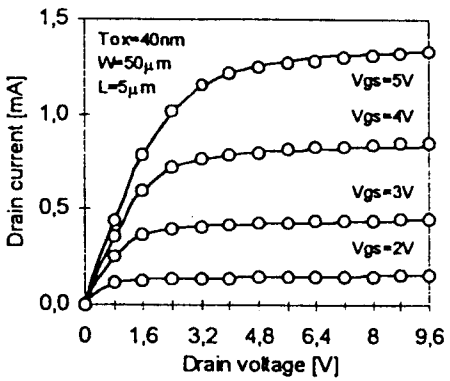

Fig. 5. A PMOS, L=5μm (MOSIS)

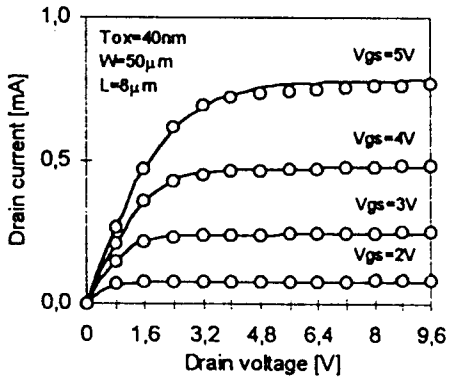

Fig. 6. A PMOS, L=8μm (MOSIS)

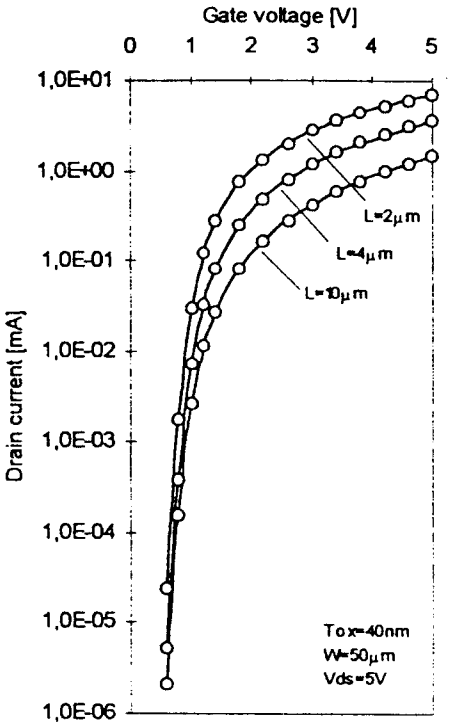

Fig. 7. An NMOS, lgI_D vs. V_{GS} (MOSIS)

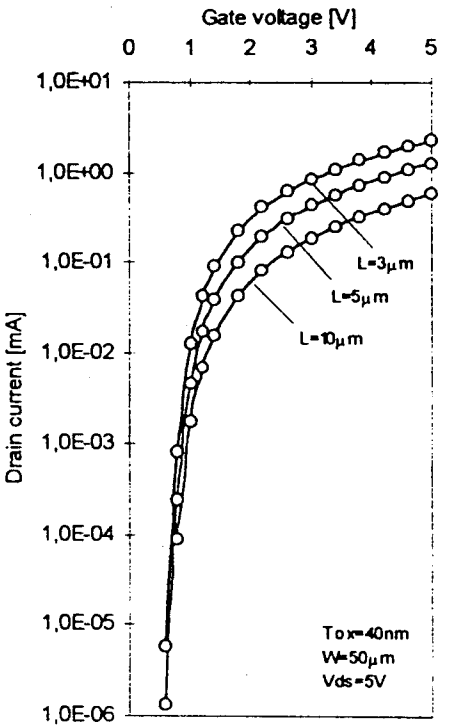

Fig. 9. A PMOS, lgI_D vs. V_{GS} (MOSIS)

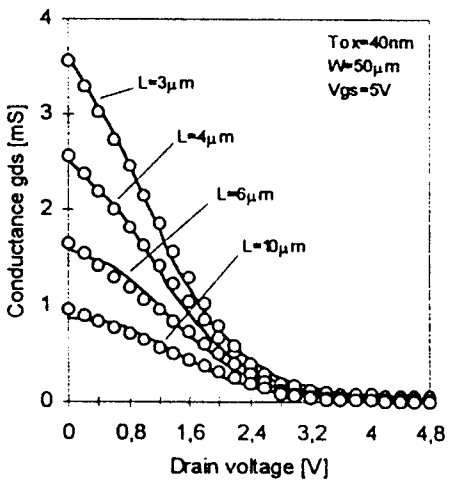

Fig. 8. An NMOS, g_{ds} vs. V_{DS} (MOSIS)

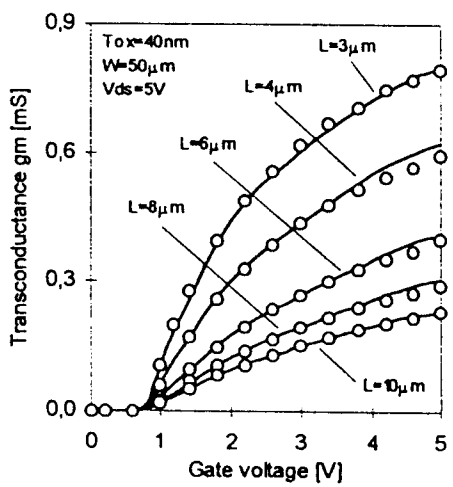

Fig. 10. A PMOS, g_m vs. V_{GS} (MOSIS)

4. CONCLUSIONS

A scaling procedure for the fully analytical, physically based compact MOSFET model for circuit simulation has been proposed. It has been demonstrated that the parameters of the model are independent of the channel length and transistor bias voltages. Unlike the BSIM3v3 [1] and other published MOSFET models the one satisfies the Gummel symmetry test, reflects reverse short-channel effect, and is free from such non-realistic term as shortening channel effect. There are no physical inconsistencies in the model. The model can be applied for CMOS transistors with any long channel down to sub-0.1μm and is very useful for circuit analysis and simulation purposes.

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