

Analog VLSI hardware for fuzzy systems

Bogdan M. Wilamowski

University of Wyoming

Department of Electrical Engineering

Laramie, WY 82071, USA

wilam@uwyo.edu

Abstract - Our world has an analog nature and it is natural to process signals in an analog way. Analog signal processing can be much faster than digital ones and AD or DA conversion is not required. The main obstacle is to develop adequate circuits for nonlinear signal processing. In the presentation several new circuits are proposed. These circuits use nonlinear characteristics of MOS transistors for nonlinear signal processing. The fuzzy signal processing is used as an example. The proposed fuzzyfier circuits are relatively simple while almost arbitrary shapes of membership functions can be obtained. The proposed current mode MAX and MIN operators exhibit accuracy superior to other circuits. The defuzzyfier circuit uses the concept of signal normalization and weighted sum. New normalization circuit, operating in the subthreshold conduction mode, exhibits almost ideal characteristics. The described new building blocks were used to design the entire analog fuzzy VLSI chip.

I. INTRODUCTION

Numerous applications of industrial electronics use intelligent control systems. For example many motor control systems require sophisticated computation. The intelligence is also involved in smart sensors that are able to measure flux and other electrical parameters just by analyzing currents and voltages on the supply terminals. Hardware implementation of intelligent systems use computers or microcomputers for the computation. The digital approach has many advantages. Primarily it is flexible and easy to be reprogrammed. At the same time those digital systems are rather complex and they require analog to digital conversion at the front of the system and digital to analog conversion at its end. Our world has an analog nature and it would be wise to perform all computation in analog fashion.

Analog signal processing is usually much faster than the digital one. Several computation processes can be done simultaneously, and AD and DA conversion is not required. Analog integration or differentiation have been used for many years already. Also, analog summation and multiplication are quite common. For intelligence computation more sophisticated nonlinear functions are required such as WTA (Winner Takes All), fuzzy membership functions [1][3][6][9][14][16], normalization circuits [5][10][11][14], MIN and MAX operators [2][3][7][8][12] division circuits, analog memory, neural circuits, and others. This presentation is focused on the VLSI implementation of fuzzy systems. Nonlinear signal processing is taking advantage of nonlinear characteristics of MOS devices. All building blocks operate in current

mode, which means that the current not voltage carries information.

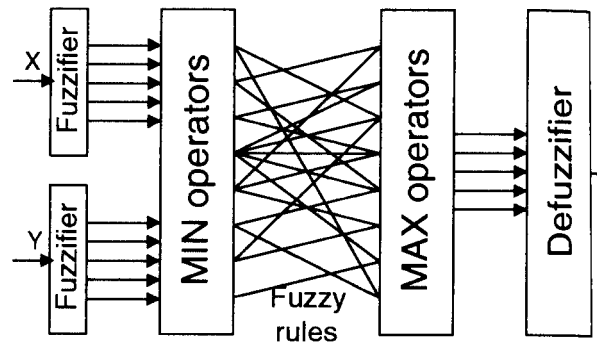


Fig. 1 Classical Zadeh-type fuzzy controller

The block diagram of the classical Zadeh-type [17] fuzzy system is shown in Fig. 1. The system consists of fuzzyifiers, a main processing unit with MIN and MAX operators, and a defuzzyfier. Several VLSI implementations of fuzzy system were already presented [10][15]. The approach in [15] uses voltage mode computation and Tagagi-Sugeno defuzzyfication [13] which leads to simple programming, but requires many transistors for implementation. In the presented approach several new circuit analog signal processing circuits are described. Those circuits are often simpler and have better characteristics.

II. FUZZYFIERS

The fuzzyfier block must convert crisp analog values into several fuzzy variables. The conversion takes place based on the dedicated membership functions of triangular, trapezoidal or Gaussian type shapes. Several different circuits have been already proposed. Ahmadi et al [1] used PWL approximations using current sources. Yamagawa [16] used bipolar technology. Ota and Wilamowski [9] used a similar approach, but MOS transistors were used. In both cases, for a single membership function, two differential pairs were required. Also those differential pairs had to be supplied by several identical current sources. In the proposed approach only one differential pair is required per membership function and one current source per fuzzyfier.

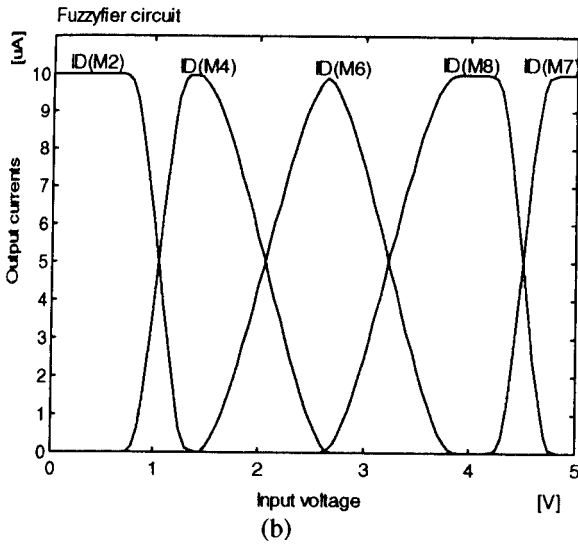
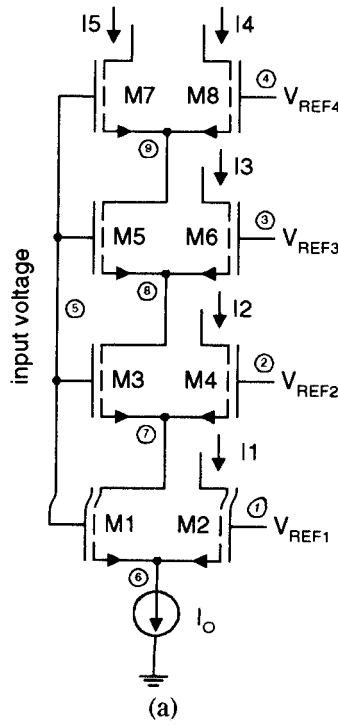


Fig. 2 Fuzzyfier circuit with four differential pairs creating five membership functions: three Gaussian/trapezoidal-like in the center and two sigmoidal types at the ends of the input range: (a) circuit diagram and (b) fuzzyfier characteristics generated by SPICE program.

The circuit diagram of the fuzzyfier is shown in Fig. 2(a), while the fuzzyfier characteristics are shown in Fig. 2(b). In the example shown in Fig. 2(b) transistors M1, M2, M7, and M8 have $W/L = 10\mu\text{m}/2\mu\text{m}$, while others have $W/L = 4\mu\text{m}/4\mu\text{m}$. Transistor models of typical $2\mu\text{m}$ n-well MOSIS process were used in the simulation. Reference voltages were set to 1.0V, 2.0V, 3.2V, and 4.5V. Note that several different shapes of the membership function can be obtained such as: triangular, trapezoidal, and Gaussian. Reference voltages control the width of membership functions, while slopes depend on the W/L ratio of coterminal differential pairs.

III. MIN AND MAX OPERATORS

The voltage mode MIN and MAX operations are very simple to implement [14][15][16]. All that is required to have several voltage followers circuits with all emitters/sources shorted together. Those simple voltage mode MIN and MAX operator have limited accuracy and can operate only in relatively low signal ranges. Current mode MIN/MAX operators operate correctly over several orders of magnitude of signal change. Baturone et al [4] proposed a very clever current mode MAX operator with relatively high accuracy (Fig. 3). The presented here MAX operator is equally simple, but even higher accuracy can be obtained (Fig. 4). Its performance is illustrated in Fig. 5. Each MAX circuit can be easily converted into a MIN circuit by introducing additional biasing currents as it is shown in Fig. 6.

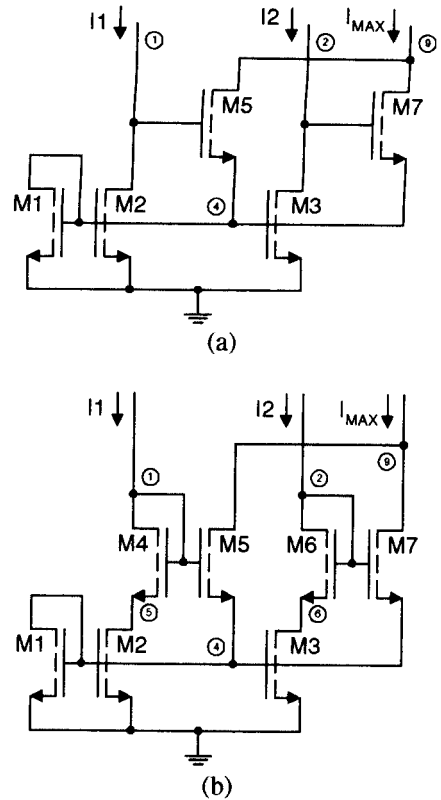
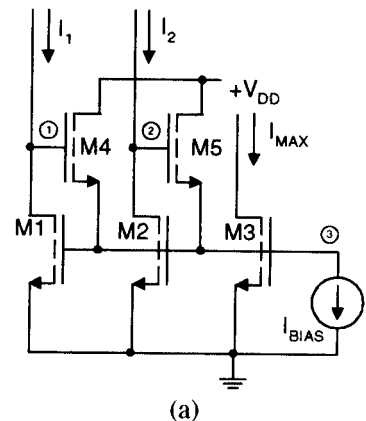


Fig. 3. Baturone MAX operator circuit for two inputs (a) concept diagram and (b) actual implementation.



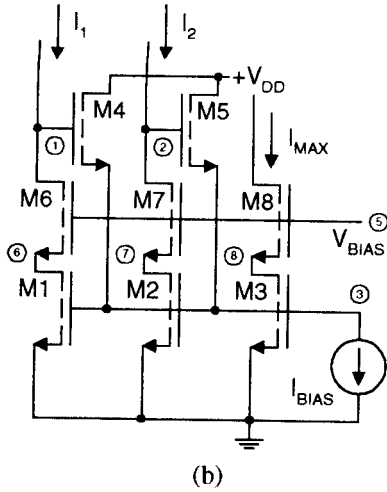


Fig. 4. Proposed MAX operator (a) concept diagram and (b) actual implementation.

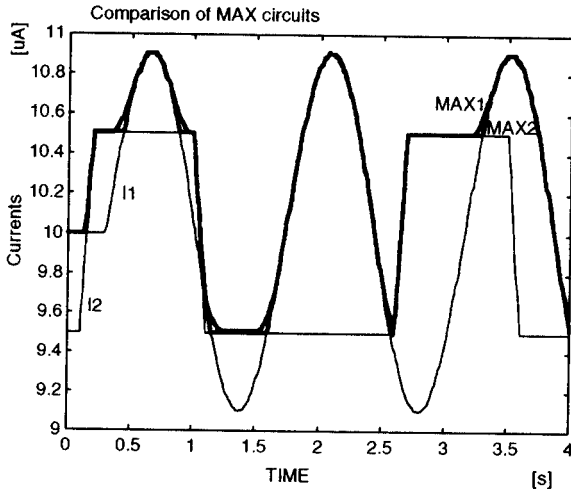


Fig. 5. Accuracy comparison of Baturone MAX1 and new proposed MAX2 circuits

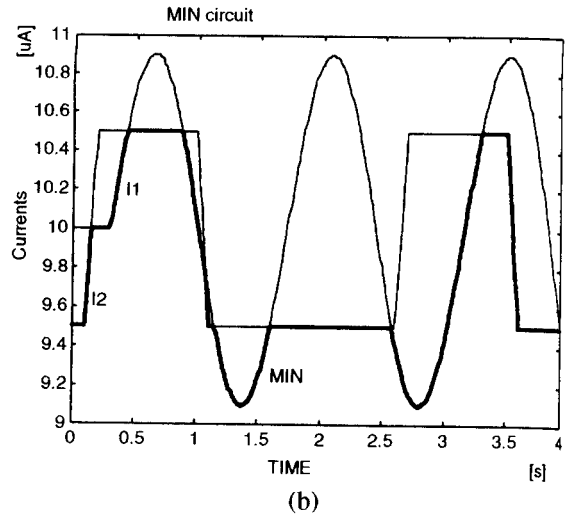
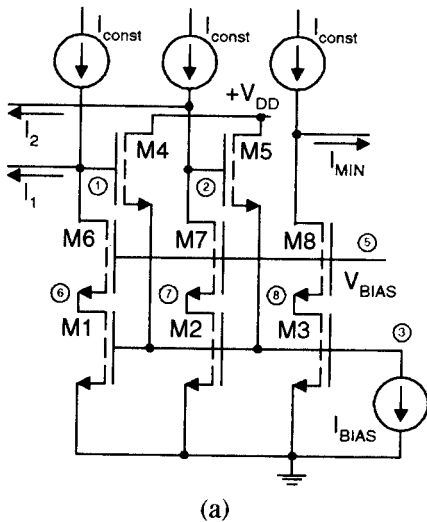


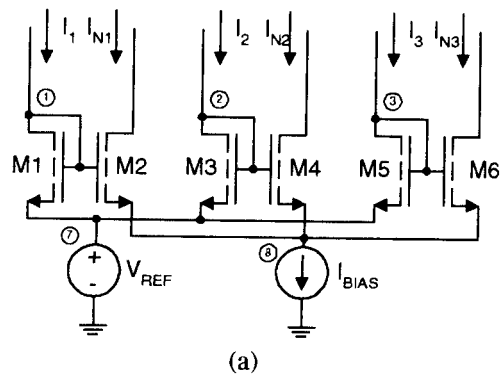
Fig. 6. SPICE simulation results for MAX and MIN circuits (a) accuracy comparison of Baturone et al and new proposed MAX circuits and (b) Results of proposed MIN circuit.

VI. DEFUZZIFYER CIRCUIT

The simplest defuzzification circuit should perform the following computation:

$$OUT = \frac{w_1 x_1 + w_2 x_2 + \dots + w_n x_n}{x_1 + x_2 + \dots + x_n}$$

The required division is very difficult to implement in VLSI. Several attempts have already been made to substitute division by another technique. When negative the feedback approach [7][11] is used, only the effect of dominant inputs (inputs with large signals) is calculated correctly. A similar problem exists, when normalization techniques as described in [10] are used. In order to avoid the defuzzification Takagi-Sugeno [13] was used in the VLSI implementation [15]. Fig. 7 shows new normalization circuit which uses MOS transistors operating in subthreshold conduction mode. The normalization concept requires a gain control on all input signal paths so each signal is attenuated the same way and that the sum of the reduced signals is always constant $x_1 + x_2 + \dots + x_n = const$. Such normalized signals are then summed with weights to complete the defuzzifier circuit.



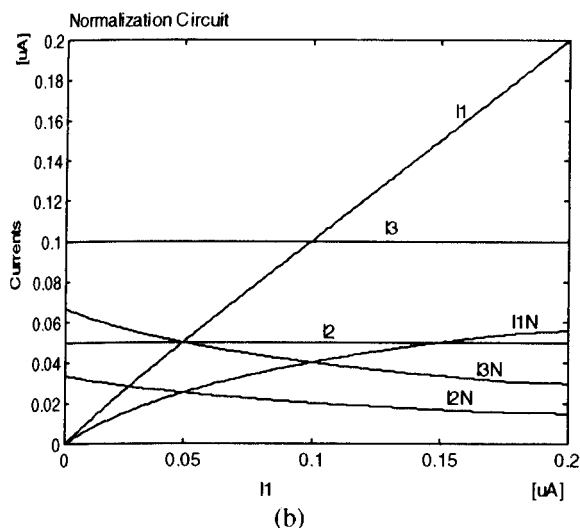


Fig. 7. Normalization circuit with almost ideal characteristics (a) circuit diagram and (b) characteristics

When all transistors of the circuit in Fig. 75. operate in the subthreshold conduction mode the circuit exhibits almost ideal characteristic. This can be also proven analytically. If currents are larger and transistors operate in the strong inversion mode, results are only an approximation of that required. Fig. 7 shows simulation results. Note that sum of normalized currents is always constant and that the same current ratios are preserved after normalization. The latter feature is very difficult to accomplish in other solutions of normalized circuits.

V. CONCLUSION

The presented building blocks such as fuzzyfier, MIN and MAX operators, and defuzzyfier were used in the design of the entire fuzzy VLSI chip. At this point, the designed chip has to be individually designed for each application. The number of membership functions and its shape require proper reference voltages and proper W/L ratios in fuzzyfier circuits. Weights of the defuzzyfier are also adjusted by adequate W/L ratios of current mirrors. Inputs of MIN operators have fixed connections. Fuzzy rules are implemented by proper connections between outputs of MIN operators and inputs of MAX operators.

VI. REFERENCES

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