VLSI Architecture for Analog Bidirectional Pulse-Coupled Neural Networks

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Abstract

A compact architecture for analog CMOS VLSI implementation of voltage-mode pulse-coupled neural network (PCNN) is presented. The main feature of the proposed neuron circuit is that the structure is compact, yet exhibiting all the basic properties of natural biological neurons. Another unique feature of the proposed neuron cell is that one node serves as both input and output, mimicking a natural biological neuron, and the neuron cell uses frequency modulated bidirectional pulse-streams. Functionality of the proposed PCNN circuit is verified with SPICE simulations.

1. Introduction

Natural biological neurons employ rapid pulses, called *action potentials*, for long distance transmission of signals without attenuation. An action potential is fired when the internal potential of the axon hillock exceeds a threshold potential. Because incoming pulses are summed with time, the neuron generates a pulse train with a higher frequency for higher positive excitation. Each neuron is characterized by non-excitability for a certain time after the firing pulse, which is referred to as the *refractory period.* The refractory period sets an upper limit on the frequency of the output pulse train or how rapidly the excitable tissue can discharge. The idea of the neuristor line is to abstract the five key axon properties of (i) threshold of excitation, (ii) refractory period, (iii) constant pulse-propagation velocity, (iv) pulse-shaping action during its propagation through the neuristor line, and (v) annihilation of pulses in case of their collision [1]-[4].

The analog hardware implementation method shows inherent fault tolerance specialties and high speed, which is usually more than an order over the software counterpart. Thus, in order to obtain the full benefit of neural network algorithms, special purpose hardware must be designed and built. Other advantages of using a pulse-coupled technique are that it is immune to noise and less susceptible to process variations between devices. Furthermore, because of their capabilities with regard to image processing applications, PCNN is gaining attention and becoming more popular [5]-[8].

2. CMOS Model of Pulse-Coupled Neuron

Inspired by biological models and the advantages of PCNN, a simple integrated circuit structure for a neuron with synaptic weight multiplication and summation is described in this section. The circuit schematic of the voltage-mode neuron cell shown in Fig. 1 is an electronic analogy of a biological soma; i.e., it initiates reactions, with a given external stimulus, by generating a stream of electrical pulse waves. The circuit structure is based on the current-driven simple neuron cells [9]-[12]. Synaptic weights in these current-mode neuron cells are controlled by current mirrors at the output of the neuron cell with proper *W/L* ratios. However, the synaptic weights controlled by this scheme are relatively sensitive to noise, and thus accuracy of current (synaptic weight) multiplication becomes relatively low.

The proposed voltage-mode neuron cell in Fig. 1 functions as follows. First, notice that both input and output nodes occupy the same node, which is also observed in biological neurons. The circuit has two capacitors, C1 and C2. The stored charge on capacitor C1 corresponds to the charge of sodium ions (Na^+), and the charge stored on C2 corresponds to the potassium ions (K^+) [12]. The potential due to sodium ions changes at a faster rate than the potential due to potassium ions. Therefore, the time constant of the C1 circuit is made smaller than that of the C2 circuit. In a steady state, all the MOS transistors (M1-M3) are cut off. As the potential on C1 increases in time domain, the potential on C1 exceeds the potential on C2 by the threshold value of transistor M1 at some point, then transistor M1 change its state into active region of operation and further activates transistors M2 and M3 which form a current mirror. This leads to the rapid increase of the potential on both capacitors from the supply voltage, V_{DD}, causing an integrate-and-fire action. This positive feedback through transistors M1, M2 and M3 is quickly terminated once capacitor C2 is

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fully charged, and all the transistors become turned off. During the recovery process, known as *refractory period*, capacitor C2 is slowly discharged by resistor R2, and the neuron cell does not respond to any incoming excitations until the potential on C1 exceeds the potential on C2 by the threshold value of M1. Transistors M4 and M5 operate in linear mode and act as resistors. The transient response of the circuit of Fig. 1 for a shifted sinusoidal input excitation is illustrated in Fig. 2. Notice from Fig. 2 that the frequency of output pulses is proportional to the input excitation level; however, the maximum frequency of output oscillation is limited by this refractory period. One can observe this effect with an almost constant frequency for high input excitation level, which illustrates the basic characteristic of a *nonlinear sigmoidal* function seen in both biological and artificial neural networks.

The operation of synaptic weight multiplication in the proposed design can be easily achieved by employing Ohm's law. By adjusting the resistance of the coupling resistors as shown in Fig. 3(a), the current which flows through the axon is controlled, yielding a corresponding rate of pumping charges into the input capacitor C1. In silicon implementation, these coupling resistors are replaced with MOS active resistors as shown in Fig.3(b). The *W/L* ratio in each active resistor as a coupling resistor is adjusted accordingly for synaptic weight multiplication.

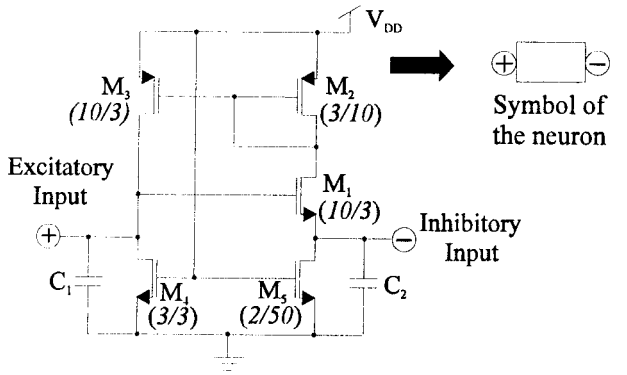


Fig. 1. Circuit schematic of the voltage-mode pulse-coupled neuron and the symbolized neuron with two input nodes.

In order to control both excitatory and inhibitory synaptic weights, the proposed circuit design has two input nodes in the neuron cell; i.e., one node at capacitor C1 for an excitatory (positive) synaptic input, and the other at capacitor C2 for an inhibitory (negative) synaptic input. The block diagram representation of this concept is illustrated in Fig. 3. While the incoming voltage inputs summed at the excitatory node pump up capacitor C1, yielding a positive effect on triggering transistor M1 at its threshold value, the voltage inputs summed at the inhibitory node pump up capacitor C2 and has a negative effect on triggering transistor M1 by increasing its threshold value. In this scheme both excitatory and inhibitory synaptic weights are controlled, as in natural biological neural networks.

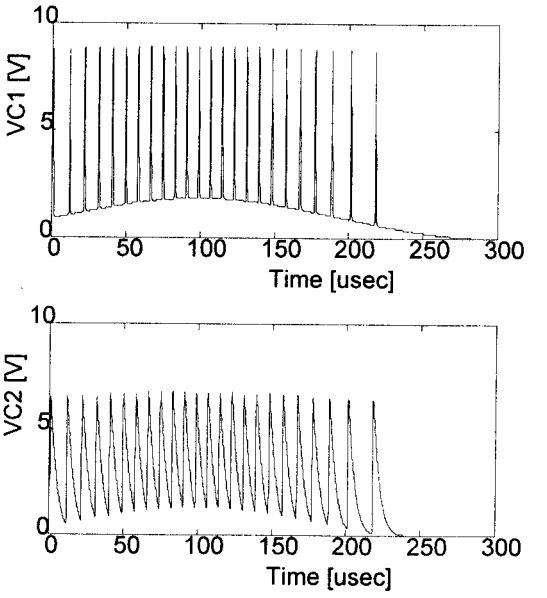


Fig. 2. SPICE simulated transient response of the circuit of Fig. 1 excited with a shifted sinusoidal input. The top graph shows the response on capacitor C1, and the bottom graph shows the response on C2. Notice that the discharge time on C2 is much slower than the discharge time on C1.

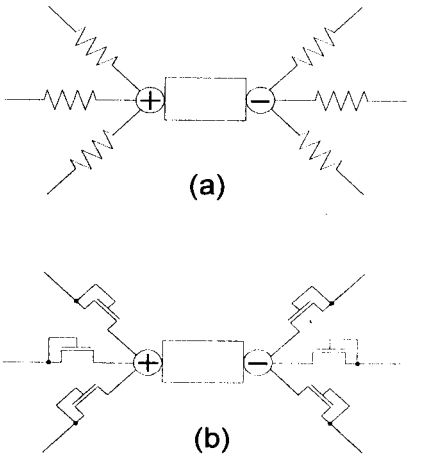


Fig. 3. Concept diagram of synaptic weight multiplication and summation. Notice that there are two input nodes - one for excitatory (+) synaptic inputs, and the other for inhibitory (-) synaptic inputs. (a) Synaptic weights are controlled by the resistance of the coupling resistors. (b) CMOS implementation of the resistors in (a) for synapses. Synaptic weights are adjusted with *W/L* ratios of the MOS transistors.

3. Neuromorphic Pulse Delay Lines and Properties of Axons

While neural cells in nervous systems are small, their axons for transmitting pulse trains may be very long. Those axons may be coated with *myelin sheath*, which takes the form of a series of nodes. Every few millimeters on a myelinated axon, a bare patch of axon is exposed at what are called *nodes of Ranvier*. Those nodes of Ranvier create a segmented effect, allowing passage of sodium ions and potassium ions. The inputs of series of neural cells can be connected in a chain by simple coupling resistors to form an axon as shown in Fig. 4. In this section, the following basic properties of axons are emphasized and demonstrated:

1. threshold point of a pulse firing action
2. pulse shaping action during its propagation through an axon (delay line)
3. refractory period
4. constant pulse-propagation velocity
5. annihilation of pulses in case of their collision
6. bidirectional form pulse propagation

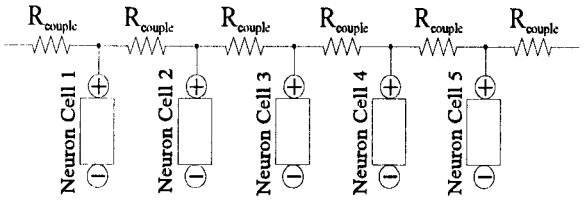


Fig. 4. Neuron cells connected in a chain to form an axon.

Several researchers have developed a neuromorphic delay lines [1]-[3],[12],[14] demonstrating some of the above properties. Some of these existing designs are compact and attractive, yet some utilize bipolar transistors [1],[2], which consume more power than CMOS counterparts, and an extra synaptic weight control unit is necessary to form a complete neural network [1]-[3]. Another interesting design uses a number of CMOS inverters (9 stages) [14] in a single neuron cell to accomplish these properties. The biggest merit of the presented design here is the significantly reduced number of CMOS transistors, allowing less power consumption and reduced silicon area. The area of a single neuron cell, using the standard MOSIS 2μm, single-polysilicon, double-metal technology, is approximately 60μm x 120μm. These six axon properties with the proposed circuit design are discussed in detail here.

1. Threshold Point:

The first property, threshold point of a pulse firing action, was already demonstrated in Fig. 2 in the previous section. Recall that a pulse is fired when the potential on C1 exceeds the potential on C2 by the threshold value of transistor M1.

2. Pulse Shaping Action:

Without a pulse shaping action, traveling pulses could be seriously attenuated and dispersed throughout the transmission. Therefore, axons which have similar membrane structures should be able to regenerate the shape of transmitting pulses. Incoming pulses are regenerated and shaped as they transmit along the axon. Fig. 5 illustrates the pulse shaping action for a square input pulse. If an input pulse is too narrow, it will be annihilated. The shaping of the propagated pulse through the axon depends on the time constant of the output capacitor circuit.

3. Refractory Period:

When the axon circuit is excited with a series of incoming pulses, those pulses can be transmitted through the axon if the incoming pulses are widely separated, as shown in Fig. 6(a). On the other hand, some incoming pulses are skipped and not transmitted when the time interval between the incoming pulses is small, as shown in Fig. 6(b). The refractory period of the delay line is caused by the existence of the cut-off threshold voltage at the transistor M1 after passing of a pulse through each section of the delay line.

4. Constant Pulse-Propagation Velocity:

Fig. 5 also demonstrates the property of constant pulse-propagation velocity. Neuron Cell 1 of Fig. 4 is initially stimulated with a voltage input in this simulation. One can observe that the resulting output pulse from Neuron Cell 1 activates Neuron Cell 2 and is seen to propagate at a constant velocity from left to right toward Neuron Cell 5. The extended refractory period of the excited pulses prevents the output pulses of neighboring units from reactivating a previous neural cell and insures that a single pulse is propagated.

5. Annihilation of Pulses:

Annihilation of pulses in case of their collision when pulses are propagating from opposite directions is

a consequence of the existence of the refractory period, which causes a pulse attenuation. By simultaneously stimulating Neuron Cell 1 and Neuron Cell 5 in Fig. 4, two analog pulses will collide at Neuron Cell 3 and annihilate each other since both Neuron Cell 2 and Neuron Cell 4 will both be in refractory period when Neuron Cell 3 fires a pulse. This important property is demonstrated in Fig. 7.

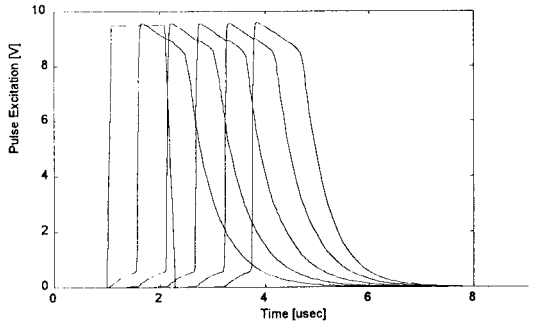
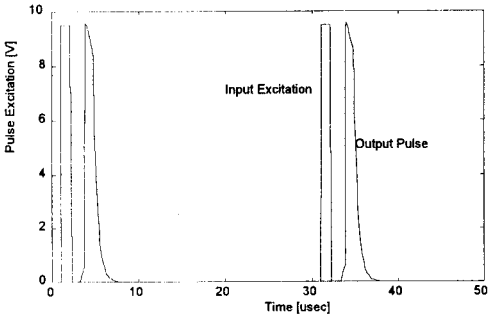
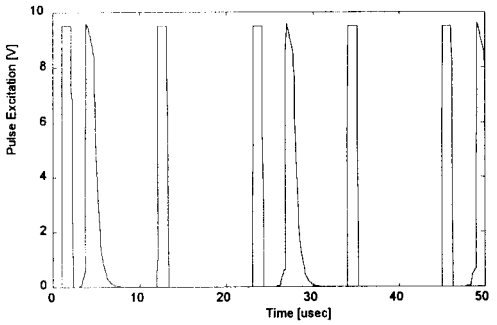


Fig. 5. SPICE simulated transient response to demonstrate the pulse shaping action and constant pulse-propagation velocity from Neuron Cell 1 to Neuron Cell 5 in the axon with a square input voltage.



(a)



(b)

Fig. 6. SPICE simulated transient response to demonstrate the refractory period. (a) With a large time interval between input excitations, all excitations are transmitted through the axon. (b) With a small time interval between input excitations, some excitations are not transmitted due to the existence of the refractory period.

6. Bidirectional Form Pulse Propagation:

Notice also from Fig. 7 that with this proposed neuron cell, excited pulses are capable of propagating in bidirectional form, as opposed to the existing conventional neuron circuits in which excited pulses transmit only in one direction.

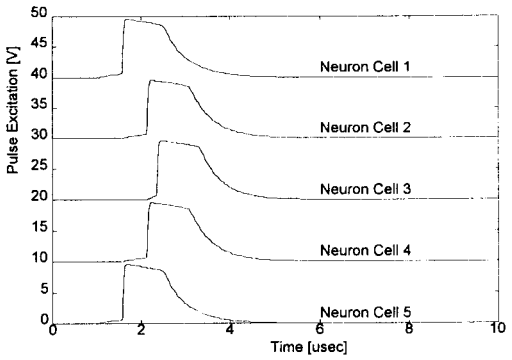


Fig. 7. SPICE simulated transient response to demonstrate the annihilation of pulses in case of their collision. Note that two pulses are propagating from *opposite directions*, demonstrating *bidirectional* pulse transmission capability. Inputs are excited at Neuron Cell 1 and Neuron Cell 5 simultaneously, and the pulses collide at Neuron Cell 3. After the collision, the pulses are annihilated as a consequence of the existence of the refractory period in the neighboring neuron cells. (Note that in order to illustrate the individual pulse action, pulses on Neuron Cells 1, 2, 3, and 4 are shifted at the post-processing stage. In other words, all the pulse excitations are within a 10-volt range.)

4. Conclusion

A CMOS hardware design to realize a pulse-coupled neural network is developed. The proposed neuron circuit has all the basic properties of natural biological neurons: (i) threshold point firing, (ii) pulse shaping action during its propagation through an axon, (iii) refractory period (i.e., showing a nonlinear sigmoidal characteristic), (iv) constant pulse-propagation velocity, (v) annihilation of pulses in case of their collision, and (vi) bidirectional pulse propagation. Another important feature of the proposed design is that the circuitry is robust to additive noise. Excitatory and inhibitory synaptic inputs are applied to the two capacitors (two input nodes), C1 and C2, respectively, and synaptic weights are adjusted and multiplied by proper *W/L* ratios of MOS active resistors in axons. The neuron cell circuitry which has been developed here exhibits functional similarities to natural biological neurons. One improvement that can be made for future is to extend the original circuit for programmable (adjustable) synaptic weights using either analog memory or digital memory. A digital memory approach is straightforward using

SRAM or shift registers or PAL. An 8-bit digital programmable weight multiplication circuit [16] can be used for an accurate and easy weight adjustment.

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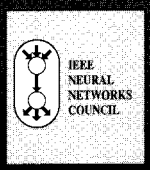

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