DESIGN, CALIBRATION, AND APPLICATION OF OPTIMIZED (111) SILICON STRESS SENSING TEST CHIPS

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ABSTRACT

Test chips incorporating piezoresistive stress sensors are powerful tools for experimental stress analysis of electronic packages. Sensor rosettes on (111) silicon offer the unique ability to characterize the complete stress state on the surface of a die. In this work, the design and calibration of two second generation (111) stress sensor test chips are described. The first test chip contains perimeter pads suitable for wire bond packages, and the second test chip contains an area pad array suitable for flip-chip applications. The rosettes on the fabricated (111) silicon sensor die have been calibrated using four-point bending, hydrostatic, and wafer level calibration methods. The test chips are currently being utilized to characterize stress in a variety of plastic encapsulated and flip-chip packages.

INTRODUCTION

The basic concepts involved when using test chips incorporating piezoresistive sensors for experimental stress analyses of electronic packages are shown in Figure 1. The structures of interest are semiconductor chips which are incorporated into electronic packages. The sensors are resistors which are conveniently fabricated into the surface of the die. Thus, they are an integral part of the structure (chip) to be analyzed. The stresses in the chip produce resistance changes in the sensors (due to the piezoresistive effect) which can be easily measured. Using appropriate piezoresistivity theory and calibrated material constants, one or more of the stress components can be calculated from the measured resistance changes. Therefore, the sensors are capable of providing non-intrusive measurements of the state of stress at points on the surface of a chip, even within encapsulated packages (where they are embedded sensors). If the piezoresistive sensors are calibrated over a wide temperature range, thermally-induced stresses can be measured. Finally, a full-field mapping of the stress distribution over a die's surface can be obtained using specially designed test chips which incorporate an array of sensor rosettes.

Theoretical analysis [1,2,3] has established that properly designed sensor rosettes on the (111) silicon wafer plane have several advantages relative to sensors fabricated using standard (100) silicon wafers. In particular, optimized rosettes on (111) silicon can be used to measure the complete state of stress (6 stress components) at a point on the top surface of the die, while optimized rosettes on (100) silicon can measure at most 4 stress components. Also, optimized sensors on (111) silicon are capable of measuring 4 temperature compensated combined stress components, while those on (100) silicon can only be used to measure 2 temperature compensated quantities. Furthermore, it has been established that the (111) plane offers the opportunity to measure the highest number of stress components in a temperature compensated manner [3]. This is particularly important, given the large thermally induced errors which can often be found in stress sensor data. The 4 stress components which can be measured in a temperature compensated manner using (111) silicon sensors are the 3 shear stress components and the difference of the in-plane normal stress components.

(111) SILICON TEST CHIP DESIGNS

In the current work, two (111) silicon test chips were designed, fabricated, and calibrated. Each chip design features an array of optimized eight-element measurement rosettes. As shown in Figure 2, these rosettes are

composed of two sets of n- and p-type resistors, each with the orientations of 0-45-90-135. As discussed above, such rosettes can be used to evaluate all 6 stress components, and 4 temperature compensated combined stress components. The first test chip contains perimeter pads suitable for wire bond packages, and the second test chip contains an area pad array suitable for direct chip attach (DCA/flip-chip) applications.

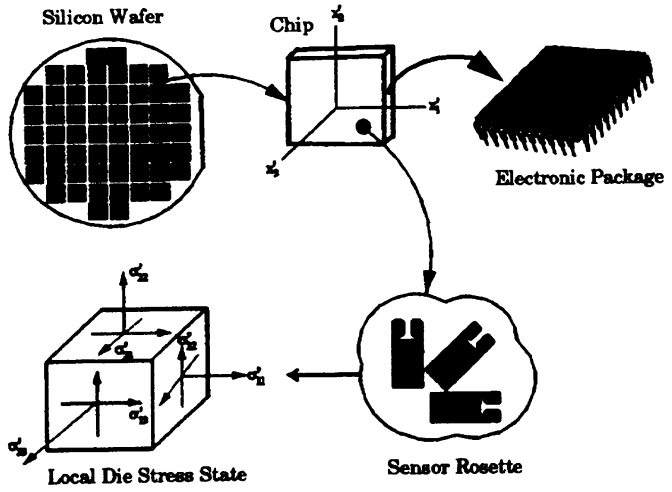

Figure 1 - Piezoresistive Test Chips

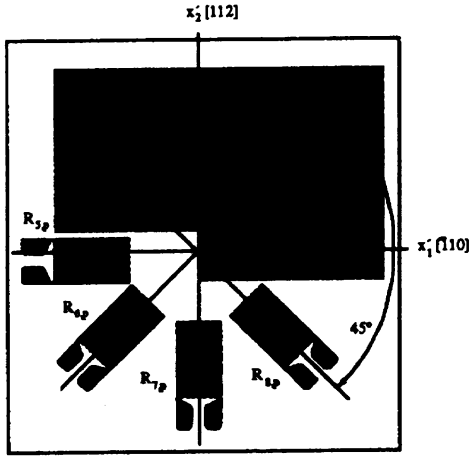

Figure 2 - Optimized Rosette

A schematic of the perimeter pad chip (BMW1 Test Chip) is shown in Figure 3. The basic die image is 200 x 200 mils. It contains 12 of the eight-element optimized complete stress state measurement rosettes. A photograph of a rosette from one of the fabricated test chips is shown in Figure 4. The eight rosette elements can be configured as four two-element half-bridges in order to simplify the resistor change measurements. A fully ion-implanted process has been used to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. Process simulations and experimental results from a processing matrix have verified that relatively large values of the piezoresistive coefficients have been achieved.

Figure 3 - BMW1 Test Chip

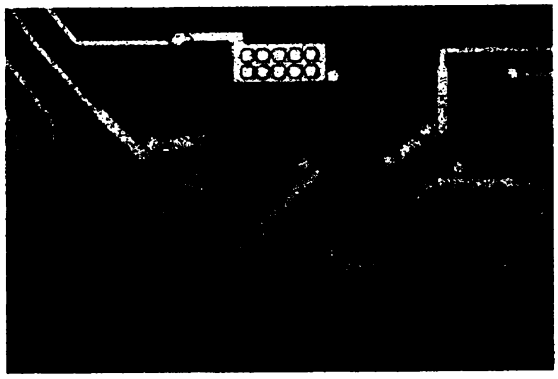

Figure 4 - Fabricated Rosette

The overall wafer image is formed by replication of the basic 200 x 200 mil die. The sensors on each die have been positioned to fully map the die surface stress distributions when the die is symmetrically loaded. The die are interconnected on the wafer using a special inter-chip connection pattern which permits the wafer to be cut up in multiples of 200 mils in both the horizontal and vertical directions, while maintaining access to the interior sensors across three chip boundaries. This interconnection pattern permits access to interior sensors on die as large as 1200 x 1200 mils. The basic 200 x 200 mil die image also contains 100 x 100 mil and 100 x 200 mil subimages for use in stress studies involving smaller die.

The flip-chip design (BMW3 Test Chip) provides an area array of 5 x 5 mil pads, on 20 mil centers. The optimized eight element rosettes are placed between the pads as well as directly under pads. This facilitates studies of the out-of-plane shear stresses transmitted to the die by the solder bumps. The basic repeated image on the wafer is a sensing cell (see Figure 5) with a 4 x 4 set of pads (80 x 80 mils). This cellular approach allows flip-chip test die of almost any preferred size to be cut from the wafers.

TEST CHIP CALIBRATION

The stress states at points on the die are extracted from the resistance changes measured with the sensor rosettes using a set of complicated theoretical equations established by the authors [1,2,3]. Due to size limitations, these expressions are not repeated here. For utilization, the mathematical expressions require accurately calibrated values of six piezoresistive coefficients (B_1, B_2, and B_3 for both the p- and n-type resistors). These parameters are material constants relating the resistivity components to the stress components, and can be measured using controlled calibration experiments where the resistance versus stress behavior is monitored for a particular mechanical loading applied to the chip. In this work, the rosettes on the optimized (111) test chips have been calibrated using four-point bending [4], wafer level [5,6], and hydrostatic [7] calibration methods. The four-point bending and wafer level techniques subject the die to in-plane stress states, so that only constants B_1 and B_2 can be evaluated. It has been shown that characterization of material constant B_3 requires the die to be subjected to a controlled stress state which has non-zero out-of-plane normal or shear stresses. Hydrostatic calibration has proven to be the most expedient method to satisfy this condition.

In the four-point bending method, a rectangular strip containing a row of chips is cut from a wafer and is loaded in a four-point bending loading fixture (see Figure 6). Figure 7 shows typical resistance change versus uniaxial stress data obtained using four point-bending loading of a strip cut from one of the fabricated BMW1 test chip wafers. In this case, resistance change data were recorded for the 0-90 n-type resistors in one of the rosettes. Using the established theoretical equations, the slopes of these data sets are known to be the desired piezoresistive coefficients B_1 and B_2 for the n-type sensors. In the wafer level calibration method, the wafer itself was supported on a vacuum chuck, and air inside the chamber was removed causing a uniformly distributed load to be applied to the wafer (see Figure 8). This technique also allowed coefficients B_1 and B_2 to be measured, providing a check on the four-point bending data. In the case of hydrostatic calibration, a high capacity pressure vessel was used to subject a single die to triaxial compression. Theoretical considerations has shown that the slope of the resistance change versus pressure response in this case is $(B_1 + B_2 + B_3)$ for a sensor at any orientation.

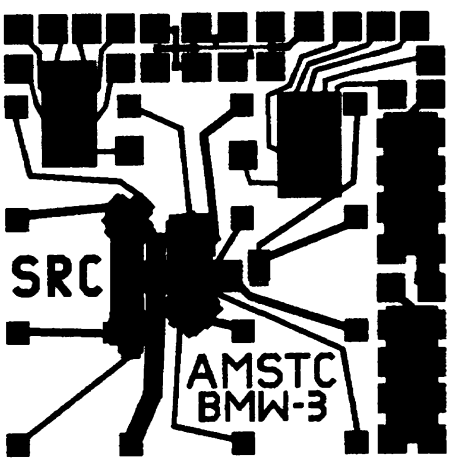

Figure 5 - BMW3 Sensing Cell

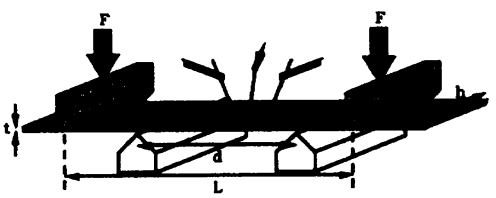

Figure 6 - Four-Point Bending Schematic

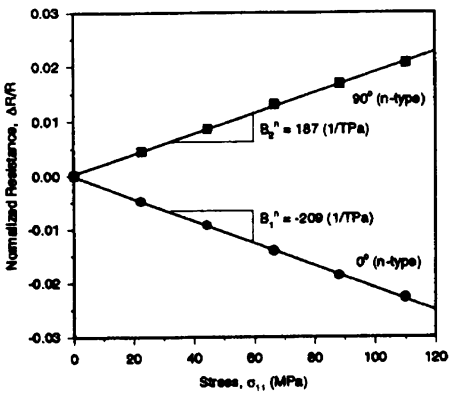

Figure 7 - Typical Calibration Results

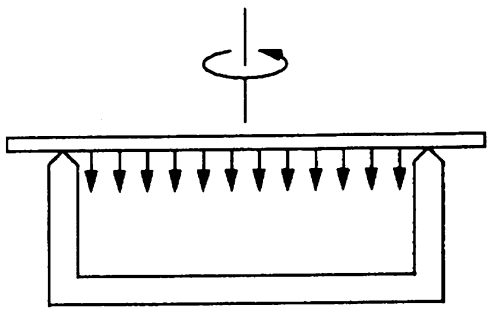

Figure 8 - Wafer Level Calibration Schematic

TECHCON DEMONSTRATION

In the scheduled demonstrations at the TECHCON conference, sample test chips (both bare and packaged die) will be available for inspection. Also, calibration experiments will be performed on sample test chips, and typical data will be recorded and processed. Finally, software for data acquisition and stress measurement will be demonstrated for test chips packaged in both chip-on-board and plastic encapsulated packages.

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