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CMOS IMPLEMENTATION OF A VOLTAGE-MODE FUZZY MIN-MAX CONTROLLER

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In this paper, a general-purpose fuzzy min-max network using a Gaussian-type membership function fuzzifier is proposed. Particularly, CMOS implementations of the Gaussian-type membership function fuzzifier circuits, min-max operators, and the defuzzifier circuit are analyzed. Programmability of the proposed Gaussian-type function fuzzifier can be achieved by changing the gate voltages and the sizes of transistors in the differential pairs. A closed-loop control scheme is used between the fuzzifier and defuzzifier blocks to compensate the global normalization of the denominator in the division of a centroid calculation in the defuzzifier block.

1. Introduction

Fuzzy systems were introduced by L. Zadeh[1] as a means of representing and manipulating data that was not precise, but rather fuzzy. His theory provided a mechanism for representing *linguistic* variables such as "hot", "warm", "cool", and "cold". On the other hand, the traditional set theory describes rather *crisp* information. There are no middle values in the latter case, and it uses probability theory to explain whether an event will occur. In contrast, fuzzy theory describes the degree to which an event occurs.

Starting in the late 1970s fuzzy logic systems became a practical reality. The number of practical applications of fuzzy controllers is currently growing at an accelerated rate and are finding applications in commercial consumer products such as cameras, rice-cookers, washing machines, and so forth. Fuzzy controllers were implemented initially in the form of software using conventional microprocessors. This resulted in relatively slow operation speed, well below 1 kFLIPS (Fuzzy Logic Inferences Per Second) which is not large enough for real-time control problems.[2] For high speed applications, analog techniques are known to be faster than digital techniques with significantly less power consumption and silicon area requirements. Inherent imprecision of analog circuits which has hindered their applications in other areas is expected to be of little concern in fuzzy controllers because such systems are inherently tolerant to imprecision as linguistic variables are used. Analog fuzzy chips have also a distinctive compatibility with sensors. Although the comparison of merits and demerits between analog and digital fuzzy hardware systems is not an issue in this paper, there are some distinctive features of employing digital fuzzy hardware as well. It has an easy programmability and good compatibility with

digital systems. The adoption between analog and digital fuzzy hardware systems should be made according to the circumstances and applications.

In fuzzy systems there are three main steps: (1) fuzzification (membership function generation), (2) fuzzy inference or fuzzy rule evaluation, and (3) defuzzification as shown in Fig. 1. An excellent tutorial on the utility of a fuzzy system and its application are reported.[3] A Gaussian or triangular function is normally used in the fuzzification process. The second step, fuzzy rule evaluation or fuzzy inference, uses a technique called min-max inference to calculate numerical values representing the truth for certain consequent action based on a set of rules bearing the consequent. The development of the fuzzy min-max operators has been an evolutionary process that is fast, efficient, reliable, and still capable of revealing structure although the system itself is an unsupervised leaning network. The defuzzification step is a process of combining all fuzzy outputs in a specific, crisp result that can be applied to each system output.

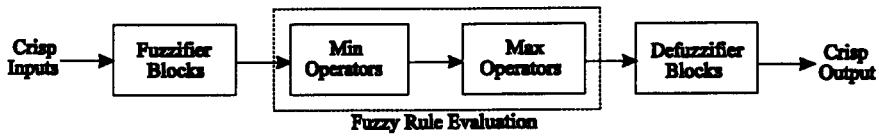


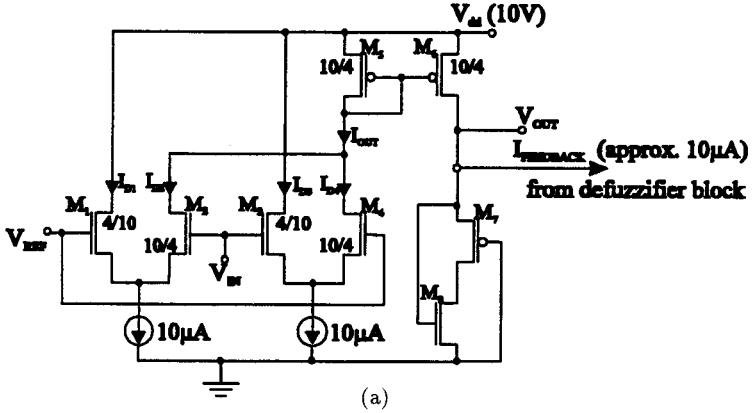
Fig. 1. Block diagram of conventional fuzzy min-max network.

The remainder of this paper is organized as follows. Section 2 provides the fuzzifier block using a Gaussian-type membership function and its hardware implementation. Section 3 gives the min-max fuzzy inference structure with the circuit designs, and Sec. 4 explores the defuzzification process and its hardware implementation. Finally, Sec. 5 concludes this paper with some possible future issues that need to be addressed.

2. Fuzzifier Block

The first stage of a fuzzy system is the fuzzifier block. A Gaussian or triangular membership function is normally used in this step. A membership function of an analog consequent is sampled to discrete grades. J. Choi *et al.*[4] introduced a voltage-input/current-output programmable Gaussian function network. In their design capacitors are used for the programmability; therefore, periodic refreshing is necessary to maintain an accurate programmed value. Also, the reference current needs to be adjusted to control the amplitudes of the output current in their design. A membership function circuit which can realize any four types of membership functions: S-function, Z-function, trapezoidal function, and triangular function, using bipolar transistors was reported.[3] However, a drawback of this design is that it needs emitter-follower arrays for impedance transformation and level/temperature compensation. I. Baturone *et al.*[5] proposed current-mode membership functions of triangular and trapezoidal types using two reference voltages.

Two approaches have been taken to design a fuzzifier circuit in this paper. The two approaches here have basically the same structures, and they are not biased in the subthreshold region so that a significant driving capability is achieved. In the strong-inversion region, the MOS transistors have a power-law dependence on the gate bias voltages. Since the strong-inversion operation of MOS circuits provides the features of high current driving, large dynamic range, and high noise immunity, the high-speed analog VLSI fuzzy controllers are desirable to be built with MOS transistors biased in the strong-inversion region. It is also optimized for several design issues such as operation speed, cell compactness, and precision to be suitable for scaleable fuzzy controller implementation. The transistors with large channel lengths are used to avoid the channel-length modulation effect and to lower the output conductance. The circuit schematic of the first approach of



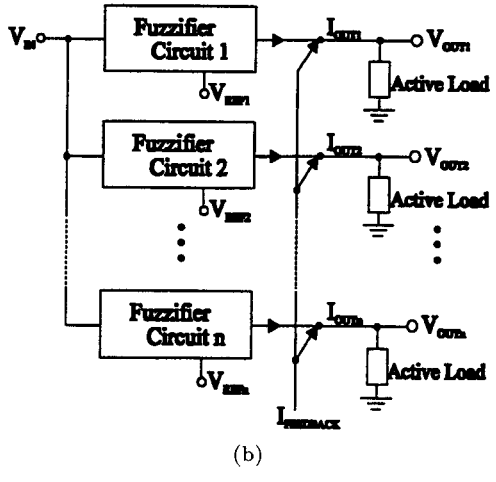
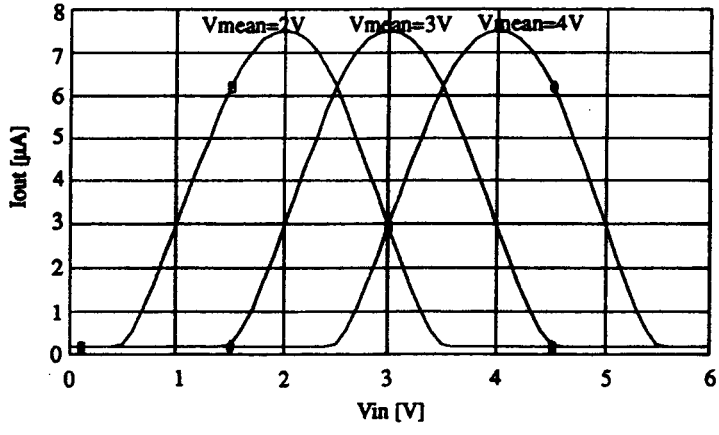
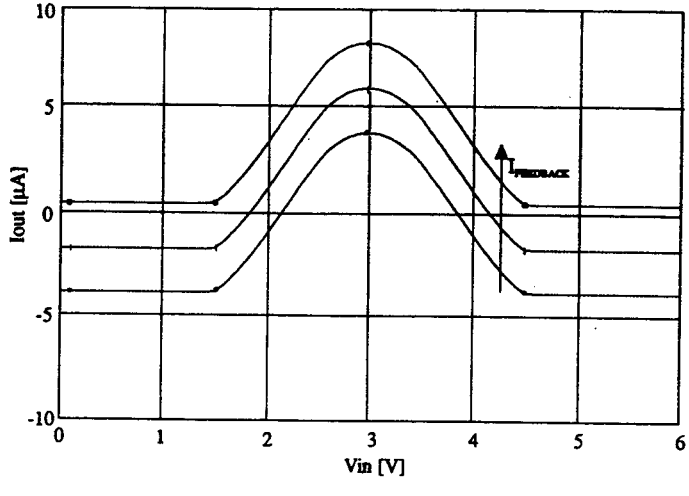


Fig. 2. Gaussian-type membership function fuzzifier #1. (a) Circuit diagram of the first proposed designed. Transistor sizes are shown. (b) Block diagram of the implementation.

the Gaussian-type membership function generator with CMOS differential pairs is shown in Fig. 2(a). In the first approach the input voltage is applied to the gate terminals of M2 and M3 in the differential pair, and the voltage that determines the mean of a Gaussian-type curve is applied to the gate terminals of M1 and M4. The transistors M7 and M8 are used as a high resistive load.[6] Figure 2(b) shows the block diagram of the implementation of the fuzzifier circuit with different mean values, and its SPICE simulated characteristic of the output voltages of this implementation is shown in Fig. 3(a). The fuzzifier circuit is also controlled by the feedback current which is the output current of the defuzzifier block. The



(a)



(b)

Fig. 3. (a) SPICE simulation result with different mean values. (b) Effect of the feedback current in the fuzzifier circuit.

detailed explanation of the defuzzifier block as well as the feedback concept is given in Sec. 4, but the basic idea of the feedback current is that it compensates and shifts the output voltage of the defuzzifier circuit so that the division in the computation of the centroid can be avoided. To compensate the output voltage of the defuzzifier circuit, the output voltage of the fuzzifier circuit needs to be shifted up or down. This compensation is achieved by supplying an extra current source using the feedback current to the fuzzifier circuit. Figure 3(b) shows the SPICE simulated result of the effect of the feedback current in the fuzzifier circuit. As can be seen, a Gaussian-type curve shifts down as the feedback current decreases in the direction shown in the figure, and vice versa.

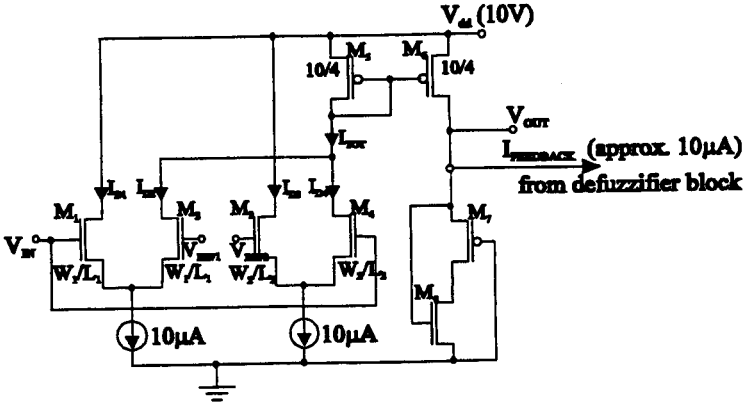


Fig. 4. Circuit schematic of the Gaussian-type membership function fuzzifier #2. Transistor sizes are shown.

The second fuzzifier design is shown in Fig. 4. It functions in a similar manner as the first approach. The difference is that there are two reference voltages applied to the gates of M2 and M3. The average of these two reference voltages determines the mean of a Gaussian-type curve, and the input voltage is applied to the gates of M1 and M4. For transistors operating in the saturation region, the drain currents are expressed using the quadratic approximation as

$$I_D = \frac{K'W}{2L}(V_{GS} - V_{th})^2 \tag{1}$$

where K' is a transconductance parameter, W is channel width, L is channel length, V_{GS} is gate-to-source voltage, and V_{th} is threshold voltage. Using Eq. (1) drain currents for the differential pairs shown in Fig. 4 can be derived as

$$\begin{aligned} I_{D1} &= \frac{I}{2} + V_{id1}\frac{I}{2V_{th}}\sqrt{2\left(\frac{K'W_1V_{th}}{2L_1I}\right) - \left(\frac{V_{id1}}{V_{th}}\right)^2\left(\frac{K'W_1V_{th}}{2L_1I}\right)^2} \\ &= \frac{I}{2}\left[1 + \alpha_1\sqrt{2\beta_1 - \alpha_1^2\beta_1^2}\right] \end{aligned} \tag{2}$$

where

$$V_{id1} = V_{IN} - V_{REF1}\,, \tag{3}$$

$$\alpha_1 = \frac{V_{IN} - V_{REF1}}{V_{th}} \quad \text{and} \quad \beta_1 = \frac{K'W_1V_{th}}{2L_1I} \tag{4}$$

and

$$I_{D2} = \frac{I}{2}\left[1 - \alpha_1\sqrt{2\beta_1 - \alpha_1^2\beta_1^2}\right] \tag{5}$$

and similarly,

$$I_{D3} = \frac{I}{2}\left[1 + \alpha_2\sqrt{2\beta_2 - \alpha_2^2\beta_2^2}\right] \tag{6}$$

$$I_{D4} = \frac{I}{2}\left[1 - \alpha_2\sqrt{2\beta_2 - \alpha_2^2\beta_2^2}\right] \tag{7}$$

where

$$\alpha_2 = \frac{V_{IN} - V_{REF2}}{V_{th}} \text{ and } \beta_2 = \frac{K'W_2V_{th}}{2L_2I}\,. \tag{8}$$

For n-channel MOS transistors, $K' = 24\ \mu\text{A/V}^2$ and $V_{th} = 0.75$ V which are typical values used in a standard MOSIS technology. In order for the circuit to generate a Gaussian-type curve properly, V_{REF1} must be greater than V_{REF2}. Also, because Eqs. (2), (5), (6), and (7) become invalid when the voltage V_{GS} is lower than V_{th}, the following condition must be met.

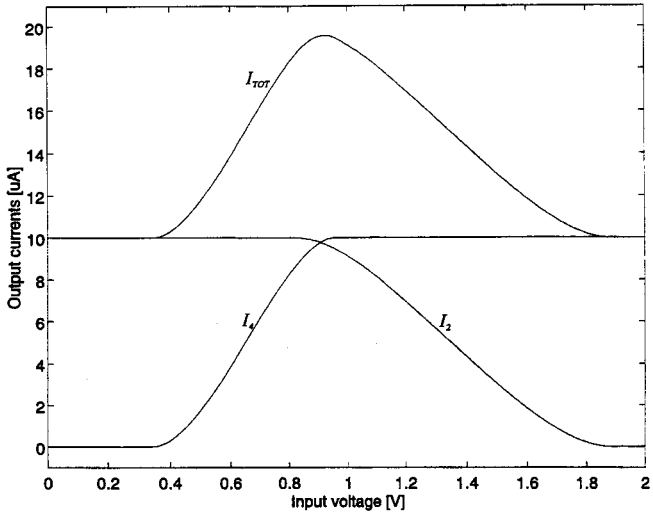
$$-\sqrt{\frac{1}{\beta_i}} < \alpha_i < \sqrt{\frac{1}{\beta_i}}; \qquad i = 1,\ 2 \tag{9}$$

The drain currents reach 0 or the source current I depending on the biasing at the outside of the range given by relation (9). The output current I_{OUT} is then the sum of the two currents I_{D2} and I_{D4}, and it is expressed as

$$\begin{aligned} I_{OUT} &= I_{D2} + I_{D4} \\ &= I + \frac{\alpha_1}{2}\sqrt{2\beta_1 - \alpha_1^2\beta_1^2} - \frac{\alpha_2}{2}\sqrt{2\beta_2 - \alpha_2^2\beta_2^2} \end{aligned} \tag{10}$$

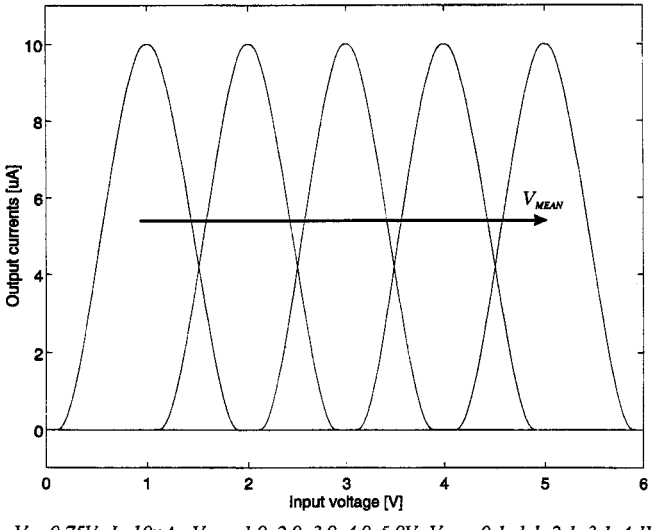
The simulated characteristic of the output current I_{OUT} is shown in Fig. 5(a). As can be seen, the output current resembles a Gaussian function curve with asymmetrical slopes. In this simulation different W_i/L_i ratios are used between the two differential pairs to generate an asymmetrical curve. Note that the resultant output current is shifted up by 10 μA because two currents are summed. However, in further simulations this current shift is subtracted down by 10 μA. The values of the control parameters α_i and β_i specified in expressions (4) and (8) are chosen to obtain a desired shape of Gaussian-type curves. As mentioned, the mean of a Gaussian-type curve is determined by taking the average of the two reference

voltages, V_{REF1} and V_{REF2}. Figure 5(b) demonstrates the programmability of the mean values of the Gaussian-type curves. As the ratio of W_i/L_i is varied, the value of β_i changes as well, and the slopes of the Gaussian-type curve can be adjusted as needed. The output characteristic of the Gaussian-type curves with different



V_{th}=0.75V, I=10μA, V_{REF1}=1.9V, V_{REF2}=0.1V, W_1/L_1=30/4, W_2/L_2=10/4

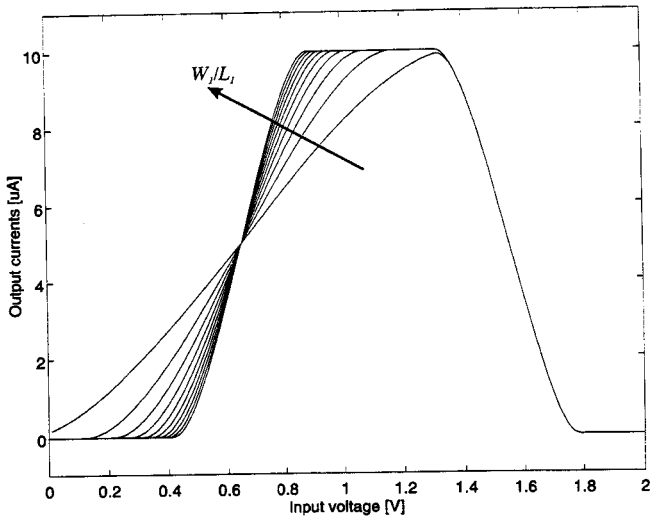
(a)



V_{th}=0.75V, I=10μA, V_{REF1}=1.9, 2.9, 3.9, 4.9, 5.9V, V_{REF2}=0.1, 1.1, 2.1, 3.1, 4.1V, W_1/L_1=15/4, W_2/L_2=15/4

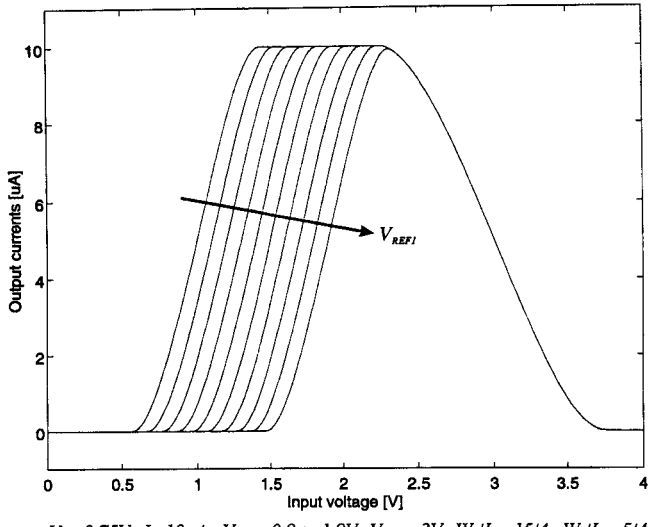
(b)

Fig. 5. (a) Characteristics of the transistor currents. (b) Simulation result with different mean values. (c) Simulation result with different W/L ratios for width control. (d) Simulation result with various differences in two reference voltages.



V_{in}=0.75V, I=10μA, V_{REF1}=2V, V_{REF2}=0.2V, W_1/L_1=5/4 to 50/4, W_2/L_2=50/4

(c)



V_{in}=0.75V, I=10μA, V_{REF1}=0.9 to 1.9V, V_{REF2}=3V, W_1/L_1=15/4, W_2/L_2=5/4

(d)

Fig. 5. (*Continued*)

W/L ratios is shown in Fig. 5(c). It depicts the programmability and availability of asymmetrical curves. If symmetrical curves are desired, then the sizes of M1 and M2 must match the sizes of M3 and M4 in the differential pairs. In this figure the characteristic of the curves with various sizes of the transistors in the

second balanced differential pair consisting of M3 and M4 is seen. Notice also from Fig. 5(c) that as the sizes of transistors in one differential pair increases, the output current becomes saturated at the value of the current source, and the shape of the output current characteristics approaches to a trapezoid. The programmability of the shape of the output current is also obtained by varying the difference of the reference voltages. This phenomenon is illustrated in Fig. 5(d). In this case, V_{REF1} is kept constant at 3 V, while V_{REF2} is varied from 0.9 V to 1.9 V with an increment of 0.1 V. As can be seen, the output current curve approaches a trapezoidal shape as the difference of the two reference voltages becomes larger.

3. Fuzzy Inference (Fuzzy Rule Evaluation) with Min-Max Operators

The most popular fuzzy logic functions which implement logical "AND" and logical "OR" are MIN and MAX, respectively. The result of the rule evaluation is a fuzzy output for each type of consequent action. Yamakawa[3] approached the design of min-max circuits using bipolar transistors in the emitter-coupled form. Because of the thermal drift and the 0.7 volt voltage shift of emitter junction produced at the output of the comparator, it is necessary to add an extra compensator to adjust the offset in his design. I. Baturone *et al.*[7] introduced both voltage- and current-mode min-max circuits. They employed DeMorgan's law to obtain min-max operators for the current-mode circuits and utilized the dual behavior of PMOS and NMOS transistors for the voltage-mode circuits. Although they improved the number of transistors required to perform each min and max operation to $3n+1$ from conventional $5n+1$ transistors[8] for n inputs, it would still consume a large area. The proposed design has basically a similar structure as given by Yamakawa, but it uses MOS transistors, instead of bipolar transistors, employed in the subthreshold mode of operation. It consists of a p-channel voltage follower for the min-selector circuit and an n-channel voltage follower for the max-selector circuit. The circuit schematics of the min-max operators are shown in Fig. 6. The min and max circuits also produce a small voltage shift. However, the shift compensation can be neglected since min and max circuits introduce the same magnitude of offset but in the opposite direction. As can be seen, the min- and max-circuit implementations complement each other. That is, the direction of the current sources are reversed from min circuit to max circuit, and vice versa. Whereas the conventional min-max circuits require $5n+1$ transistors[8] or $3n+1$ transistors[7] for n inputs to perform each operation, the proposed circuit structure requires only n transistors if the design of the current source is excluded, and even with the current source design it requires $n+4$ transistors. It leads to a smaller area and low power consumption.

The min circuit is configured as a two-dimensional array form to detect a smaller voltage of a set of two input voltages. That is, it functions such that

$$V_{min} = \min[V_1, V_2] + \delta V_{MIN\ shift} \qquad \text{with } \delta V_{MIN\ shift} > 0 \tag{11}$$

It is equivalent to finding the *intersection* of two fuzzy sets V_1 and V_2, $V_1 \cap V_2$.

$\delta V_{MIN\,shift}$ is a small voltage shift caused by a small voltage drop in the circuit. While the max operator functions such that

$$V_{max} = \max[V_1, V_2] - \delta V_{MAX\,shift} \qquad \text{with } \delta V_{MAX\,shift} > 0 \tag{12}$$
$$\text{with } |\delta V_{MAX\,shift}| \approx |\delta V_{MIN\,shift}|$$

and it is equivalent to finding the *union* of two fuzzy sets V_1 and V_2, $V_1 \cup V_2$.

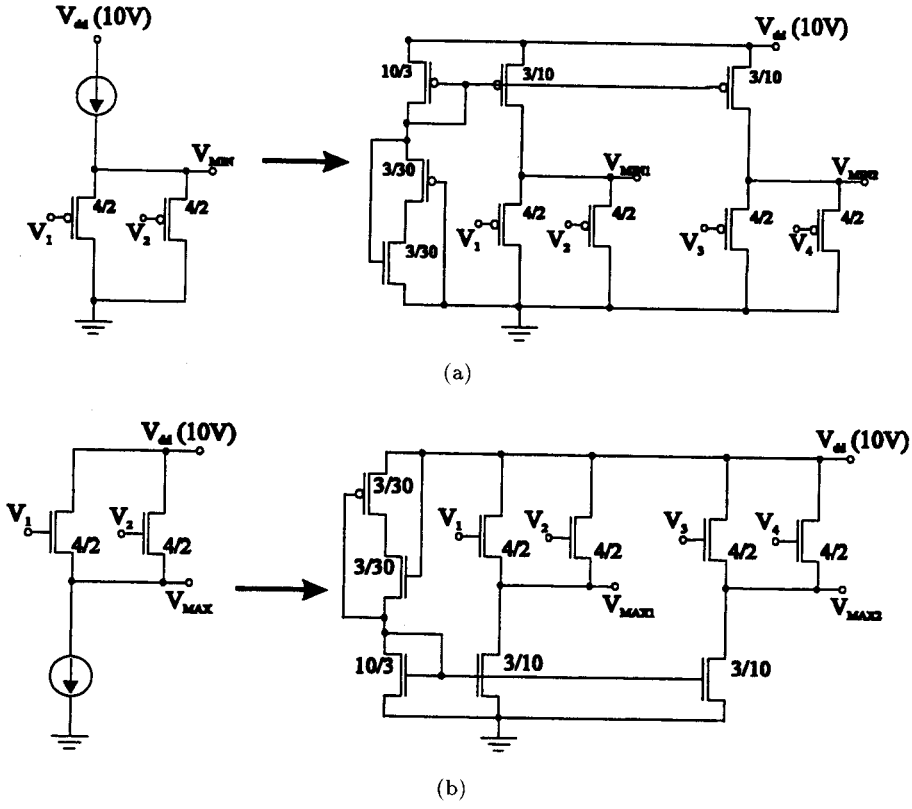
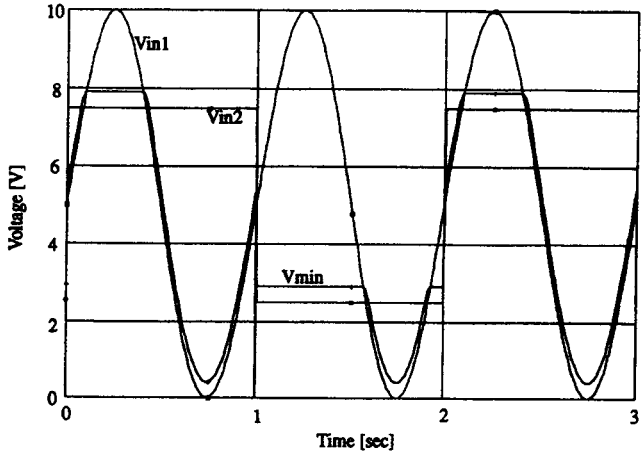
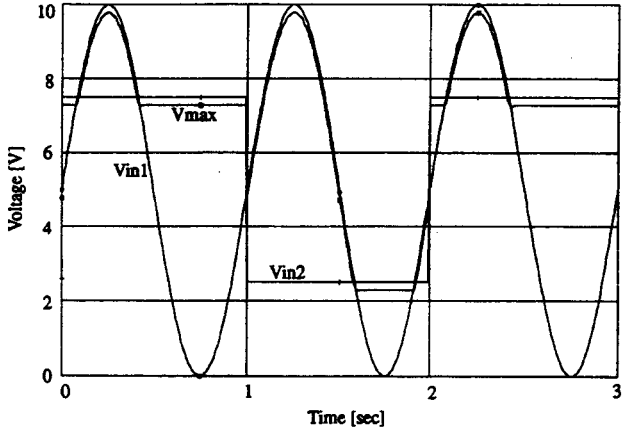


Fig. 6. Circuit schematics of the min-max operators. W/L ratios of each transistor are also shown. (a) Min circuit. (b) Max circuit.

The SPICE simulation of the min-max operators with two input voltages is shown in Fig. 7. Note that the positive and negative voltage shifts for the min and max circuits, respectively, compensate each other when the min and max circuits are connected in cascade. In other words, the overall offset in the min-max operators becomes negligible.



(a)



(b)

Fig. 7. SPICE simulation of the min-max operators. (a) Min circuit. (b) Max circuit.

4. Defuzzifier Block

The centroid, or the center of gravity (CG), method is simple and the most popular defuzzification method. Its algorithm can be expressed as

$$\text{C.G.} = \frac{\sum_{i=1}^{n} \mu(z)_i \cdot z_i}{\sum_{i=1}^{n} \mu(z)_i} \tag{13}$$

where n represents the number of fuzzy sets on the universe of discourse, and $\mu(z)_i$ and z_i represent the membership function and the weighting value of the ith fuzzy set, respectively. With the min-max fuzzy inference controller, Eq. (13) can be rewritten as

$$\text{C.G.} = \frac{\sum_{i=1}^{n} V_{MAX_i} \cdot z_i}{\sum_{i=1}^{n} V_{MAX_i}} \tag{14}$$

From a MOS analog circuit point of view, division has always been a costly operation in terms of time and area. B. D. Liu *et al.*[9] introduced a CMOS current-mode defuzzification circuit to compute a centroid. It is implemented by using the square-law MOS characteristics to compute the centroid. It gives high linearity and large dynamic range. However, its use is limited to only a current-mode to take an advantage of summation and multiplication (Ohm's law). Therefore, voltage-to-current (V-I) and current-to-voltage (I-V) conversions are necessary if the other components in a fuzzy controller are in a voltage-mode which would be simpler and more accurate because a sensitivity problem can be avoided. I. Baturone *et al.*[5] also introduced a current-mode singleton defuzzification circuit using four transistors which form the variable transresistance element. They also had to use V-I and I-V converters in their design, which seems to be redundant if everything is operated in voltage-mode. Many of the reported fuzzy controllers impose the condition that the denominator in expression (13) assumes the value 1 to avoid the division, or some constant value within global normalization loops.[3,8]

The strategy followed in the proposed design here is the use of a closed-loop feedback loop between the defuzzifier and fuzzifier blocks as shown in Fig. 8. The circuit schematic of the transconductance amplifier in Fig. 8 is shown in Fig. 9. As can be seen, simple resistive summers with operational amplifiers are used. The values of the external resistors are chosen freely based on the weighting values z_i, and hence they are externally programmable. The output currents from the output of the transconductance amplifier are fed into the membership function circuits, which shift output voltages of the Gaussian-type curves up or down depending on the amount of output feedback current as seen in Fig. 3(b). The purpose of the feedback is based on the principle of the global normalization to make the denominator in expression (13) constant. The transconductance amplifier circuit shown in Fig. 9 functions as follows. The denominator voltage is fed to the gate of transistor M6, and it is compared to a reference voltage which is applied to the gate of M7 in the differential pair. Thus, the denominator voltage which is a function of the max voltage, which in turn, is directly proportional to the output voltage of the membership function circuit, is compared to the reference voltage to minimize the difference in the gate voltages in the differential pair to avoid the division in the centroid calculation.

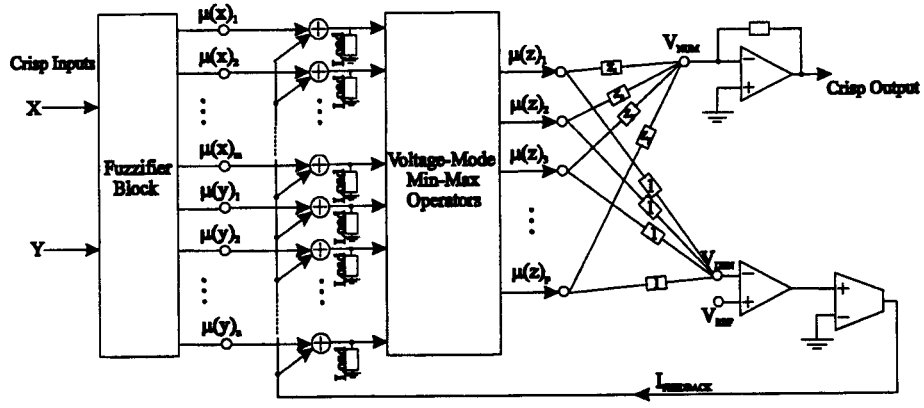


Fig. 8. Fuzzy min-max controller with a feedback loop and a defuzzifier which avoids a division in the centroid calculation.

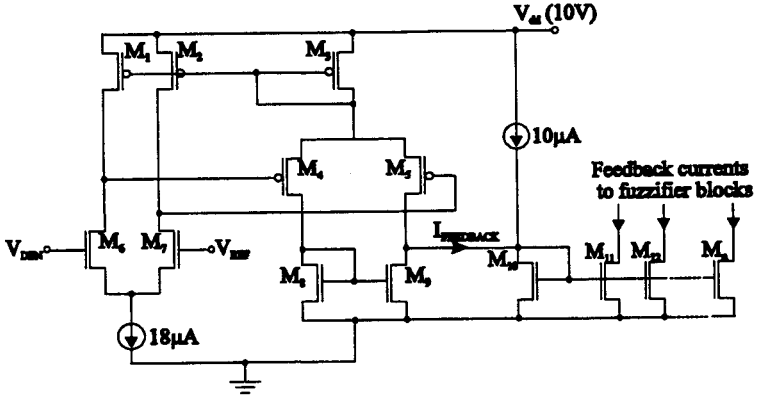


Fig. 9. Circuit schematic of the transconductance amplifier. The transistor sizes are all 3 μm/2 μm

5. Conclusions

A complete, programmable CMOS implementation of a min-max fuzzy controller has been developed. The proposed design is operated in voltage-mode and employs a closed-loop feedback between the fuzzifier and defuzzifier blocks. The feedback loop is controlled by the output current of the defuzzifier block which sources the input current of the membership function circuit. By using this concept, the output voltage of the fuzzifier circuit is shifted up or down depending upon the magnitude of the output current of the defuzzifier block, achieving the quasi-normalization of the denominator in the centroid calculation in expression (13). Thus, the troublesome division in the expression is avoided as well as I-V and V-I conversions which are seen in the conventional current-mode defuzzification circuits.

The main characteristics of the proposed architecture are reduced area costs, high operation capacity, simple inference, high precision, and low power consumption. Since the proposed fuzzy controller is designed for general purpose use, it can be used for any fuzzy-logic based controllers.

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