# CMOS IMPLEMENTATION OF A PULSE-CODED NEURAL NETWORK WITH A CURRENT CONTROLLED OSCILLATOR

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## ABSTRACT

This paper presents a compact architecture for CMOS implementation of a pulse-coded neural network with a current controlled oscillator. A computational style described in this paper mimics a biological neural system using pulse-stream signaling and analog summation and multiplication. Synaptic weights are multiplied by employing current mirrors and choosing proper $W/L$ ratios of output transistors of the pulse-coded neuron cell.

## 1. INTRODUCTION

In the vertebrate nervous system, communication between distant neurons is accomplished using encoded pulse streams. These biological neurons employ rapid pulses, called action potentials, for long distance transmission of signals. Neuron cells that fire action potentials typically fire either continuously or in bursts of several action potentials separated by quiescent periods. In biological neurons, information is sent in the form of *frequency modulated* pulse trains. The large fan-in and fan-out of most neurons, the wide variation in synaptic weights, the presence of both excitatory and inhibitory synapses on single neurons, and the complexity of the convolution of post- synaptic potentials make neurons computationally powerful devices.

Pulse-stream encoding technique [1]-[13] uses *digital* signals to carry information and control *analog* circuitry, while storing further analog information on the time axis. Main advantages of using a pulse-stream technique are that it is immune to noise and less susceptible to process variations between device.

A. Murray *et al.* [1] introduced a technique for generating pulses with a digital approach using a multiplexor and handshake RTT/RTR control transmission lines. Murray and A. Smith [2] developed a technique with a "chopping clock" signal that is asynchronous to all neural firing. It is logically "high" for exactly the correct fraction of time to allow the appropriate fraction of the presynaptic pulses through to multiply synaptic weights. Their weights, however, must be normalized for a proper operation. They also utilized digital circuitry to accomplish their design for neural and synaptic functional blocks. G. Moon *et al.* [4] introduced a neuron-type cell that encodes the information into the form of pulse duty cycles. The neuron-type cell structures three CMOS inverters for digitizing the pulse waves, where a threshold level is determined by an inverter logic threshold voltage. J. Meader *et al.* [5] presented a frequency- modulated pulse-firing circuit with a synapse electronic circuits using the threshold voltage of NMOS and floating- gate FETs. The threshold voltage of a floating-gate FET is adjustable in small steps via the application of programming pulses between the control gate and the substrate.

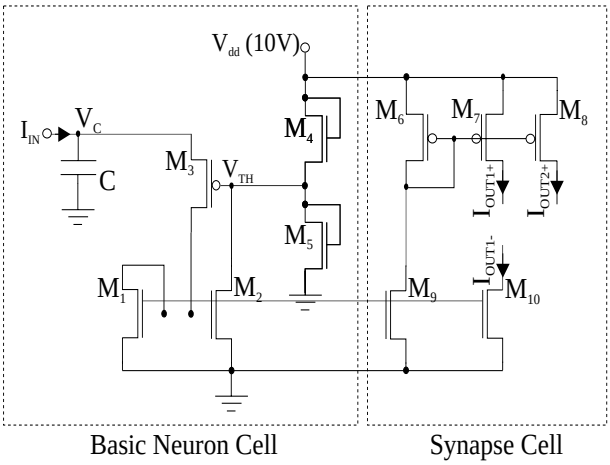


**Figure 1. Circuit schematic of the neuron and synapse cells.**

## 2. STRUCTURE OF A NEURON CIRCUIT

Inspired by biological models and advantages of hybrid pulse-stream neural networks, a simple integrated circuit structure for a neuron with synaptic weight multiplication and summation is described in this section. The neuron circuit shown in Fig. 1 is an electronic analogy of a biological soma; i.e., it initiates reactions, with a given external stimulus, by generating a stream of electrical pulse waves. In this case, the external stimulus is current. It also contains a synapse cell at the output of the neuron cell. As can be seen from the figure, the neuron cell consists of three MOS transistors (M1-M3), a pair of active resistors (M4 and M5), and a capacitor (C). The threshold level to the neuron cell is determined by the voltage divider consisting of the active resistors (M4 and M5). The neuron cell operates as follows. In a steady state, transistors M2 and M3, which form a "thyristor" subcircuit, are cut off. As the input $I_{IN}$ increases in time domain, the charge on the capacitor, and thus the capacitor voltage $V_C$, increases. When $V_C$ reaches a certain level and above, or when the gate voltage of M3 exceeds the threshold voltage, the transistors M2 and M3 change their state into active regions of operation and then causes saturation of M2. The saturation time for M2, which determines the output pulse width, is determined by the discharge time of the capacitor through M3. Thus, the out-

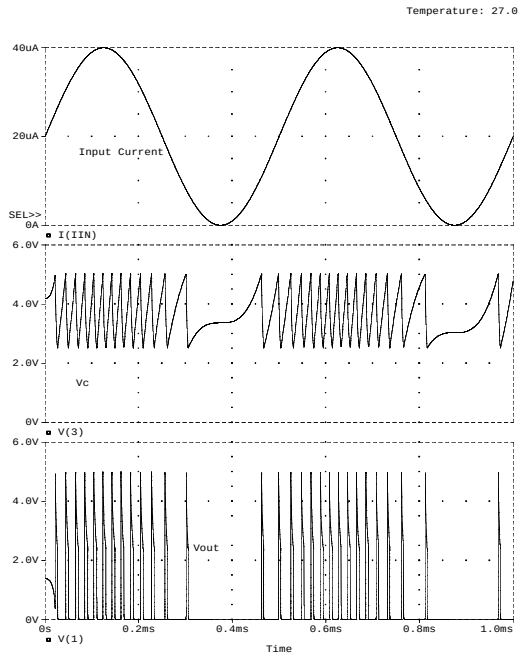


**Figure 2. SPICE simulated characteristic of the neuron cell circuit.**

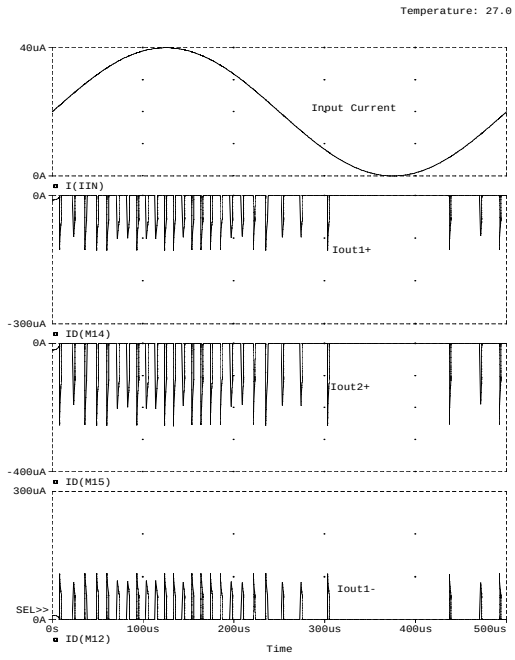


**Figure 3. SPICE simulated characteristic of the neuron cell with synaptic weight multiplication. For this simulation, $(W_8/L_8) = 2 \times (W_7/L_7)$ and $(W_{10}/L_{10}) = -1 \times (W_7/L_7)$.**

put starts to oscillate with a fixed height depending upon the capacitance on the capacitor and the input level. More specifically, the rate of the output oscillation increases as the amplitude of the current input or the capacitor voltage increases. Fig. 2 shows the SPICE simulated characteristic of the neuron cell with a sinusoidal current input. As can be seen from Fig. 2, the firing rate increases as the current input level increases. The firing rate varies from zero when net excitation lies below the firing-onset threshold to some saturating value, which illustrates the basic characteristic of nonlinear sigmoidal function normally seen in both biological and artificial neural networks.

There are two functions essential in a neural network – multiplication and addition. In digital systems these are well-defined functions, although they may be implemented in detail in several ways. In analog and pulse-stream systems, there is more than one generic approach to each operation. The operation of synaptic weight multiplication and summation in the proposed design can be achieved by an additional current mirror structure (M6-M10) at the output of the basic neuron cell, as seen in Fig. 1. For an *excitatory* synaptic weight multiplication, $p$-channel MOS current mirrors are used, and $n$-channel MOS current mirrors are used for an *inhibitory* synaptic weight multiplication in the circuit. The transistors in the proposed design are not biased in the subthreshold region so that a significant driving capability and faster signal processing can be achieved. In the strong-inversion region, the MOS transistors have a power-law dependence on the gate bias voltages. For MOS transistors operating in the saturation region, the drain currents are expressed using the quadratic approximation of Shichman-Hodges MOSFET model [14]. The $W/L$ ratios of the transistors in the synapse cell can be considered as a variable for synaptic weight multiplication. Synaptic weights are multiplied through the current mirrors and then summed together either to obtain output pulse stream or to apply to neuron cells on next neuron layer. Fig. 3 shows SPICE simulation result of the neuron circuit with two excitatory synapses and one inhibitory synapse.

## 3. EXAMPLE

In order to check the functionality of the neuron cell circuit design, a simple example is simulated with SPICE. An oscillatory 3-neuron Hopfield recurrent network is tested. Hopfield network [15] is a single layer recurrent neural network in which every neuron provides input to all others excluding itself. In addition, weights are symmetric; i.e., the weight of the synapse that connects the output of neuron $i$ to the input of neuron $j$, $w_{ij}$, is equal to the one of the synapse connecting the output of neuron $j$ to the input of neuron $i$, $w_{ji}$, with zero elements on the main diagonal ($w_{ij} = 0$ for $i = j$). For this 3-neuron Hopfield network whose interconnection topology shown in Fig. 4, there are $2^3 = 8$ possible input combinations. Let us assign a normalized synaptic weight matrix $\mathbf{W}$ and an input threshold vector $\mathbf{Y}$ as

$$\mathbf{W} = \begin{bmatrix} 0 & 1 & -1 \\ 1 & 0 & -1 \\ -1 & -1 & 0 \end{bmatrix} \tag{1}$$

$$\mathbf{Y} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{2}$$

Hopfield recurrent networks are particularly useful to solve

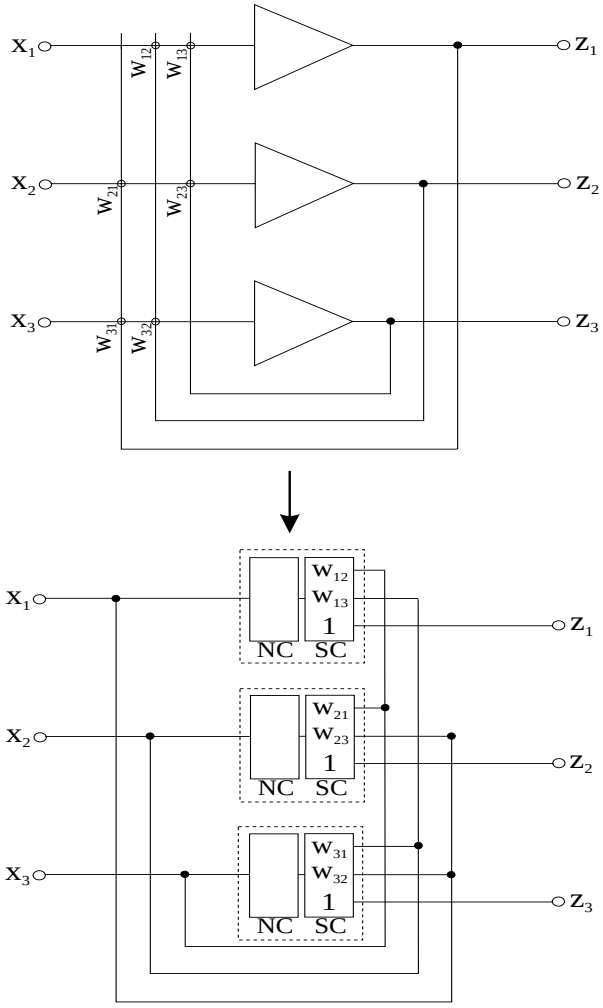


**Figure 4. Interconnection topology of the 3-neuron oscillatory Hopfield network with the proposed circuit (NC - neuron cell; SC - synapse cell).**

many optimization and linear programming problems. Table 1 summarizes the stable steady states obtained for all possible input combinations. Notice that the system either converges to a pattern *001* or to its complementary pattern *110*. Also note that the output is simply zero state and generates no oscillations, as expected, when all the inputs are not excited. This is simply the nature of the biological and artificial neural network and its computation system. The SPICE simulated transient response of the convergence to patterns *001* and *110* is illustrated in Figs. 5 and 6, respectively. Each one of them shows the input and output voltages of one of the neurons The simulations of a logical exclusive-OR function and a parity-3 function are also performed to verify the functionality of the proposed circuit design. The test results of these functions match the expected values respectably, and the functionality of the proposed circuit design is checked accordingly. Hence, it is also anticipated that the circuit design can be extended to a larger and more complex system and that it would function accordingly as well.

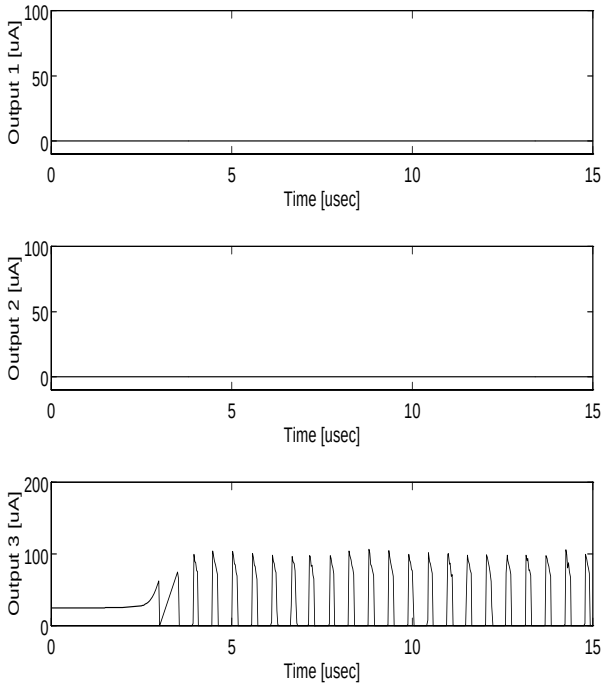


**Figure 5. SPICE result of the 3-neuron Hopfield network. Convergence to a pattern *001*.**

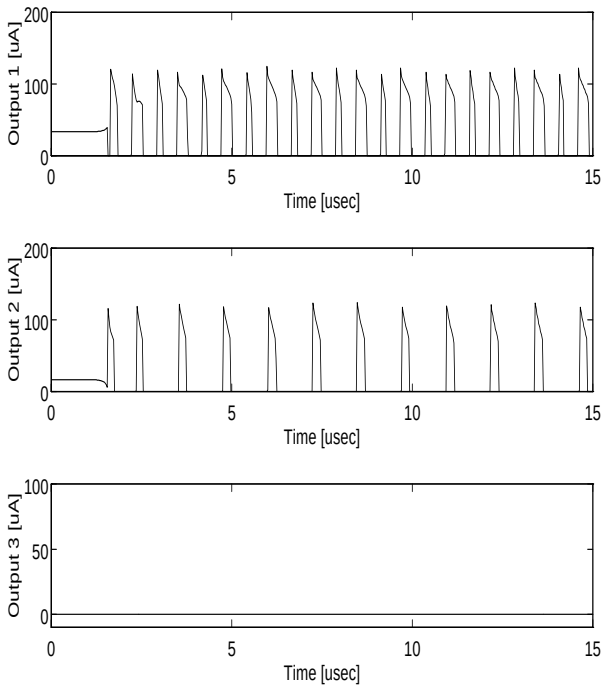


**Figure 6. SPICE result of the 3-neuron Hopfield network. Convergence to a pattern *110*.**

**Table 1. Simulation result of stable states for the 3-neuron oscillatory Hopfield network.**

| State # | Input Pattern | Output Pattern |
|---|---|---|
| 1 | 000 | 000 |
| 2 | 001 | 001 |
| 3 | 010 | 110 |
| 4 | 011 | 110 |
| 5 | 100 | 110 |
| 6 | 101 | 110 |
| 7 | 110 | 110 |
| 8 | 111 | 110 |

## 4. CONCLUSIONS

In this paper the CMOS hardware design to realize weighting and summing signals in our pulse-coded neural network with a current controlled oscillator has been introduced. In particular, a novel design and implementation of pulse-stream neural cell with synaptic weighting and summing capability is presented. Synaptic weight multiplication and summation are achieved by proper $W/L$ ratios of MOS transistors of the output current mirrors in the neuron circuit. The neuron circuit which has been developed here exhibits functional similarities to natural biological neurons. Our future goal is to develop programmable synapse circuits based on the proposed original structure.

## REFERENCES


[1] A. F. Murray, D. D. Corso, and L. Tarassenko, "Pulse-Stream VLSI Neural Networks Mixing Analog and Digital Techniques," *IEEE Trans. Neural Networks*, Vol. 2, No. 2, pp. 193-204, March 1991.

[2] A. F. Murray and A. V. W. Smith, "Asynchronous VLSI Neural Networks Using Pulse-Stream Arithmetic," *IEEE Journal Solid-State Circuits*, Vol. 23, No. 3, pp. 688-697, June, 1989.

[3] A. Hamilton, A. F. Murray, D. J. Baxter, S. Churcher, H. M. Reekie, and L. Tarassenko, "Integrated Pulse Stream Neural Network: Results, Issues, and Pointers," *IEEE Trans. Neural Networks*, Vol. 3, No. 3, pp. 385-393, May 1992.

[4] G. Moon, M. E. Zaghloul, R. W. Newcomb, "VLSI Implementation of Synaptic Weighting and Summing in Pulse Coded Neural-Type Cells," *IEEE Trans. Neural Networks*, Vol. 3, No. 3, 394-403, May 1992.

[5] J. L. Meador, A. Wu, C. Cole, N. Nintunze, and P. Chintrakulchai, "Programmable Impulse Neural Circuits," *IEEE Trans. Neural Networks*, Vol. 2, No. 1, pp. 101-109, January, 1991.

[6] A. F. Murray and L. Tarassenko, *Analogue Neural VLSI: A Pulse Stream Approach*, Chapman & Hall, London, UK, 1994.

[7] J. E. Tomberg and K. K. K. Kaski, "Pulse-Density Modulation Technique in VLSI Implementation of Neural Network Algorithms", *IEEE Journal Solid-State Circuits*, Vol. 25, No. 5, pp. 1277-1286, Oct. 1990.

[8] A. F. Murray, "Pulse Arithmetic in VLSI Neural Networks," *IEEE Micro Magazine*, pp. 64-74, Dec. 1989.

[9] T. G. Clarkson, C. K. Ng, and Y. Guan, "The pRAM: An Adaptive VLSI Chip," *IEEE Trans. Neural Networks*, Vol. 4, No. 3, pp. 408-412, May 1993.

[10] J. Donald and L. Akers, "An Adaptive Neural Processing Node," *IEEE Trans. Neural Networks*, Vol. 4, No. 3, pp. 413-426, May 1993.

[11] K. P. Roenker, A. P. Dhawan, and C. K. Song, "Electronic, Pulse-Mode Neural Circuits Based on a Novel Semiconductor Device," *Proc. Intelligent Engineering Systems Through Artificial Neural Net.*, ANNIE'94 Conf., St. Louis, Vol. 4, pp. 65-70, Nov. 1994.

[12] N. El-Leithy and R. W. Newcomb, "Overview of Neural-Type Electronics," *Proc. of the 28th Midwest Symposium on Circuits and Systems*, August, 1985.

[13] M. E. Zaghloul, J. L. Meador, and R. W. Newcomb, *Silicon Implementation of Pulse Coded Neural Networks*, Kluwer Academic Publ., Norwell, MA, 1994.

[14] H. Shichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits," *IEEE Journal Solid State Circuits*, Vol. SC-3, pp. 285-289, Sept. 1968.

[15] D. W. Tank and J. J. Hopfield, "Simple 'Neural' Optimization Networks: An A/D Converter, Signal Decision Circuit, and a Linear Programming Circuit," *IEEE Trans. Circuit and Systems*, Vol. 33, No. 5, May 1986.