CMOS Realization of a Pulse-Stream Artificial Neural Network using a Current Controlled Oscillator

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Abstract
This paper presents a compact and power efficient architecture for CMOS realization of a current-driven pulse-stream artificial neural network. The computational style described in this paper mimics a biological neural network using pulse-stream signaling and analog summation and multiplication. Synaptic weights are multiplied by employing current mirrors and choosing proper *W/L* ratios of output transistors of the pulse-coded neuron cell. The refractory period of action potentials is also considered and demonstrated in this paper.

I. Introduction

Neuron cells that fire action potentials typically fire either continuously or in bursts of several action potentials separated by quiescent periods. Because incoming pulses are summed with time, the neuron generates a pulse train with a higher frequency for higher positive excitation. Each neuron is characterized by nonexcitability for a certain time after the firing pulse, which is referred as the *refractory period.*

It was well into the 1930's before significant measurements of pulse-coded electrical activity in the brain had begun. The neuristor and its derivatives led to a large number of circuits being proposed for neural network realizations in the mid 1960s through the mid 1970s. The main results to come out of this research activity in the pulse-stream hardware area were the development of a bipolar circuit that acted as an action-potential-like-pulse generator by Wilamowski, *et al.* [1], its companion circuit by Newcomb, *et al.* [2], and a similar MOS circuit [3].

Pulse-stream encoding technique [4]-[14] uses digital signals to carry information and control analog circuitry, while storing further analog information on the time axis. Other advantages of using a pulse-stream technique are that it is immune to noise and less susceptible to process variations between device; thus, it is robust against the rigors of interchip communication. In a restricted sense, pulse-stream technique mimics the biological idea of neuron action using both analog and digital structures.

Several pulse-stream techniques were proposed by Murray *et al* [4]-[6]. The pulse duty cycle technique [6] uses weighting signals that are summed by means of switching CMOS transistors and a capacitor, and weighting on the pulse duty cycle is performed by a voltage-controlled resistor. A frequency modulated pulse-firing circuit with a programmable synapses using the threshold voltage of NMOS and floating-gate FETs is introduced [8]. The circuit uses the negative resistance characteristics of the MQW-IMD device was also introduced [9]. An adaptive neural processing node with on chip learning using the unsupervised weight modification rule [12] demonstrates the capability of producing linearly separable outputs that correspond to dominant features of the inputs. This study presents a simple but powerful circuit for pulse-mode neural networks.

II. CMOS Circuit Structure and Operation

The concept of the neuron cell circuit is shown as a simplified circuit in Fig. 1. The circuit structure is based on the current-driven simple neuron cell [10]. Transistors M1 and M3, which form a "thyristor" subcircuit, are normally cut off. For positive input current excitation the input voltage on capacitor C1 increases. When *V1* reaches a level above threshold voltage of transistor M1, the transistors M1, M2, and M3 become activated. Due to the positive closed-loop, all currents will rapidly increase leading to discharge of capacitor C1 toward negative supply voltage. The charge stored on C1 is the driving force in this pulse generation action. This state exists as long as C1 is not fully discharged. At this moment resistor R2 drives gate of M1 toward positive voltages and M1, and consequently M2 and M3, are turned off. After a pulse is generated, the voltage on capacitor C1 is low, and it is not possible to turn on transistor M1 because source node has large negative voltage and gate has close to zero potential. Then V1 voltage gradually approaches zero and reaches the steady-state condition. This recovery time is known as refractory period. If incoming signals are strong, a neuron can fire before steady state condition reaches. This effect of the refractory period dependence on input excitation is also observed in real neurons. The CMOS implementation of the neuron circuit is shown in Fig. 1(b). Resistors R1 and R2 are substituted by transistors M4 and M5. Transistor M2, M3 and multiple transistors MN form multiple outputs negative current sources.

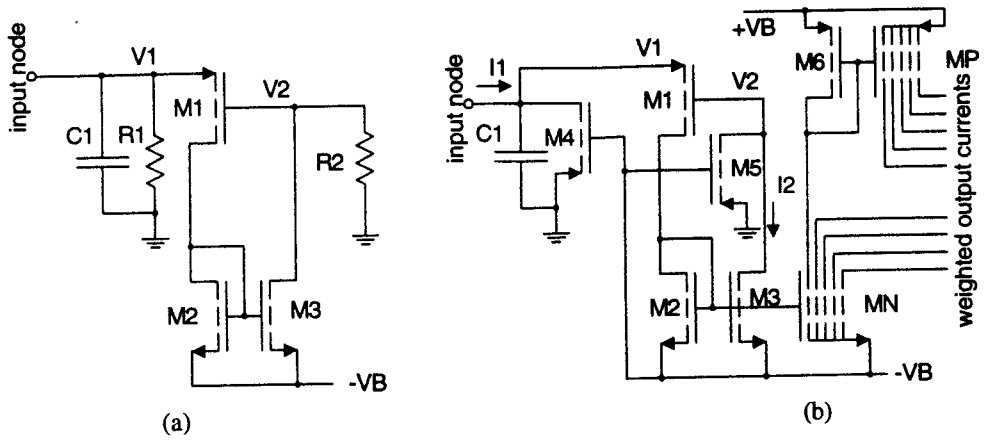

Fig. 1. Circuit diagram of neural cell: (a) concept diagram; (b) CMOS implementation.

Using M6 and MP the set of positive current sources are created. By choosing proper *W/L* ratios in MN and MP any positive or negative weighted current sources can be obtained. All transistors are off for most of the time, and they conduct currents only during existence of pulse. This way the circuit is very energy efficient.

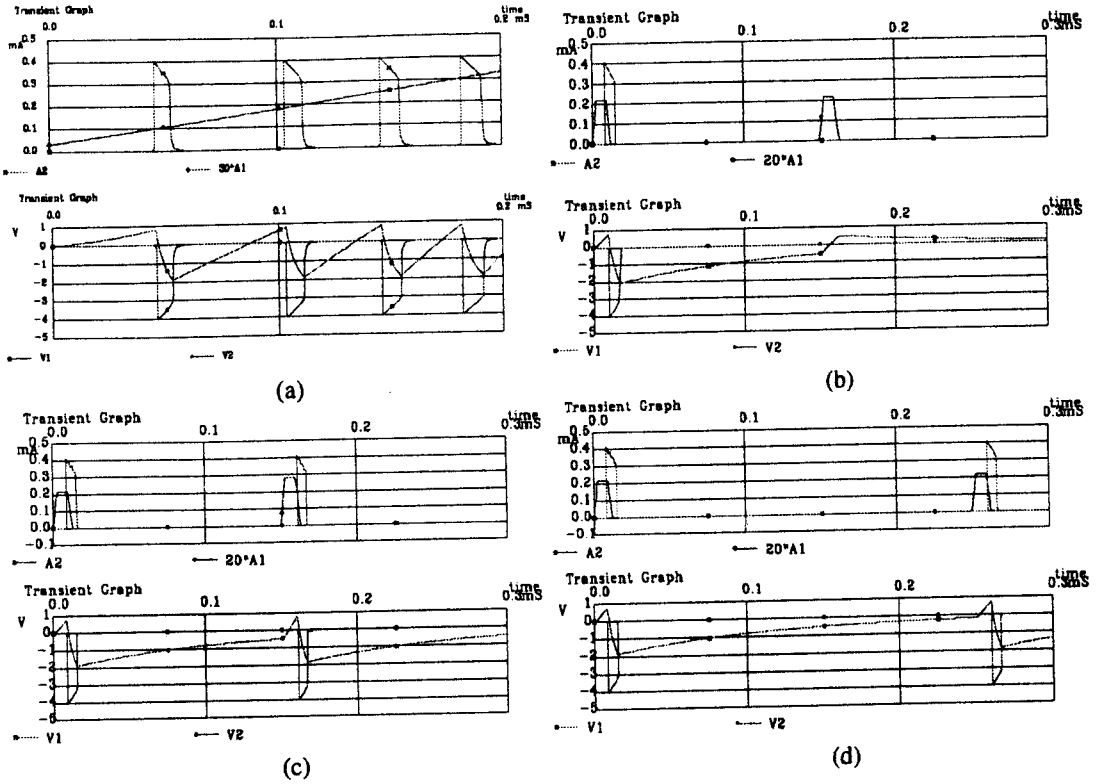

Fig. 2. Neuron circuit response for various excitations: (a) ramp input current; (b) two input current pulses too close to fire second pulse due to refractory period; (c) two input pulses well separated so the second pulse can fire neuron; and (d) the same pulse separation as in case (b) but due to the large magnitude of the second input pulse neuron is fired. Upper diagrams shows V1 and V2 voltages and lower diagrams shows input and output currents. Note that currents are drawn not to scale.

Fig. 2 shows the SPICE simulated characteristic of the neuron cell with a sinusoidal current input. As can be seen from this figure, the firing rate increases as the current input level increases. The same effect can be also observed in Fig. 3, where the neuron circuit is excited with raising input current. Lower diagrams in Fig. 2 show voltages on source and gate of M1. It can be clearly seen that neuron fires when input voltage reaches 0.75V threshold. Fig. 3 also shows that the firing frequency is a function of the strength of input excitation.

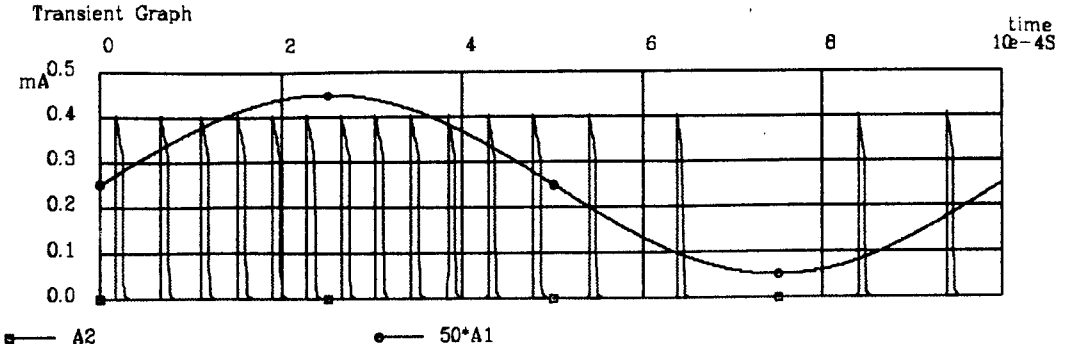

Fig. 3. Response of a neuron excited by the shifted sinusoidal current source.

III. Parity-3 Function as Network Example

This example illustrates the functionality of the proposed neuron circuit design with a parity-3 function which demonstrates a nonlinear mapping of a set of variables. For a parity-3 function, if the number of logic "1" (pulse firing action) inputs is odd, then the output is also assigned to a logic "1"; otherwise, the output is assigned to a logic "0" (no pulse firing action). The network structure with the synaptic weights is shown in Fig. 4. The neural network architecture and the synaptic weights for this example are obtained using the trainable functional link neural network (TFLNN) training technique [15]. TFLNN converges much quicker than some other existing network training methods by introducing hidden neuron units in the network architecture. The circuit simulation result is illustrated in Fig. 5. The circuit functions as expected and follows the nonlinear mapping patterns as required.

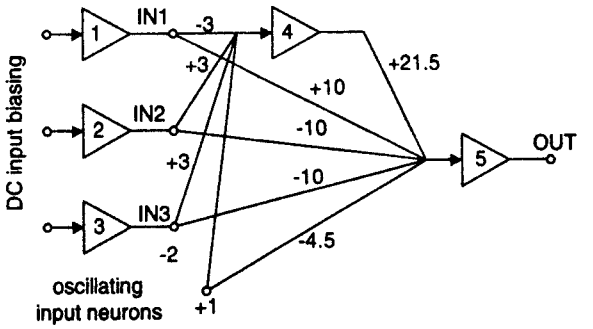

Fig. 4. Network structure for the parity-3 example.

IV. Conclusion

In this paper a CMOS hardware design to realize weighting and summing signals for pulse-stream neural networks is developed. In particular, implementation of a pulse-stream neural cell with synaptic weighting and summing capability is presented. The proposed neuron circuit has merit for hardware implementation due to its simple structure, small size, and high speed of operation. It also has a refractory period characteristic which is analogous to a natural biological neuron. Synaptic weight multiplication and summation are achieved by proper *W/L* ratios of MOS transistors of the output current mirrors in the synapse cell. The neuron cell circuit which has been developed here exhibits functional similarities to biological neurons through the demonstrated example. The circuit is very power efficient and uses a stored energy in C1 with incoming excitations to generate a pulse.

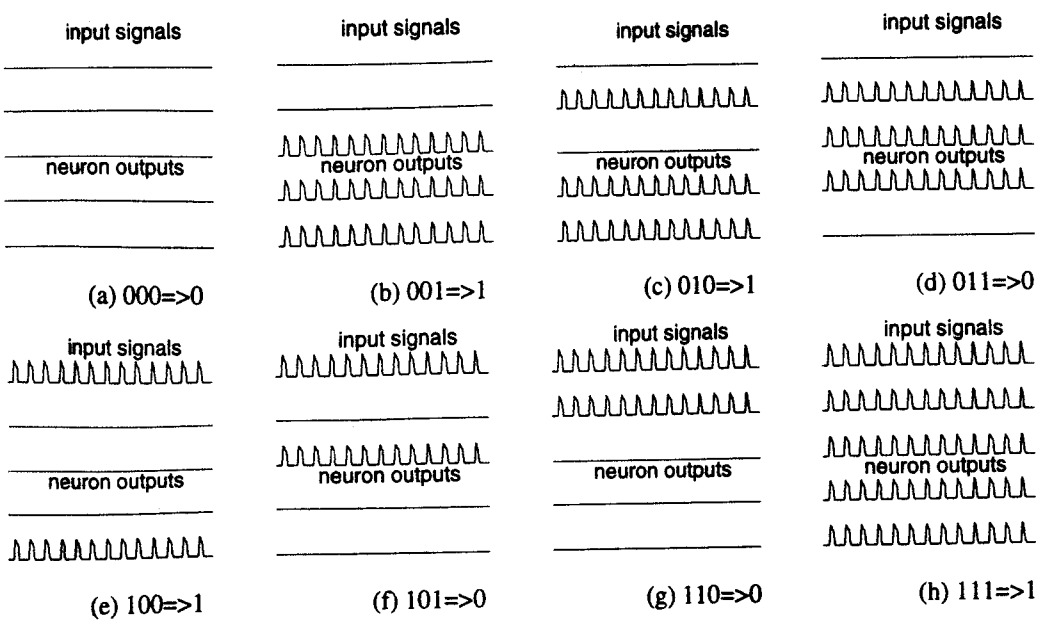

Fig. 5. Current waveforms on the outputs of neurons (1 through 5) obtained with the SPICE in the circuit of Fig. 4. First three neurons are converting DC signal into current pulse trains. Neurons 4 and 5 perform logical operation of parity-3.

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