56

Monolithic Device Models

B. M. Wilamowski
University of Wyoming

John Choma, Jr.
University of Southern California

Stephen I. Long
University of California Santa Barbara, CA

Nhat M. Nguyen
Hewlett Packard Company

Martin A. Brooke
Georgia Institute of Technology

56.1 Bipolar Junction Transistor

B. M. Wilamowski

The bipolar transistor is the most commonly used discrete active device. It has the highest transconductance among all transistors. Therefore, it can drive a reactive load with very high frequencies. The MOS transistor has a high switching speed only in integrated circuits, where parasitic capacitances are very small. The bipolar transistor also has some disadvantages. It requires a large area on the surface of integrated circuits. It has a relatively small input impedance and the switching speed is very much limited by the storage time of injected minority carriers.

In recent years the complexity of electronic circuits has increased significantly. Computer tools aid the design process. In a case of integrated circuits, computer-aided design is a necessity. Obviously the accuracy of design depends on the modeling accuracy. The knowledge of transistor models, and the understanding of model parameters is therefore essential.

Ebers–Moll Model

The bipolar transistor has three terminals: emitter, base, and collector. It consists of two junctions: the forward-biased emitter–base junction and the reverse-biased collector–base junction. Minority carriers injected from emitter to base are then extracted from the base by the reverse-biased

0-8493-8341-2/95/$0.00+$.50

collector junction. Therefore, the collector current is proportional to the emitter–base current. In the forward-active mode, the current–voltage characteristic of the emitter junction is described by the well-known diode equation

$$I_E = I_{EF} = I_{E0}\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right] \tag{56.1}$$

where I_{E0} is the emitter saturation current and $V_T = kT/q$ is the thermal potential (about 25 mV at room temperature). The collector current is always smaller than the emitter current $I_{CF} = \alpha_F I_{EF}$, where α_F is the forward current gain, which is smaller than unity.

The positions of the emitter and collector can be switched. The base–collector junction can become the forward-biased junction and the base–emitter junction can become the reverse-biased junction. In this reverse-active mode the collector current can be expressed by

$$I_C = I_{ER} = I_{C0}\left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1\right] \tag{56.2}$$

where I_{C0} is the collector saturation current. In a similar way, $I_{CR} = \alpha_R I_{ER}$, where α_R is the reverse current gain. When both junctions, the base–emitter and the base–collector, are forward biased, transistor operates in saturation mode and an equivalent transistor model is composed of two transistors operating in forward- and reverse-active modes, as Fig. 56.1 illustrates. The forward transistor operation is described by (56.1), and the reverse transistor operation is described by (56.2). From Kirchoff's current law one can write $I_C = I_{CF} - I_{ER}$, $I_E = I_{EF} - I_{ER}$, and $I_B = I_{BF} + I_{CR}$. Using (56.1) and (56.2) the emitter and collector currents can be described as

$$\begin{aligned} I_E &= a_{11}\left(\exp\frac{V_{BE}}{V_T} - 1\right) - a_{12}\left(\exp\frac{V_{BC}}{V_T} - 1\right) \\ I_C &= a_{21}\left(\exp\frac{V_{BE}}{V_T} - 1\right) - a_{22}\left(\exp\frac{V_{BC}}{V_T} - 1\right) \end{aligned} \tag{56.3}$$

which are known as the Ebers–Moll equations [1]. The Ebers–Moll coefficients a_{ij} are given as

$$a_{11} = I_{E0} \qquad a_{12} = \alpha_R I_{C0} \qquad a_{21} = \alpha_F I_{E0} \qquad a_{22} = I_{C0} \tag{56.4}$$

The Ebers–Moll coefficients are a very strong function of the temperature

$$a_{ij} = K_x T^m \exp\frac{V_{go}}{V_T} \tag{56.5}$$

where K_x is proportional to the junction area and independent of the temperature, $V_{go} = 1.21$ V is the potential gap in silicon (referenced to 0 K), and m is a material constant with a value between 2.5 and 4. When the transistor saturates, the current injection through the collector junction may activate parasitic transistors, where base acts as emitter, collector as base, and substrate as collector. In typical integrated circuits, bipolar transistors must not operate in saturation. Therefore, for the integrated bipolar transistor the Ebers–Moll equations can be simplified to the form

$$\begin{aligned} I_E &= a_{11}\left(\exp\frac{V_{BE}}{V_T} - 1\right) \\ I_C &= a_{21}\left(\exp\frac{V_{BE}}{V_T} - 1\right) \end{aligned} \tag{56.6}$$

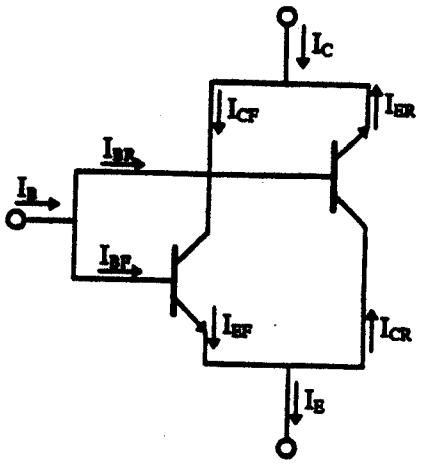

FIGURE 56.1 The equivalent circuit of the bipolar transistor for forward, reverse, and saturated modes.

where $a_{21}/a_{11} = \alpha_F$. This equation corresponds to the circuit diagram as shown in Fig. 56.1, but without the reverse transistor.

Circuit-Level Gummel–Poon Model

In real bipolar transistors the current–voltage characteristics are more complex than those described by the Ebers–Moll equations. Typical current–voltage characteristics of the bipolar transistor, plotted in semilogarithmic scale, are shown in Fig. 56.2. At small base–emitter voltages, due to the generation–recombination phenomena, the base current is proportional to

$$I_{BL} \propto \exp \frac{V_{BE}}{2V_T} \tag{56.7}$$

Also, due to the base conductivity modulation at high-level injections, the collector current for larger voltages can be expressed by the similar relation

$$I_{CH} \propto \exp \frac{V_{BE}}{2V_T} \tag{56.8}$$

Note, that the collector current for wide range is given by

$$I_C = I_s \exp \frac{V_{BE}}{V_T} \tag{56.9}$$

The saturation current is a function of device structure parameters

$$I_s = \frac{qAn_i^2 V_T \mu_B}{\int_0^{w_B} N_B(x)\,dx} \tag{56.10}$$

where $q = 1.6 \cdot 10^{-19}$ C is the electron charge, A is the emitter–base junction area, n_i is the intrinsic concentration ($n_i = 1.5 \cdot 10^{10}$ at 300 K), μ_B is the mobility of the majority carriers in the transistor base, w_B is the effective base thickness, and $N_B(x)$ is the distribution of impurities in the base. Note that the saturation current is inversely proportional to the total impurity dose in the base. In the transistor with the uniform base, the saturation current is given by

$$I_s = \frac{qAn_i^2 V_T \mu_B}{w_B N_B} \tag{56.11}$$

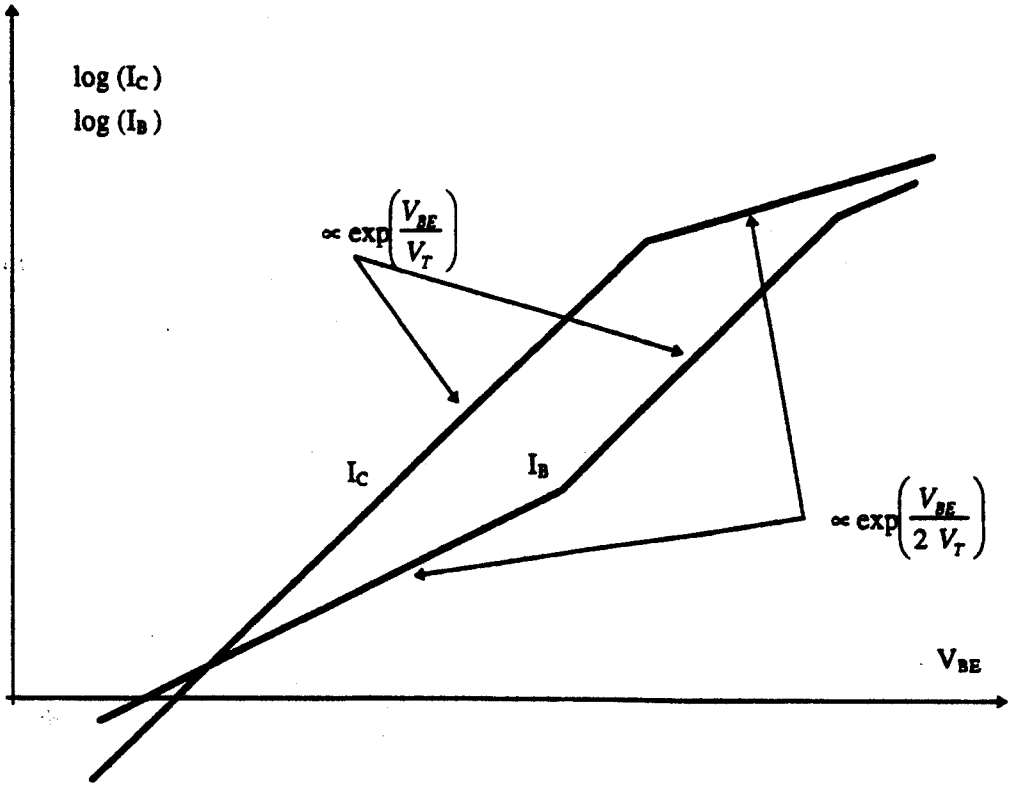

FIGURE 56.2 Collector and base currents as a function of base–emitter voltage.

When a transistor operates in the reverse-active mode (emitter and collector are switched) then the current of such biased transistor is given by

$$I_E = I_s \exp \frac{V_{BC}}{V_T} \tag{56.12}$$

Note that the I_s parameter is the same for forward and reverse mode of operation. The Gummel–Poon transistor model [2] was derived from the Ebers–Moll model using the assumption that $a_{12} = a_{21} = I_s$. For the Gummel–Poon model (56.3) is simplified to the form

$$\begin{aligned} I_E &= I_s \left(\frac{1}{\alpha_F} \exp \frac{V_{BE}}{V_T} - \exp \frac{V_{BC}}{V_T} \right) \\ I_C &= I_s \left(\exp \frac{V_{BE}}{V_T} - \frac{1}{\alpha_R} \exp \frac{V_{BC}}{V_T} \right) \end{aligned} \tag{56.13}$$

These equations require only three coefficients, while the Ebers–Moll requires four. The saturation current I_s is constant for a wide range of currents. The current gain coefficients α_F and α_R have values smaller, but close to unity. Often, instead of using the current gain as $\alpha = I_C/I_E$, the current gain β as a ratio of the collector current to use the base current $\beta = I_C/I_B$ is used. The mutual relationships between α and β coefficients are given by

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \quad \beta_F = \frac{\alpha_F}{1 - \alpha_F} \quad \alpha_R = \frac{\beta_R}{\beta_R + 1} \quad \beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{56.14}$$

The Gummel–Poon model was implemented in SPICE [3] and other computer programs for circuit analysis. To make the equations more general, the material parameters η_F and η_R were

introduced

$$I_C = I_s \left[\exp \frac{V_{BE}}{\eta_F V_T} - \left(1 + \frac{1}{\beta_R}\right) \exp \frac{V_{BC}}{\eta_R V_T} \right] \tag{56.15}$$

The values of η_F and η_R vary from one to two.

Current Gains of Bipolar Transistors

The transistor current gain β is limited by two phenomena: base transport efficiency and emitter injection efficiency. The effective current gain β can be expressed as

$$\frac{1}{\beta} = \frac{1}{\beta_I} + \frac{1}{\beta_T} + \frac{1}{\beta_R} \tag{56.16}$$

where β_I is the transistor current gain caused by emitter injection efficiency, β_T is the transistor current gain caused by base transport efficiency, and β_R is the recombination component of the current gain. As one can see from (56.16), smaller values of β_I, β_T, and β_R dominate. The base transport efficiency can be defined as a ratio of injected carriers into the base, to the carriers that recombine within the base. This ratio is also equal to the ratio of the minority carrier lifetime, to the transit time of carriers through the base. The carrier transit time can be approximated by an empirical relationship

$$\tau_{\text{transit}} = \frac{w_B^2}{V_T \mu_B (2 + 0.9\eta)} \qquad \eta = \ln\left(\frac{N_{BE}}{N_{BC}}\right) \tag{56.17}$$

where μ_B is the mobility of the minority carriers in base, w_B is the base thickness, N_{BE} is the impurity doping level at the emitter side of the base, and N_{BC} is the impurity doping level at the collector side of the base. Therefore, the current gain due to the transport efficiency is

$$\beta_T = \frac{\tau_{\text{life}}}{\tau_{\text{transit}}} = (2 + 0.9\eta)\left(\frac{L_B}{w_B}\right)^2 \tag{56.18}$$

where $L_B = \sqrt{V_T \mu_B \tau_{\text{life}}}$ is the diffusion length of minority carriers in the base.

The current gain β_I due to the emitter injection efficiency is given

$$\beta_I = \frac{\mu_B \int_0^{w_E} N_{E\text{eff}}(x)\,dx}{\mu_E \int_0^{w_B} N_B(x)\,dx} \tag{56.19}$$

where μ_B and μ_E are minority carrier mobilities in the base and in the emitter, respectively, $N_B(x)$ is impurity distribution in the base, and $N_{E\text{eff}}$ is the effective impurity distribution in the emitter.

The recombination component of current gain β_R is caused by the different current–voltage relationship of base and collector currents, as can be seen in Fig. 56.2. The slower base current increase is due to the recombination phenomenon within the depletion layer of the base–emitter junction. Since the current gain is the ratio of the collector current to the base current, the relation for β_R can be found as

$$\beta_R = K_{R0} I_C^{1-(1/\eta_R)} \tag{56.20}$$

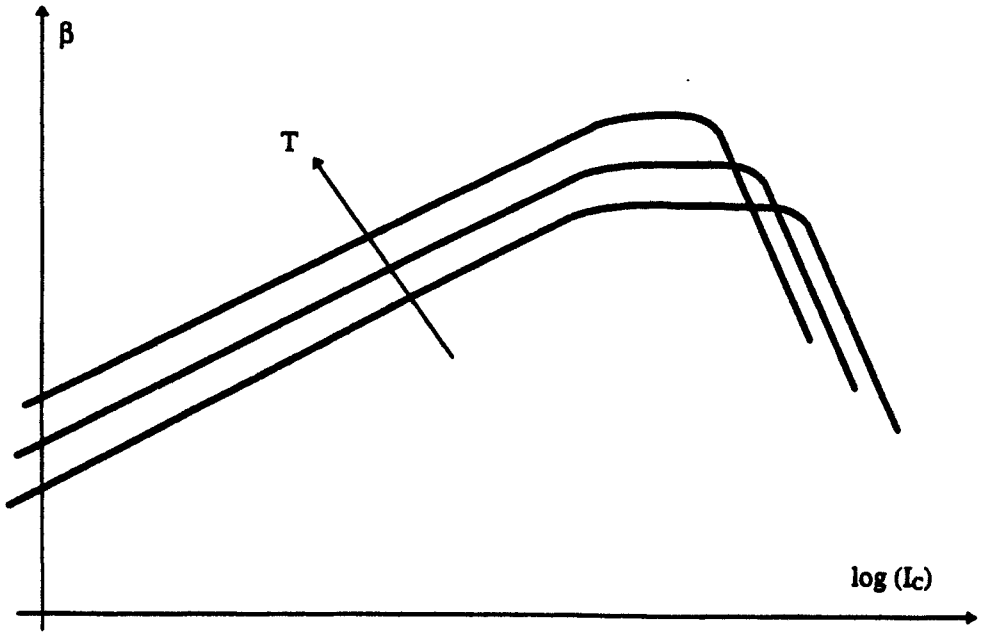

FIGURE 56.3 The current gain β as the function of the collector current.

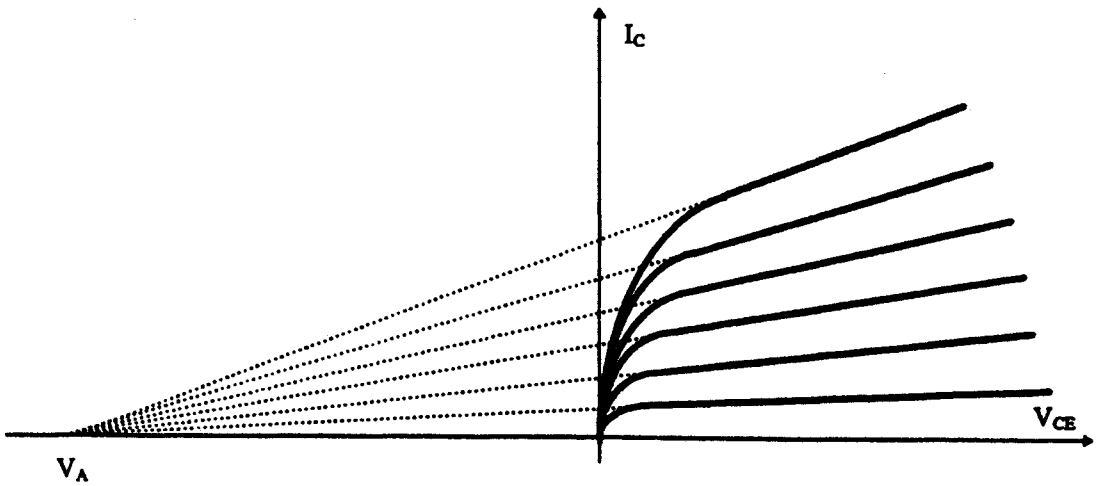

FIGURE 56.4 Current–voltage characteristics of a bipolar transistor.

As can be seen from Fig. 56.2, the current gain β is a function of the current. This gain–current relationship is illustrated in Fig. 56.3. The range of a constant current gain is wide for bipolar transistors with a technology characterized by a lower number of generation–recombination centers.

With an increase of collector–base voltage, the depletion layer penetrates deeper into the base. Therefore, the effective thickness of the base decreases. This leads to an increase of transistor current gain with applied collector voltages. Figure 56.4 illustrates this phenomenon, which is known as Early's effect. The extensions of transistor characteristics (dotted lines in Fig. 56.4) are crossing the voltage axis at the point $-V_A$, where V_A is known as the Early voltage. The current gain β, as a function of collector voltage, is usually expressed using the relation

$$\beta = \beta_o \left(1 + \frac{V_{CE}}{V_A}\right) \tag{56.21}$$

A similar equation can be defined for the reverse mode of operation.

High-Current Phenomena

The concentration of minority carriers increases with the rise of transistor currents. When the concentration of moving carriers exceeds a certain limit, the transistor property degenerates. Two phenomena are responsible for this limitation. The first is related to the high concentration of moving carriers (electrons in the npn transistor) in the base–collector depletion region. This is known as the Kirk effect. The second phenomenon is caused by a high level of carriers injected into the base. When the concentration of injected minority carriers in the base exceeds the impurity concentration there, then the base conductivity modulation limits the transistor performance.

To understand the Kirk effect, consider the npn transistor in forward-active mode with the base–collector junction reverse biased. The depletion layer consists of the negative lattice charge of the base region and the positive lattice charge of the collector region. Boundaries of the depletion layer are such that the total positive and negative charges are equal. When a collector current carrying negatively charged electrons flows through the junction, the effective negative charge on the base side of junction increases. Also, the positive lattice charge of the collector side of the junction is compensated by the negative charge of moving electrons. This way, the collector–base space–charge region moves toward the collector, resulting in a thicker effective base. With a large current level, the thickness of the base may be doubled or tripled. This phenomenon, known as the Kirk effect, becomes very significant when the charge of moving electrons exceeds the charge of the lightly doped collector N_C. The threshold current for the Kirk effect is given by

$$I_{\max} = qAv_{\text{sat}}N_C \tag{56.22}$$

where v_{sat} is saturation velocity for electrons ($v_{\text{sat}} = 10^7$ cm/s for silicon).

The conductivity modulation in the base, or high-level injection, starts when the concentration of injected electrons into the base exceeds the lowest impurity concentration in the base $N_{B\min}$. This occurs for the collector current $I_{\max}$ given by

$$I_{\max} < qAN_{B\max}v = \frac{qAV_T\mu_B N_{B\max}(2+0.9\eta)}{w_B} \tag{56.23}$$

The above equation is derived using (56.17), for estimation of the base transient time.

The high-current phenomena are significantly enlarged by the current crowding effect. The typical cross section of a bipolar transistor is shown in Fig. 56.5. The horizontal flow of the base current results in the voltage drop across the base region under the emitter. This small voltage difference on the base–emitter junction causes a significant difference in the current densities at the junction. This is due to the very nonlinear junction current–voltage characteristics. As a result, the base–emitter junction has very nonuniform current distribution across the junction. Most of the current flows through the part of the junction closest to base contact. For transistors with larger emitter areas, the current crowding effect is more significant. This nonuniform transistor current distribution makes the high-current phenomena, such as the base conductivity modulation and the Kirk effect, start for smaller currents than given by (56.22) and (56.23). The current crowding effect is also responsible for the change of the effective base resistance with a current. As a base current increases, the larger part of emitter current flows closer to the base contact, and the effective base resistance decreases.

Small-Signal Model

Small-signal transistor models are essential for ac circuit design. The small-signal equivalent circuit of the bipolar transistor is shown in Fig. 56.6(a). The lumped circuit shown in Fig. 56.6(a)

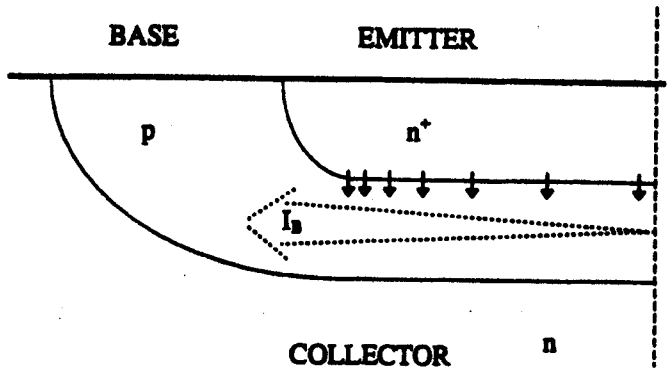

FIGURE 56.5 Current crowding effect.

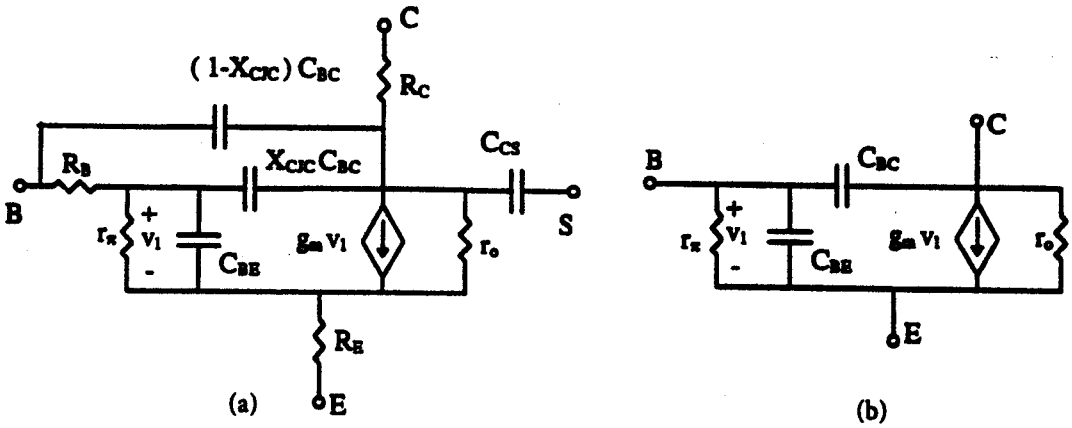

FIGURE 56.6 Bipolar transistor equivalent diagrams: (a) SPICE model, (b) simplified model.

is only an approximation. In real transistors, resistances and capacitances have a distributed character. For most design tasks, this lumped model is adequate, or even the simple equivalent transistor model shown in Fig. 56.6(b) can be considered. The small-signal resistances r_π and r_o are inversely proportional to the transistor currents, and the transconductance g_m is directly proportional to the transistor currents

$$r_\pi = \frac{\eta_F V_T}{I_B} = \frac{\eta_F V_T \beta_F}{I_C} \qquad r_o = \frac{V_A}{I_C} \qquad g_m = \frac{I_C}{\eta_F V_T} \tag{56.24}$$

where η_F is the forward emission coefficient, ranging from 1.0 to 2.0, and V_T is the thermal potential ($V_T = 25$ mV at room temperature). Equations similar to (56.24) can be written for the reverse transistor operation as well.

The series base, emitter, and collector resistances R_B, R_E, and R_C, respectively, are usually neglected for simple analysis [Fig. 56.6(b)]. However, for high-frequency analysis it is essential to use at least the base series resistance R_B. The series emitter resistance R_E usually has a constant bias-independent value. The collector resistance R_C may significantly vary with the biasing current. The value of the series collector resistance may be lowered by one or two orders of magnitude if the collector junction becomes forward biased. A large series collector resistance may force the transistor into the saturation mode. Usually however, when the collector–emitter voltage is large enough, the effect of collector resistance is not significant. The SPICE model assumes a constant value for the collector resistance R_C.

The series base resistance R_B may significantly limit the transistor performance at high frequencies. Due to the current crowding effect and the base conductivity modulation, the series

base resistance is a function of the collector current I_C [4].

$$R_B = R_{B\min} + \frac{R_{B0} - R_{B\min}}{0.5 + \sqrt{0.25 + \dfrac{i_C}{I_{KF}}}} \tag{56.25}$$

where I_{KF} is β_F high-current roll-off current, R_{B0} is the base resistance at very small currents, and $R_{B\min}$ is the minimum base resistance at high currents. Another possible approximation of the base series resistance R_B as a function of the base current I_B is [4]

$$R_B = 3(R_{B0} - R_{B\min})\frac{\tan z - z}{z \tan^2 z} + R_{B\min} \qquad z = \frac{\sqrt{1 + \dfrac{1.44 I_B}{\pi^2 I_{RB}}} - 1}{\dfrac{24}{\pi^2}\sqrt{\dfrac{I_B}{I_{RB}}}} \tag{56.26}$$

where I_{RB} is the base current for which the base resistance falls halfway to its minimum value.

The base–emitter capacitance C_{BE} is composed of two terms: the diffusion capacitance, which is proportional to the collector current, and the depletion capacitance, which is a function of the base–emitter voltage V_{BE}. The C_{BE} capacitance is given by

$$C_{BE} = \tau_F \frac{I_C}{\eta_F V_T} + C_{JE0}\left(1 - \frac{V_{BE}}{V_{JE0}}\right)^{-m_{JE}} \tag{56.27}$$

where V_{JE0} is the base–emitter junction potential, τ_F is the base transit time for forward direction, C_{JE0} is base–emitter zero-bias junction capacitance, and m_{JC} is the base–emitter grading coefficient.

The base–collector capacitance C_{BC} is given by a similar expression as (56.27). In the case when the transistor operates in forward-active mode, it can be simplified to

$$C_{BE} = C_{JC0}\left(1 - \frac{V_{BC}}{V_{JC0}}\right)^{-m_{JC}} \tag{56.28}$$

where V_{JC0} is the base–collector junction potential, C_{JC0} is the base–collector zero-bias junction capacitance, and m_{jc} is the base–collector grading coefficient.

In the case when the bipolar transistor is in the integrated form, the collector–substrate capacitance C_{CS} has to be considered

$$C_{CS} = C_{JS0}\left(1 - \frac{V_{CS}}{V_{JS0}}\right)^{-m_{JS}} \tag{56.29}$$

where V_{JS0} is the collector–substrate junction potential, C_{JS0} is the collector–substrate zero-bias junction capacitance, and m_{JS} is the collector–substrate grading coefficient.

When the transistor enters saturation, or it operates in reverse-active mode, (56.27) and (56.28) should be modified to

$$C_{BE} = \tau_F \frac{I_S \exp\left(\dfrac{V_{BE}}{\eta_F V_T}\right)}{\eta_F V_T} + C_{JE0}\left(1 - \frac{V_{BE}}{V_{JE0}}\right)^{-m_{JE}} \tag{56.30}$$

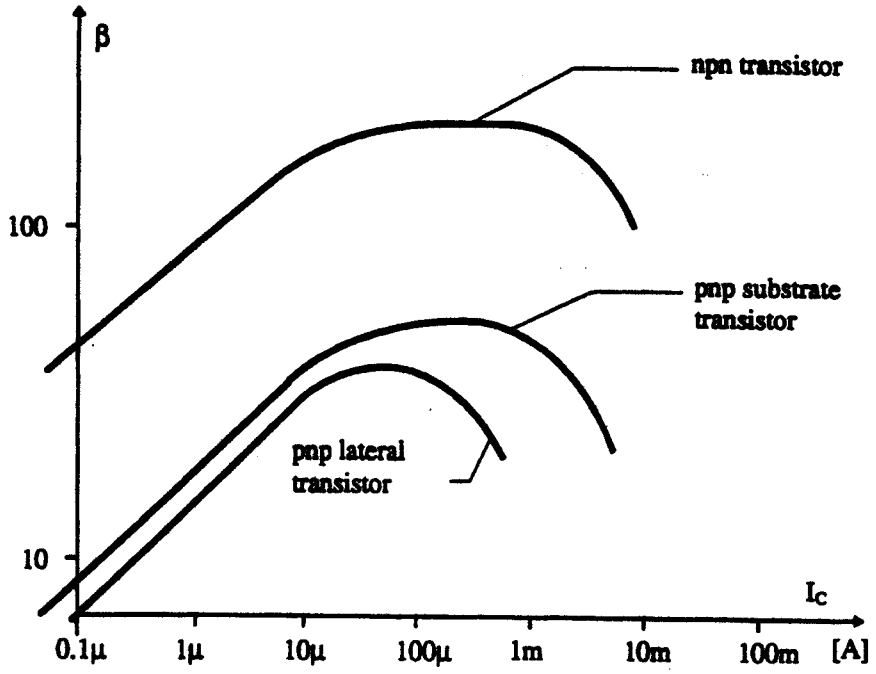

FIGURE 56.10 Transistor current gain versus collector current for npn and pnp transistors.

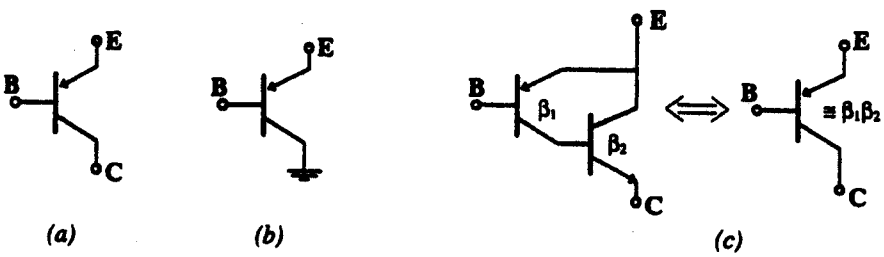

FIGURE 56.11 Integrated pnp transistors: (a) lateral transistor, (b) substrate transistor, (c) composed transistor.

and collector fabrication. The vertical transistor shown in Fig. 56.9(b) used the p-type base layer for emitter, and the p-type substrate as collector. This transistor is sometimes known as the substrate transistor. In both transistors the base is made of the n-type epitaxial layer. Such transistors with a uniform and thick base are slow. Also, the current gain β of such transistors is small. Figure 56.10 illustrates typical current gains β as a function of collector currents for npn and pnp transistors. Maximum current gain of the lateral transistor is about 30, and in the substrate transistor maximum β is about 50. Note that the vertical transistor has the collector shorted to the substrate, as Fig. 56.9(b) and 56.11(b) illustrates. When a pnp transistor with a large current gain is required, then the concept of the composite transistor can be implemented. Such a composite transistor, known also as the superbeta transistor, consists of a pnp lateral transistor, and the standard npn transistor connected as shown in Fig. 56.11(c). The composed transistor acts as the pnp transistor and it has a current gain β approximately equal to $\beta_{pnp}\beta_{npn}$.

Advanced Bipolar Integrated Circuit Fabrication

The modern bipolar process uses ion implantation for base and emitter fabrication. The emitter and base thicknesses can be as low as 0.1 μm. Also, horizontal dimensions are reduced significantly. This is possible due to the selective oxidation technique, which reduces parasitic capacitances and allows for mask self alignment. The structure of the modern bipolar transistor is shown in Fig. 56.12, and its impurity profile in Fig. 56.13.

The popular MOS integrated circuits are very fast only if the parasitic capacitances are very small. Indeed, inside integrated circuits these capacitances are on the order of fF(10^{-15} F) and

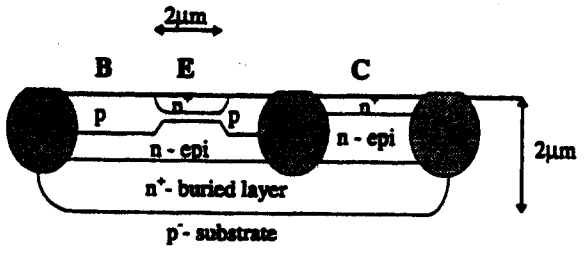

FIGURE 56.12 Structure of modern npn transistor fabricated using ion implantation and selective oxidation process.

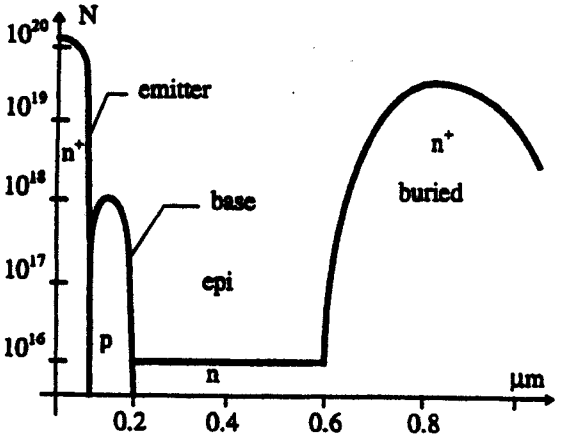

FIGURE 56.13 Impurity profile in modern bipolar transistor.

the switching times of transistors operating with a single μA range are in single ns range. The problem arises when signals have to be transmitted outside the integrated circuits, where loading capacitances are in the pF range (1000 times larger). With the same device construction the switching time will be reduced by a factor of 1000. To overcome this problem a special chain of power MOS transistors is used in output buffers. This is a costly solution. Occasionally those output buffers consume more space of integrated circuits than the functional circuitry. Another approach is to use BiCMOS technology, where bipolar transistors are used as output buffers. In this case, the high current driving capabilities of the bipolar transistors are utilized. The bipolar transistor in BiCMOS technology has a similar structure, as shown in Fig. 56.12. In BiCMOS technology, both bipolar and MOS transistors are fabricated on the same wafer. Once the bipolar transistors are introduced into the CMOS process, they are then used for another circuitry other than buffers.

Typical Parameters of Integrated Bipolar Transistors

Various types of transistors can be fabricated using integrated circuit technologies. Typical parameters of some bipolar integrated transistors are shown in Table 56.1.

Model Parameters

It is essential to use proper transistor models in computer-aided design tools. The accuracy of simulation results depends on the model accuracy, and on the values of the model parameters used. In this section the thermal sensitivity and second-order effects in the transistor model are discussed. The SPICE bipolar transistor model parameters are also discussed.

Thermal Sensitivity

All parameters of the transistor model are temperature dependent. Some parameters are very strong functions of temperature. To simplify the model description, the temperature dependence of some parameters are often neglected. In this section, the temperature dependence of the transistor model is described based on the model of the SPICE program [3]–[5]. Deviations from the actual temperature dependence will also be discussed. The temperature dependence of

At high frequencies the phase of the collector current shifts. This phase shift is computed in the SPICE program in the following way:

$$I_C(\omega) = I_C \exp(j\omega P_{TF}\tau_F) \tag{56.44}$$

where P_{TF} is a coefficient for excess phase calculation.

Noise is usually modeled as the thermal noise for parasitic series resistances, and as shot and flicker noise for collector and base currents

$$\overline{i_R^2} = \frac{4kT\,\Delta f}{R} \tag{56.45}$$

$$\overline{i_B^2} = \left(2qI_B + \frac{K_F I_B^{A_F}}{F}\right)\Delta f \tag{56.46}$$

$$\overline{i_C^2} = 2qI_C\,\Delta f \tag{56.47}$$

where K_F and A_F are the flicker noise coefficients. More detailed information about noise modeling is given in the bipolar noise section of this text (Chapter 58.2).

SPICE Model of the Bipolar Transistor

The SPICE model of bipolar transistor uses similar or identical equations as described in this chapter [3]–[5]. Table 56.2 below shows the parameters of the bipolar transistor model and its relation to the parameters used in this chapter.

The SPICE (Simulation Program with Integrated Circuit Emphasis [3]) was developed primarily for the analysis of integrated circuits. During the analysis it is assumed that the temperatures of all circuit elements are the same. This is not true for power integrated circuits, where the junction temperatures may differ by 30 K or more. This is obviously not true for circuits composed of discrete elements, where the junction temperatures may differ by 100 K or more. These temperature effects, which can significantly affect the analysis results, are not implemented in the SPICE program.

Although the SPICE bipolar transistor model used more than 40 parameters, many features of the bipolar transistor are not included in the model. For example, the reverse junction characteristics are described by (56.36) and (56.37). This model does not give accurate results. In the real silicon junction the leakage current is proportional to the thickness of the depletion layer, which is proportional to $V^{1/m}$. Also, the SPICE model of the bipolar transistor assumes that there are no junction breakdown voltages. A more accurate model of the reverse junction characteristics is described in the diode section of this text. The reverse transit time τ_R is very important in order to model the switching property of the lumped bipolar transistor, and it is a strong function of the biasing condition and temperature. Neither phenomena are implemented in the SPICE model.

Relative Machability

The device parameters of transistors fabricated on the same chip are almost the same. This feature is used for unique integrated circuit design. For various technological processes, the distribution of device parameters are different. For example, the layer's resistances in the typical diffusion process may vary by ±20 percent. When the ion implantation process is used, those variations are below ±5 percent, or occasionally, even below ±2 percent. From the circuit designer's point of view, the relative machability is still more important. The circuit parameters usually depend on the resistor to resistor ratio or the ratio of the device areas. Special care should be taken during the device layout design. For example, the integrated resistor shown

TABLE 56.2 Parameters of SPICE Bipolar Transistor Model

Name Used	Equations	SPICE Name	Parameter Description	Unit	Typical Value	SPICE Default
I_s	(56.10), (56.11)	IS	Saturation current	A	10^{-15}	10^{-16}
I_{SE}	(56.36), (56.39)	ISE	B–E leakage saturation current	A	10^{-12}	0
I_{SC}	(56.37), (56.39)	ICS	B–C leakage saturation current	A	10^{-12}	0
β_F	(56.14), (56.16), (56.21)	BF	Forward Current gain	—	100	100
β_R	(56.14), (56.16), (56.21)	BR	Reverse current gain	—	0.1	1
η_F	(56.15), (56.24), (56.30), (56.31), (56.39)–(56.41)	NF	Forward current emission coefficient	—	1.2	1.0
η_R	(56.15), (56.24), (56.30), (56.31), (56.39)–(56.42)	NR	Reverse current emission coefficient	—	1.3	1.0
η_E	(56.42)	NE	B–E leakage emission coefficient	—	1.4	1.5
η_C	(56.39), (56.42)	NC	B–C leakage emission coefficient	—	1.4	1.5
V_{AF}	(56.21), (56.40)	VAF	Forward Early voltage	V	200	∞
V_{AR}	(56.21), (56.40)	VAR	Reverse Early voltage	V	50	∞
I_{KF}	(56.22), (56.23), (56.41)	IKF	β_F high-current roll-off corner	A	0.05	∞
I_{KR}	(56.22), (56.23), (56.41)	IKR	β_R high-current roll-off corner	A	0.01	∞
I_{RB}	(56.26)	IRB	Current where base resistance falls by half	A	0.1	∞
R_B	(56.25), (56.26)	RB	Zero base resistance	Ω	100	0
$R_{B\,min}$	(56.25), (56.26)	RBM	Minimum base resistance	Ω	10	RB
R_E	Fig. 56.6	RE	Emitter series resistance	Ω	1	0
R_C	Fig 56.6	RC	Collector series resistance	Ω	50	0
C_{JE0}	(56.27)	CJE	B–E zero-bias depletion capacitance	F	10^{-12}	0
C_{JC0}	(56.28)	CJC	B–C zero-bias depletion capacitance	F	10^{-12}	0
C_{JS0}	(56.29)	CJS	Zero-bias collector-substrate capacitance	F	10^{-12}	0
V_{JE0}	(56.27)	VJE	B–E built-in potential	V	0.8	0.75
V_{JC0}	(56.28)	VJC	B–C built-in potential	V	0.7	0.75
V_{JS0}	(56.29)	VJS	Substrate junction built-in potential	V	0.7	0.75
m_{JE}	(56.27)	MJE	B–E junction exponential factor	—	0.33	0.33
m_{JC}	(56.28)	MJC	B–C junction exponential factor	—	0.5	0.33
m_{JS}	(56.29)	MJS	Substrate junction exponential factor	—	0.5	0
X_{CJC}	Fig. 56.6	XCJC	Fraction of B–C capacitance connected to internal base node (see Fig. 56.6)	—	0.5	0
τ_F	(56.17), (56.28), (56.30), (56.42)	TF	Ideal forward transit time	s	10^{-10}	0
τ_R	(56.31)	TR	Reverse transit time	s	10^{-8}	0
X_{TF}	(56.43)	XTF	Coefficient for bias dependence of τ_F	—		0
V_{TF}	(56.43)	VTF	Voltage for τ_F dependence on V_{BC}	V		∞
I_{TF}	(56.43)	ITF	Current where $\tau_F = f(I_C, V_{BC})$ starts	A		0
P_{TF}	(56.44)	PTF	Excess phase at freq $= 1/(2\pi\tau_F)$ Hz	deg		0
X_{TB}	(56.38)	XTB	Forward and reverse beta temperature exponent			0
E_G	(56.34)	EG	Energy gap	eV	1.1	1.11
X_{TI}	(56.35)–(56.37)	XTI	Temperature exponent for effect on I_s	—	3.5	3
K_F	(56.46)	KF	Flicker-noise coefficient	—		0
A_F	(56.46)	AF	Flicker-noise exponent	—		1
F_C	—	FC	Coefficient for the forward-biased depletion capacitance formula	—	0.5	0.5
T_{NOM}	(56.32)–(56.38)	TNOM	Nominal temperature specified in .OPTION statement	K	300	

FIGURE 56.14 Two resistor topologies: (a) sensitive to contacts misalignment; (b) nonsensitive to contacts misalignment.

in Fig. 56.14(a) is very sensitive to the misalignment of the contact mask, while the resistor shown in Fig. 56.14(b) is not. With small mask misalignment, the increase of resistance near one contact is compensated by the decrease of resistance near another contact. This concept can be extended for the transistor layout design. If the ratio of emitter areas of two transistors should be, for example, three, then it is recommended to fabricate three identical transistors and connect them in parallel. Any attempt to fabricate a transistor with an area three times larger than another will lead to meaningful device mismatching. This is due not only to edge effects, but also due to the current crowding effect and other phenomena.

The SPICE program has the ability to model both absolute and relative parameter distributions. It can be done by using the *LOT* and *DEV* parameters in the .MODEL statement. For example if $LOT = 10$ percent and $DEV = 1$ percent, then parameters for all devices may vary by ± 10 percent, but relative variation from device to device will be ± 1 percent. This feature makes the SPICE program very suitable for integrated circuit simulation. The Monte Carlo analysis implemented in the PSPICE program makes the integrated circuit design even easier.

References

[1] J. J. Ebers and J. M. Moll, "Large signal behavior of bipolar transistors," *Proc. IRE*, vol. 42, pp. 1761–1772, Dec. 1954.

[2] H. K. Gummel and H. C. Poon, "An integral charge-control model of bipolar transistors," *Bell Syst. Tech. J.*, vol. 49, pp. 827–852, May 1970.

[3] L. W. Nagel and D. O. Pederson, "SPICE (Simulation program and integrated circuit emphasis)," Univ. California, Berkeley, ERL Memo ERL M382, Apr. 1973.

[4] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*, New York: McGraw-Hill, 1988.

[5] A. Vladimiresku, *The SPICE Book*, New York: Wiley, 1994.

[6] A. S. Grove, *Physics and Technology of Semiconductor Devices*, New York: Wiley, 1967.

[7] S. M. Sze, *Physics of Semiconductor Devices*. 2nd ed., New York: Wiley, 1981.

[8] G. W. Neudeck, *The PN Junction Diode*, vol. II, Modular Series on Solid-State Devices, Reading, MA: Addison-Wesley, 1983.

[9] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed., New York: Wiley, 1986.

[10] E. S. Yang, *Microelectronic Devices*, New York: McGraw-Hill, 1988.

[11] B. G. Streetman, *Solid State Electronic Devices*, 3rd ed. Englewood Cliffs, NJ: Prentice Hall, 1990.

[12] D. A. Neamen, *Semiconductor Physics and Devices*, Irwin 1992.