Negative Resistance Element for a Static Memory Cell Based on Enhanced Surface Generation

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Abstract—**A negative resistance (NR) element for a novel static memory cell that uses enhanced surface generation of MOS devices is proposed. Such a memory cell will require extremely small current to maintain information and the control circuitry can be the same as in one-transistor dynamic memories. The mechanism of operation is discussed and some experimental data are presented. It is shown that in order to maintain information in a single static memory cell, the required current can be as low as a few picoamperes.**

I. Introduction

RECENTLY, two new approaches toward converting dynamic RAM memories into static ones have been announced. Both are based on modifications of the one-transistor DRAM structure and its organization.

One concept is based on properties of ferroelectric materials. This can increase the value of the storage capacitor for 64- and 256-Mb ULSI DRAM's [1] or create nonvolatile memories [2]. A much simpler technological process can be used in comparison to DRAM memories with trench capacitors. Ferroelectric nonvolatile memories have, however, a few drawbacks. While no refreshing cycles are required, after a reading cycle a restore cycle is required which results in slowed operation as in DRAM memories. Another disadvantage is that ferroelectric material is degenerated after 10^{10}–10^{11} read–write cycles.

The second concept also uses the well-known one-transistor dynamic memory cell, which is converted into a static memory cell by adding an n-type negative resistance (NR) element as shown in Fig. 1(a). The required characteristic of the NR element is shown in Fig. 1(b). With such a characteristic for the NR element, the capacitor on which charge is stored will never lose information due to leakage current, since the NR element will supply all losses. A novel structure for realizing such an NR element for a SRAM cell was recently proposed by researchers from the Toshiba ULSI Research Center [3]. The Toshiba cell is based on the reverse-bias-current (RBC) phenomenon in a bipolar transistor. It uses the negative input resistance of a bipolar transistor, which results from avalanche multiplication in the reverse-biased collector junction. This approach significantly reduces the required area for a single static memory cell.

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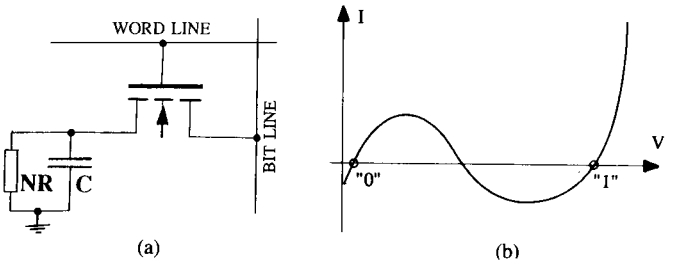

Fig. 1. SRAM cell: (a) circuit diagram, and (b) required characteristic of NR element.

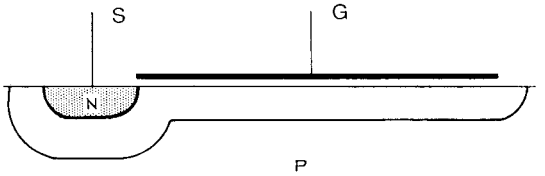

Fig. 2. P-N junction with MOS-controlled leakage current.

This cell has a relatively small logic swing (from 0.2 to 0.9 V), which can sometimes be a disadvantage. The other drawback of this solution, which is not clearly mentioned in [3], is that for proper operation the cell will consume a relatively large power when the cell is to store a ONE. In this instance, the voltage of the base–emitter junction is about 0.9 V and the collector voltage must be higher than 5 V.

II. Enhanced Generation Current in MOS Devices

In this presentation the effect of enhanced leakage current due to surface generation under the MOS gate in a MOS transistor is used for development of an NR element in a static memory cell application. Enhanced surface generation current under a MOS gate was observed more than 20 years ago [4], [5]. This device is known as a gate-controlled diode. For the structure shown in Fig. 2, the current of the reverse-biased p-n junction will have two basic generation components. The first is due to bulk generation in the depletion region:

$$I_{B\,\mathrm{gen}} = 0.5 q n_i \frac{\zeta}{\tau_0}. \tag{1}$$

The second results from enhanced surface generation when the surface under the MOS gate is depleted:

$$I_{S\,\mathrm{gen}} = 0.5 q n_i s_0 A_s \tag{2}$$

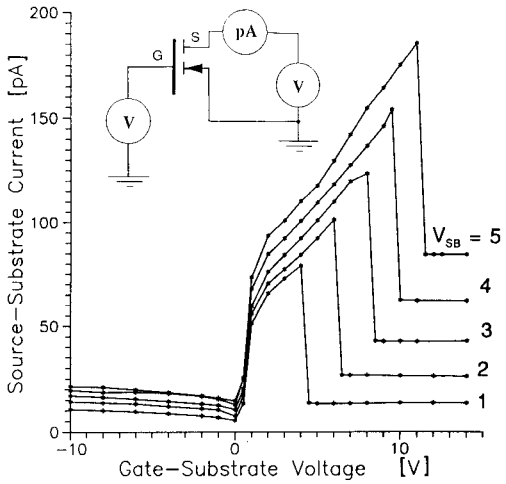

Fig. 3. Measured diode characteristics of a 2N4351 NMOS transistor.

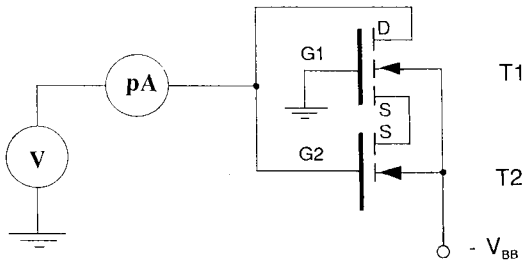

Fig. 4. Equivalent circuit of NR element.

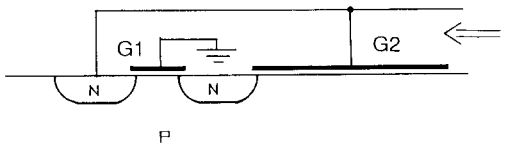

Fig. 5. Integrated structure of NR element.

where

$\zeta(V_{GB}, V_{SB})$	volume of depletion region,
A_s	surface area covered with MOS gate,
τ_0	effective lifetime,
$s_0(V_{GB}, V_{SB})$	surface recombination velocity.

The second generation component exists only when the surface under the gate is depleted. A very significant current decrease can be observed during the transition from depletion to inversion, when the depletion region is driven below the surface to where the concentration of generation–recombination centers is considerably less. In measurements on 2N4351 NMOS discrete transistors, shown in Fig. 3, this excess generation current in the depletion mode can be very easily seen. In this measurement the source–substrate junction was reverse biased and the leakage current was measured as a function of gate–substrate voltage with source–substrate voltage as a parameter. For measurement of extremely small leakage currents, the Keithley 485 digital picoammeter with a resolution of 0.1 pA and voltage drop below 200 μV was used. However, due to thermal effects and noise, practical measurement accuracy was in the range of a few picoamperes. About 20 transistors of this type and various production series were tested. All exhibited similar characteristics. In the transition from the depletion mode to the inversion mode, in all cases the leakage current drops at least by half; in some cases this current drop was one-fifth of the depletion value. This sudden leakage current drop with increasing voltage can be used to obtain the desired NR element.

III. The NR Element

The gate-controlled diode shown in Fig. 3 is a three-terminal device. Any two-terminal configuration of this device will not exhibit negative resistance behavior. In the three-terminal configuration a rapid drop of current can be observed when the source–substrate voltage is kept constant while the gate–source voltage is increased. The equivalent circuit of the proposed NR element is shown in Fig. 4. In order to achieve this, that is, to have the input current magnitude drop with an increase of input voltage, an extra transistor buffer in the common-gate configuration is introduced to keep constant

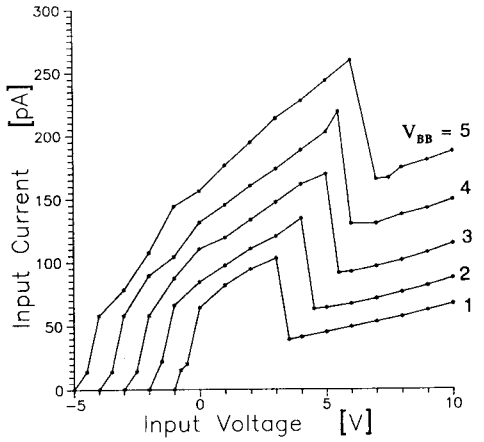

Fig. 6. Measured characteristics of circuit from Fig. 4.

voltage across the reverse-biased p-n junction (source–substrate). If the source–substrate voltage is allowed to rise, the NR region is reduced or lost.

An integrated realization of this circuit is shown in Fig. 5. Gate $G1$ should have significantly smaller area than gate $G2$ so the effect of excess current created in the depleted layer under gate $G1$ can be negligible compared to that under gate $G2$. This task can be accomplished relatively easily in an integrated structure. It was difficult to observe this effect in a circuit with two discrete 2N4351 transistors. For purposes of measurement, transistor $T1$ was chosen to have smaller leakage and excess generation currents than $T2$. Measured input currents as a function of input voltage with substrate voltage as the parameter are shown in Fig. 6. The effect of negative resistance at currents in the picoampere range can be clearly seen for all substrate voltages. In order to obtain the required characteristic as shown in Fig. 1(b), which exhibits both positive and negative currents, additional dc biasing is required. This can be accomplished using the leakage current from an extra reverse-biased diode connected between the NR node and a positive voltage.

The power required for maintaining the storage information is very small. In our experiment with discrete large-size MOS transistors, this current was in the range of 100 pA. It can be expected that in an integrated structure it can be

reduced by one or two orders of magnitude. Therefore, for a 1-Mb RAM, maintenance current can be of the order of a few microamperes. Such memories with small backup batteries can perform as essentially permanent or nonvolatile memories.

IV. Conclusion

It is shown that enhanced generation current in the depletion layer under an MOS gate can be used to construct a negative resistance element operating in the picoampere range. Operating currents are large enough to compensate for leakage currents of storage capacitors in dynamic RAM memories. By adding the described circuit in parallel with those capacitors, the dynamic memory can be converted into a static memory, requiring no refresh circuit or restoring circuit. In the proposed memory structure the storage capacitor can be reduced significantly or perhaps even eliminated. This will result in much faster operation in comparison to DRAM memories.

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