SIMPLIFIED BIPOLAR TRANSISTOR STRUCTURE FOR VLSI APPLICATIONS

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In recent years the triple diffusion transistor technology gained special attention [1][2]. Device dimentions were reduced while the current density and the sheet resistances of diffusion layers remain the same. Transistor currents are lower, and the series collector is reduced. Therefore the voltage drop across collector resistance could be almost negligible. At the same time the parasitic capacitance of collector-base junction is also reduced. Depletion layer capacitance component is smaller due to the smaller mask patterns. The diffusion capacitance is lowered because the collector layer is thinner and it has impurity gradient.

The triple diffused transistor can be considered as NPN transistor merged with PNP clamping device. Once NPN transistor is getting into saturation the substrate PNP transistor starts to conduct and it sinks an extra input current into the substrate.

The transistor structures with different parameters were fabricated. The main goal of various approaches was to investigate the influence of the collector layer parameters on the transistor performance. The value of collector resistance is 30 to 40 ohms. This resistance was measured on the collector characteristics for small collector voltages using a method described in [4]. This value of series resistance corresponds to the maximum voltage drop of 80 mV at 2 mA which is practically negligible. A forward current gain is about 20 but transistors with current gain above 100 were also fabricated.

In order to test dynamic properties of triple diffused transistor the special chain of nine inverters has been designed. The oscillation frequency of fabricated structures monotonically increases with supply voltage. It means that junction parasitic capacitances are the main factor which limits the delay time. It can be also observed that devices with thinner collector layer have smaller delay time. The minimum delay time per gate for devices with 8 μm thick collector is about 13 ns per inverter. In a case of devices with 5.6 μm deep collector the delay time is about 7 ns.

The developed transistor is suitable for digital bipolar integrated circuits. The fabrication process is much simpler, and higher packing density can be obtained with certain photolithography limits. The static and dynamic properties do not differ much from the parameters of transistors obtained by the epiplanar process. The triple diffusion technology developed is therefore also an interesting alternative to BIMOS technology where bipolar and MOS transistors are merged into one chip. Further improvement of transistor parameters seems to be possible.

REFERENCES

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