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PUNCH-THROUGH SPACE-CHARGE LIMITED LOADS

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Abstract: This presentation discusses a device which operates in a punch-through condition with space-charge control of currents. The structure is simple, with two N+ or P+ regions formed in P- or N- substrate, respectively.

Punch-through space-charge limited structures, both N+P-N+ and P+N-P+, were simulated using the developed general one-dimensional semiconductor device performance simulation program GESIM1 for dynamic and static analysis. Structures of various configurations were fabricated and tested.

These punch-through diodes should have applications as a replacement for integrated resistors in high-speed VLSI applications. They can provide very small area, large value resistors based on the space-charge limiting action of the device. Thus, they could also be called punch-through space-charge limited loads (SCLL). The range of resistance values is large, and small dimensions lead to small capacitances and fast switching times.

INTRODUCTION

The desire to increase the density of silicon devices on IC chips is causing problems associated with integrated resistors on the chip. Shrinking the device size leads to lower currents thereby requiring larger values of resistors. At the same time the values of the sheet resistance and unit capacitance basically remain unchanged. This has caused device researchers to investigate resistor like devices based on different operating or processing principles. One result is to use polysilicon resistors. However, doped polysilicon layers frequently require additional processing effort. It is relatively difficult to control the resistance of such layers because the resistance depends not only on the impurity concentration, but also on the grain size of the polycrystaline silicon.

This paper discusses a device which operates in a punch-through condition with space-charge control of currents. This device can be considered as an alternative to integrated resistors. The punch-through condition was identified some time ago as an undesirable condition to be avoided. However, a properly designed and fabricated two terminal device operating in a punch-through mode can provide stable high values of resistance in small areas on a chip. Large voltage drop at low current density is possible when space-charge neutrality is not satisfied and current flow is controlled by space charge of moving carriers. The resistance can be linear over a broad range of operating conditions, although it is a nonlinear device.

OPERATING PRINCIPLES

The theory for Space-Charge Limited (SCL) current was given by Mott and Gurney [1]. The

SCL mechanism was reported as a controlling mechanism in Shockley's Analog Transistor [2] and Teszner's Short Channel FET [3], Richman's MOS TRansistor [4], Nishizawa's SIT Transistor [5] and Ohmi's Punch-Trough Transistor [6]. A lateral version of the Punch-Through Transistor was also published [7]. A detailed theory of SCL for various devices is given in [8,9].
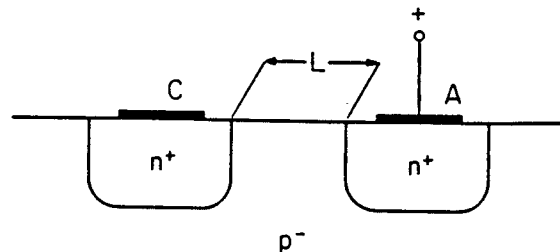

Fig. 1.   N+P-N+ punch-through structure.

Figure 1 shows the cross section structure of an N+P-N+ punch-through diode which can also be made as a P+N-P+ structure [10]. Positive voltage applied to either metal contact will reverse bias the adjacent junction creating a depletion layer region. As the applied potential is increased the depletion layer punches through the N+ region, and current starts to flow. Electrons injected into the depletion region create an internal space-charge which affects the potential distribution. This injected space-charge will control current flow as the voltage is increased beyond the "punch-through" or threshold voltage which can be controlled by geometry and substrate resistivity.

DEVICE SIMULATION

Punch-through and space-charge phenomena are complicated in nature and, in order to fully investigate and understand their behavior, a computer simulation is necessary. Most of the existing computer simulation programs use various combinations of simplified approaches [11]. Frequently simulation assumptions include: Boltzman's statistics, neglecting recombination, neglecting space charge, dominance of one type of carrier, neglecting fast transition (shorter than relaxation time). However, for small geometry high speed devices for VLSI applications, such assumptions are not valid and a more general approach is needed. Thus, a GEneral one-dimensional semiconductor device performance SIMulation program (GESIM1) has been developed. This program allows the user to simulate the static and dynamic performance of a device. The GESIM1 simulation includes all parasitic effects and provides information about the detailed transient behavior of such devices.

The input data required, consists of the impurity concentration distribution and the applied terminal voltages. The steady-state solution is found first, and then transient analysis is performed for any given voltage excitation. It is also possible to incorporate the GESIM1 device simulation into a circuit and solve for operating conditions. Transient terminal voltages and currents can be determined from the simulation.

Punch-through space-charge limited structures were simulated using the developed program. The one dimensional simulations gave the results discussed below.
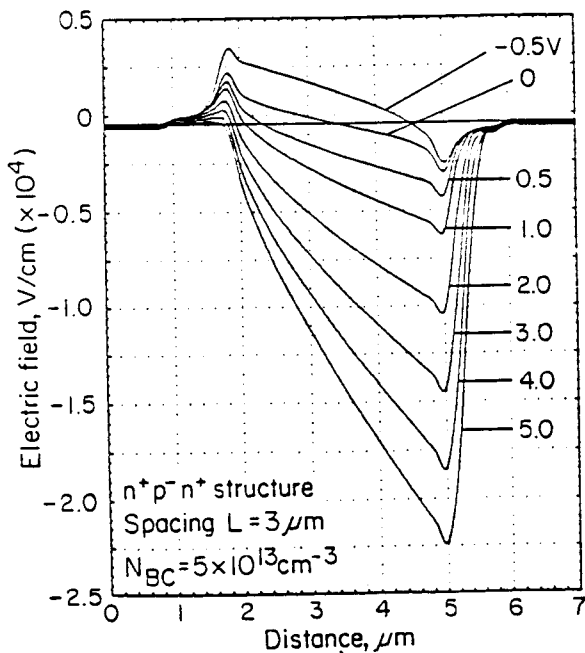
Figures 2 through 5 show the results of simulation for an N+P-N+ punch-through space-charge diode for the spacing between N+ regions L = 3 µm. The voltage applied at the anode with respect to the cathode is varied from -0.5 to 5 volts. The metallurgical cathode is at 2 microns. Fig. 2 presents potential distribution and Fig. 3 shows electric field distribution. Subsequent figures give space-charge distribution (Fig. 4) and electron density distribution (Fig. 5). One can observe that when voltage increases, the number of injected electrons also increases which creates additional negative space charge. This also affects the electrical field distribution and potential distribution.

Fig. 2. Steady-state analysis of punch-through structure; potential distribution.
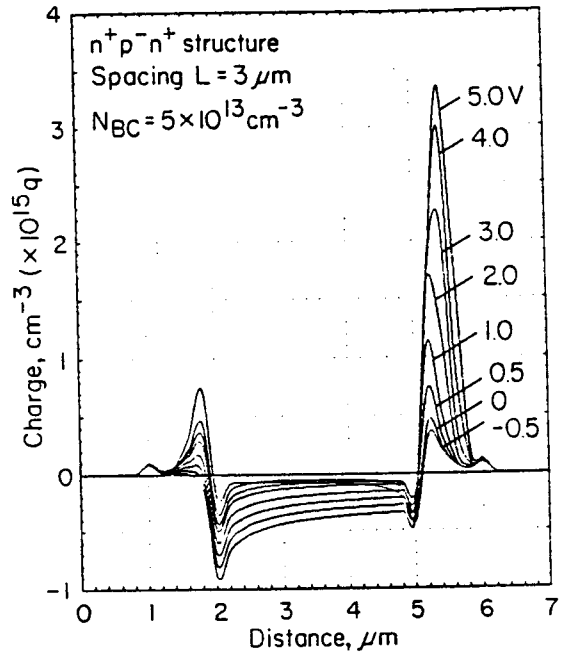

Fig. 4. Steady-state analysis of punch-through structure; space-charge distribution.

Fig. 3. Steady-state analysis of punch-through structure; electric field distribution.
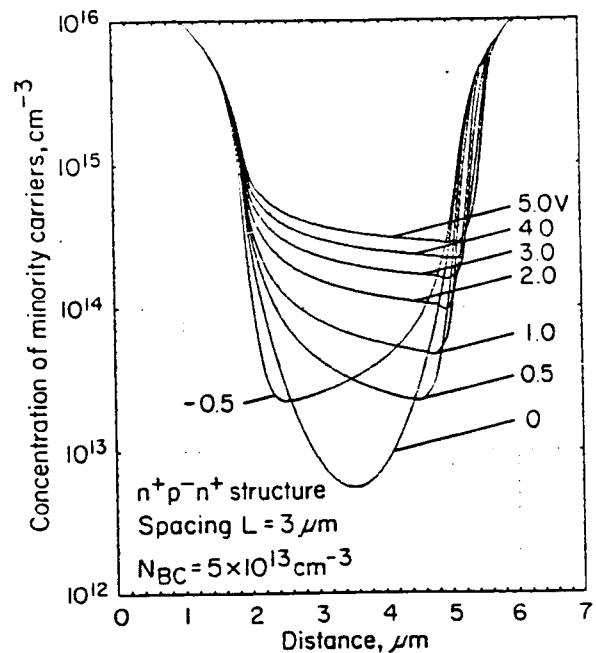

Fig. 5. Steady-state analysis of punch-through structure; minority carriers distribution.

Figures 6 through 9 show potential, electric field, charge and carriers distribution, respectively for various spacings between N+ regions varying from 1 μm to 6 μm, and 1 volt applied to the device. With the different spacing one can observe variations in charge and carrier distributions which affect potential distribution. It can be seen that current flow is controlled by potential barrier, height of which depends on the applied voltages, amount of the space charge of moving carriers, and is also a function of distance. The J - V characteristics are shown in Figure 10.

According to the classic theory with a depletion layer approach, in such a punch-through device current should start to flow for voltages exceeding the punch-through voltage given by

$$V_{pt} = q \frac{N_{BC}}{2\epsilon\epsilon_0} L^2 \qquad (1)$$
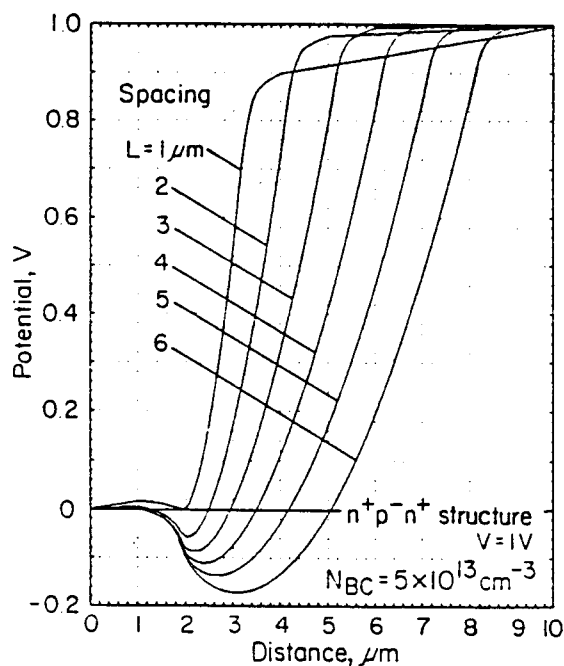

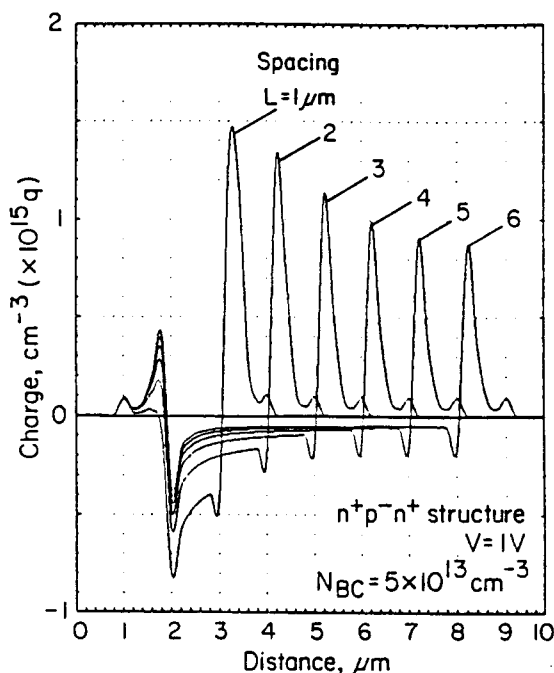Fig. 6. Steady-state analysis of punch-through structure; potential distribution.

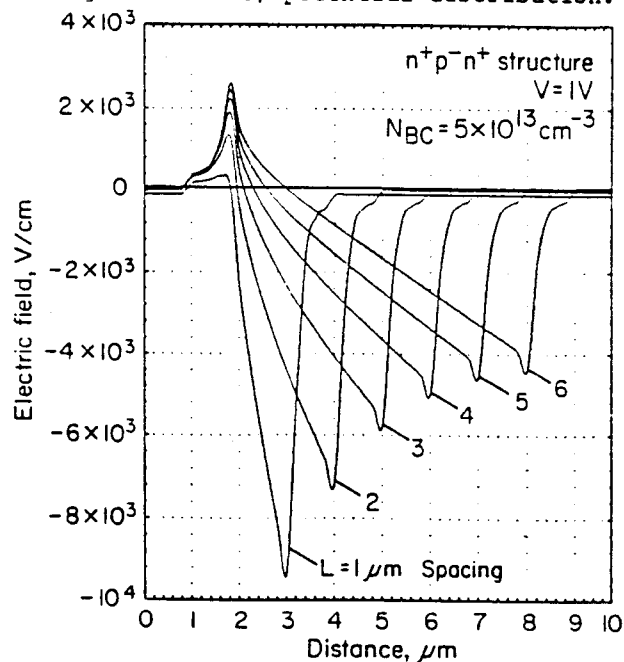Fig. 8. Steady-state analysis of punch-through structure; space-charge distribution.

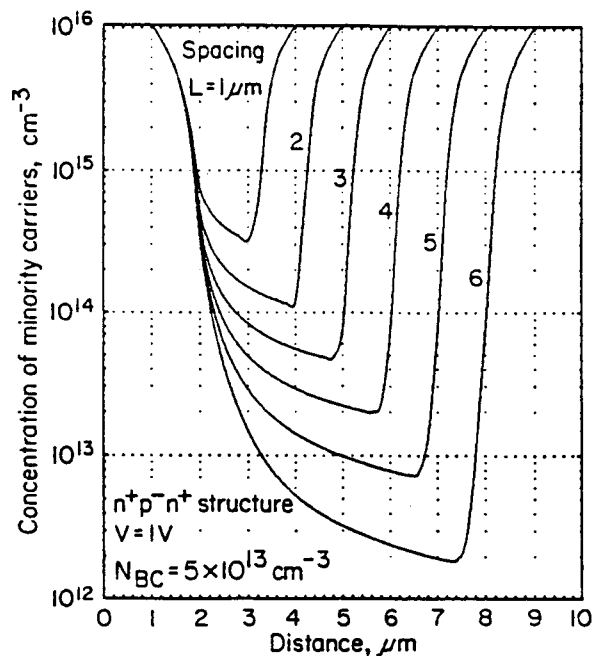Fig. 7. Steady-state analysis of punch-through structure; electric field distribution.

Fig. 9. Steady-state analysis of punch-through structure; minority carriers distribution.

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where q is the electronic charge, $\epsilon\epsilon_0$ is the dielectric constant, and N_{BC} is the substrate (background) concentration. In reality it can be observed that current may flow at much smaller voltages than V_{pt}. This effect is similar to that observed in short-channel MOS devices and is known as "sub-threshold conduction".

In case of integrated circuits not the value of current itself but an incremental resistance is of more importance. If it is assumed that carrier velocity v is proportional to electrical field E (v = u * E), then the diode current density J_d is related to its voltage V_d by [12]:

$$J_d = \frac{9}{8} \mu\epsilon\epsilon_0 \frac{V_d^2}{L^3} \qquad (2)$$

where u is the carriers mobility. From equation (2) one can obtain

$$\frac{dV}{dJ} = \sqrt{\frac{8 L^3}{9 \mu\epsilon\epsilon_0 J_d}} \qquad (3)$$

If it is assumed that the electrical field E is large and the carrier velocity is saturated (i.e. $v = v_{sat}$), then

$$J_d = \frac{2 v_{sat} \epsilon\epsilon_0}{L^2} V_d \qquad (4)$$

and

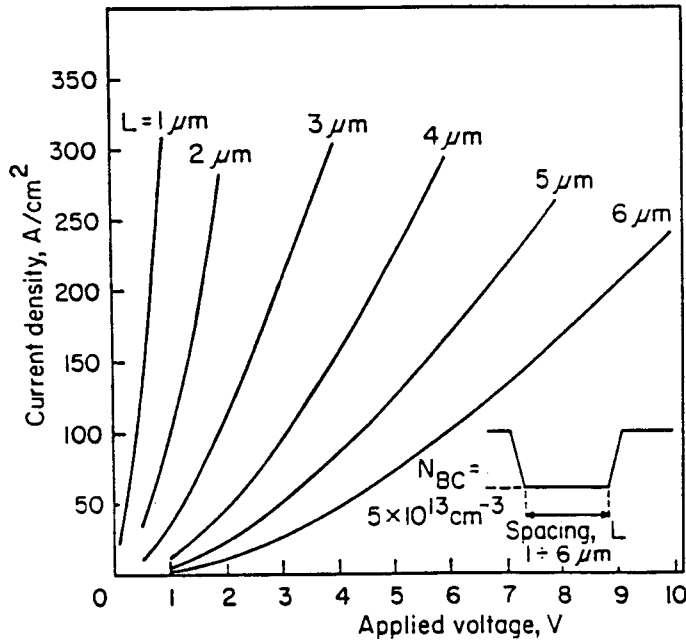$$\frac{dV}{dJ} = \frac{L^2}{2 v_{sat} \epsilon\epsilon_0} \qquad (5)$$

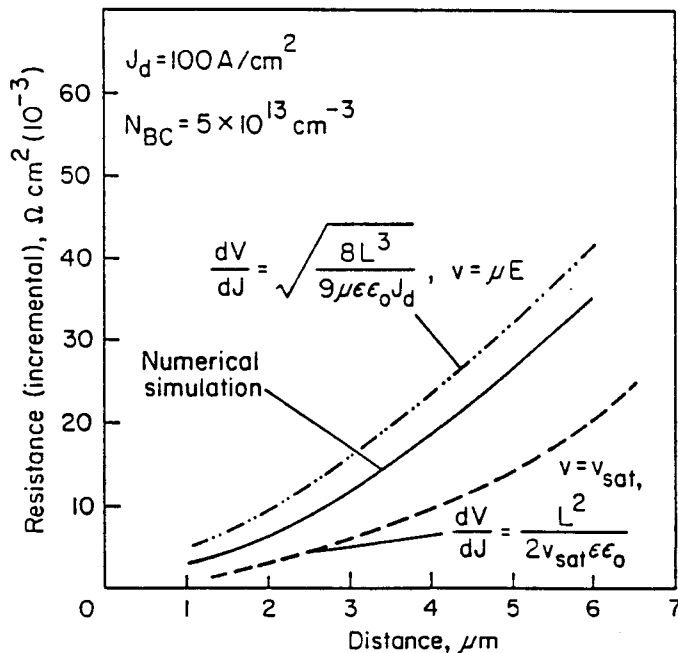Fig. 10. Steady-state analysis of punch-through structure; J-V characteristics.

Fig. 11. Punch-through structure; incremental resistanve vs. spacing between anode and cathode.

Figure 11 shows comparison of results obtained from equations (3), (5) and numerical results.

Transient analysis of punch-through space-charge loads was also performed. Some of the results for a 6-micron P+N-P+ diode are shown in Figures 12 and 13. Figure 12 gives the carrier distribution vs. distance during switching from 2 to 10 volts as a function of time in 30 psec increments and Figure 13 presents the charge distribution for the same operating conditions. As it can be seen time to reach steady state is comparable with dielectric relaxation time and it is of the order of picoseconds. Therefore, this device can be considered as very fast. Also it should be pointed out that during the operation both the cathode and anode are surrounded by thick depletion layers; therefore, parasitic capacitances to the substrate are very low.
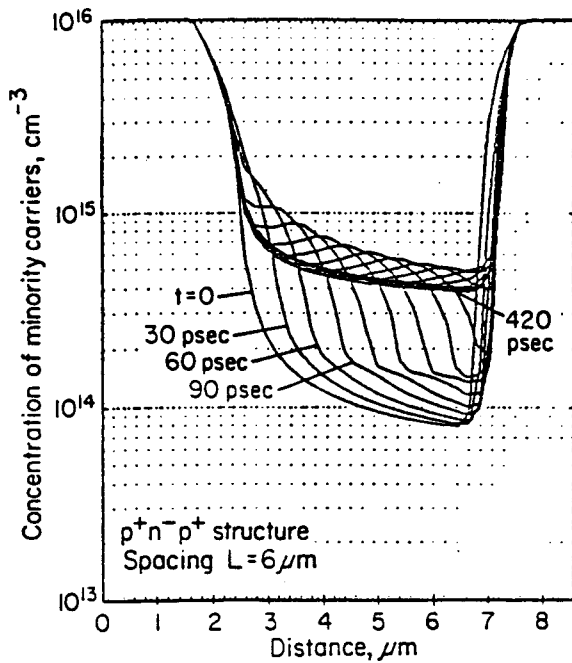
Fig. 12. Transient analysis of punch-through structure; minority carriers distribution.
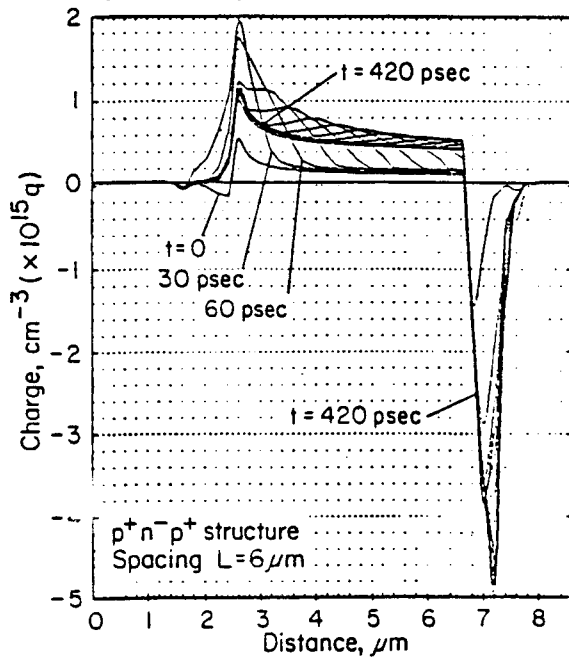

Fig. 13. Transient analysis of punch-through structure; space-charge analysis.

is shown in Figure 16. Table 1 shows the summary of the experimental results of both designs for the N+P-N+ structures.
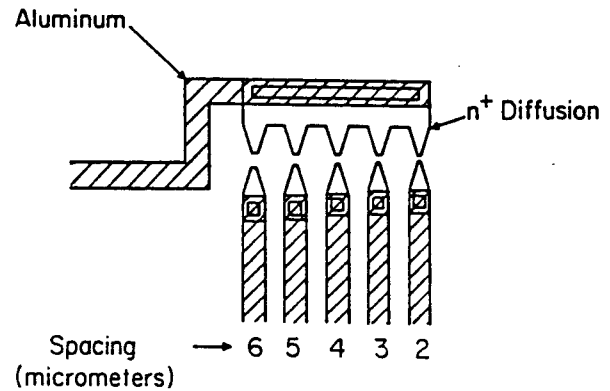

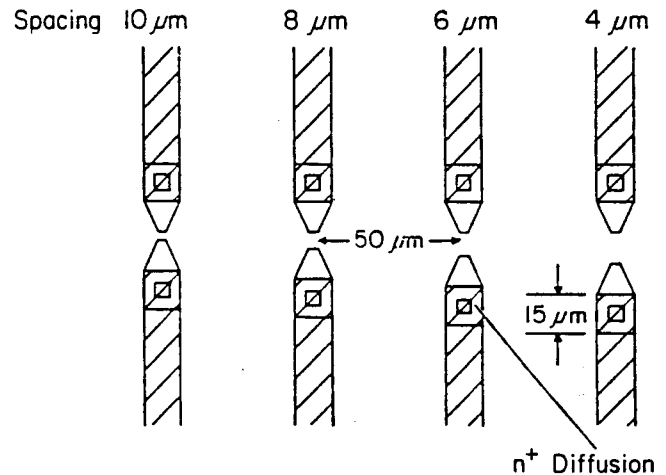Fig. 14. Punch-through space-charge limited load; preliminary design.

Fig. 15. Punch-through space-charge limited load; revised design.

EXPERIMENTS

Punch-through space-charge limited loads of various configurations were fabricated and tested. Two designs of the structure are shown in Figures 14 and 15. Devices were fabricated with various spacing between the cathode and anode: 2, 3, 4, 5, 6, 8 and 10 µm. The preliminary design (Fig. 14) exhibited nonsymmetrical I-V characteristics and was replaced with the revised design shown in Figure 15. The sample of I-V characteristics of the latter design for the N+P-N+ structure (with background concentration of 8*10**12/cm**3 and spacings of 4, 6, 8 and 10 microns)

As it can be seen both the substrate background concentration and the spacing effect the values of the incremental resistance. In the case of small spacing (high carrier concentration gradient) currents can flow for voltages below those predicted by punch-through voltage. The device spacing has somewhat different effect (in terms of exact values) on the incremental resistance than it was predicted by simulation. This can be explained by 3-dimensional phenomena which have to be considered, and therefore one can say that not only the spacing but geometry and size of cathode and anode are of importance.

Table 1. Summary of experimental results; values of incremental resistances [Ω] taken with the bias of 5.0 *) and 10 **) volts.

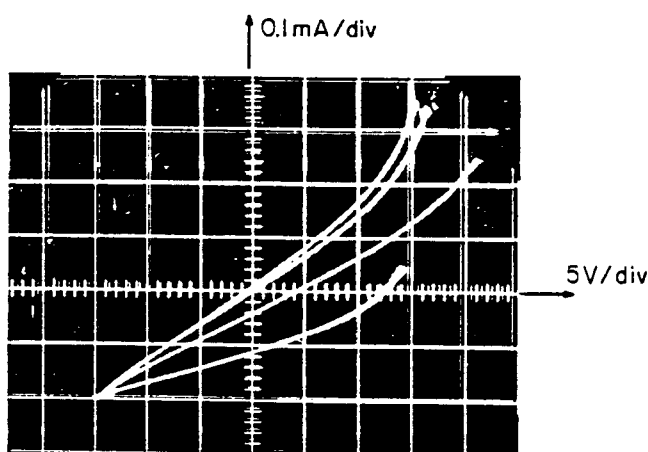| Background concentration (cm**-3)	Spacing (µm)							Note Design
	2	3	4	5	6	8	10	
7*10**13 *)			8.8k	14.0k	23.3k			Fig. 14
1*10**13 *)	8.0k	9.0k	14.0k	18.0k				Fig. 14
8*10**12 **)			67.6k		73.5k	96.0k	156.0k	Fig. 15

Fig. 16. I-V characteristics of the structure from Fig. 15.

CONCLUSIONS

The punch-through space-charge limited loads (SCLL) can be considered as an alternative solution for integrated resistors when small parasitics and high performance are required.

The advantages of SCLL are as follows: (a) small area of active device, (b) high values of resistances, (c) small parasitic capacitances, (d) very fast transients, and (e) possibility of controlling device characteristics by device geometry.

However, there are some limitations to SCLL that can be summed up as follows: (a) larger area is required to avoid couplings between neighboring devices; for that purpose special "isolation" wells can be recommended, and (b) relatively small substrate concentration is required if the controlled spacing is in the um range; however, if the submicron range is considered, the background concentration can be higher.

ACKNOWLEDGEMENT

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