SRC TOPICAL RESEARCH CONFERENCE "DEVICES AND STRUCTURES", San Diego, CA
June 15, 1984

NOVEL BIPOLAR TRANSISTOR STRUCTURES AND LOADS

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OUTLINE

26. B. M. Wilamowski, R. H. Mattson, Z. J. Staszak, R. Craigin, A. Musallam, J. N. Fordemwalt, "Novel bipolar transistor structures and loads", SRC Topical Research Conference, June 15, 1984, San Diego, USA.

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OUTLINE

1. INTRODUCTION

1.1 BACKGROUND

- BIPOLAR INTEGRATED CIRCUITS RETAIN SUPERIORITY FOR HIGH SPEED APPLICATIONS AS DIMENSIONS ARE SCALED DOWN BUT REQUIRE RELATIVELY COMPLICATED PROCESSING, INCLUDING THIN EPITAXIAL LAYERS AND BURIED SUBCOLLECTORS

1.2 RESEARCH GOALS

- TO INVESTIGATE AND DEVELOP NEW HIGH SPEED VLSI SIMPLIFIED BIPOLAR INTEGRATED STRUCTURES USING PROCESSING SIMILAR TO MOS TECHNOLOGY

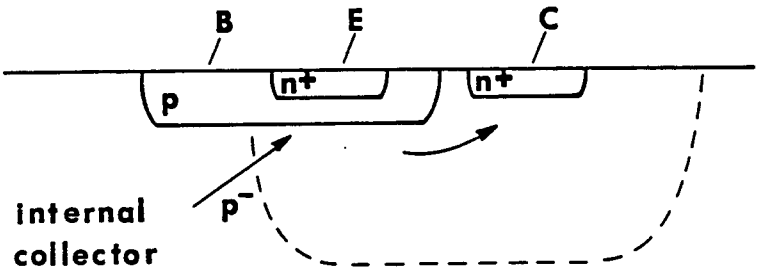
2. SATURATION PROTECTED BIPOLAR TRANSISTORS

- A NOVEL CONCEPT FOR TRANSISTOR FABRICATION
- PROTECTION AGAINST SATURATION BY USING A STATIC INDUCTION TRANSISTOR (SIT) OR A PNP SUBSTRATE TRANSISTOR AS A CLAMP
- FUNCTION OF THE SATURATION PROTECTION: TO PREVENT THE SWITCHING TRANSISTOR FROM ENTERING INTO A DEEP SATURATION MODE BY LIMITING THE CHARGE STORED IN THE COLLECTOR

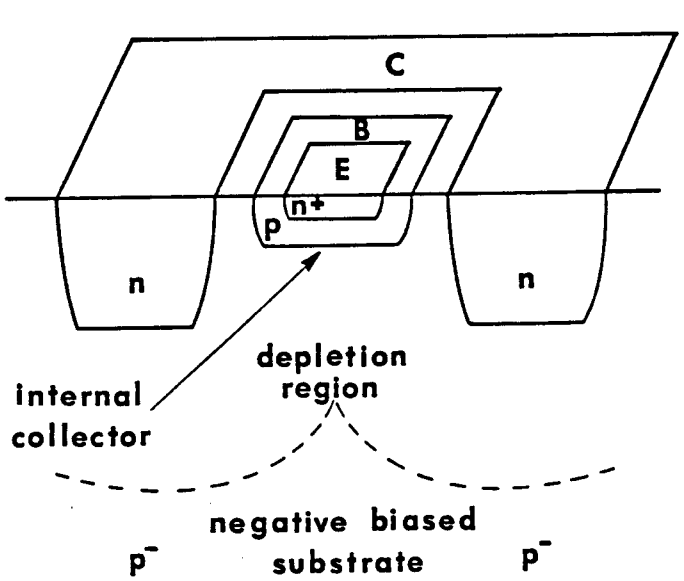
2.1 THE SIT SATURATION PROTECTED BIPOLAR TRANSISTOR (SPT/SIT)

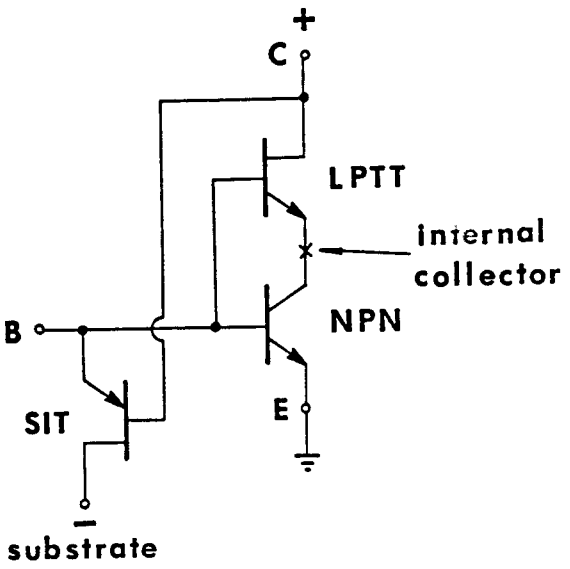
- OPERATING PRINCIPLES

  * A SIMPLIFIED BIPOLAR STRUCTURE FOR VLSI

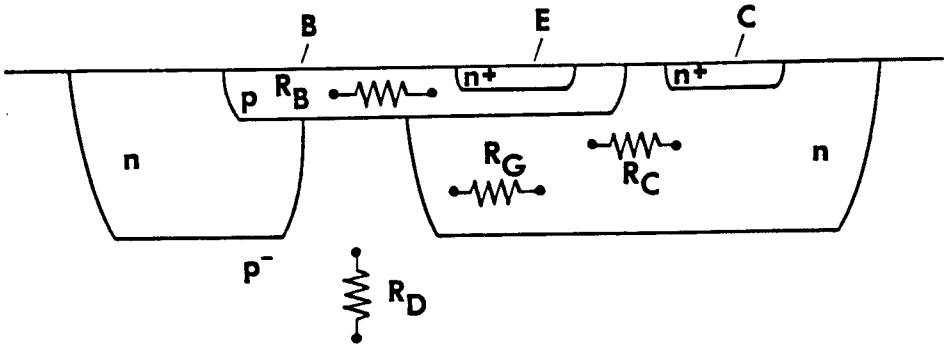


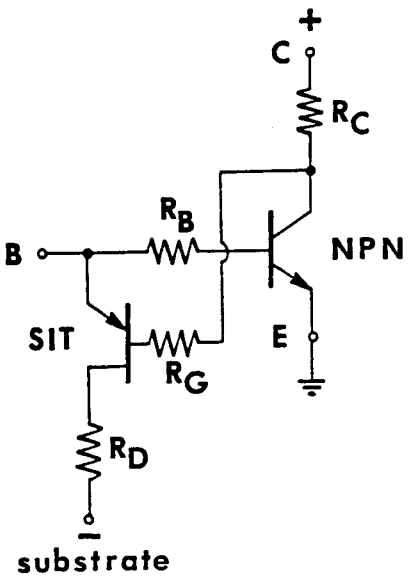
  * A MODIFIED BIPOLAR STRUCTURE FOR VLSI



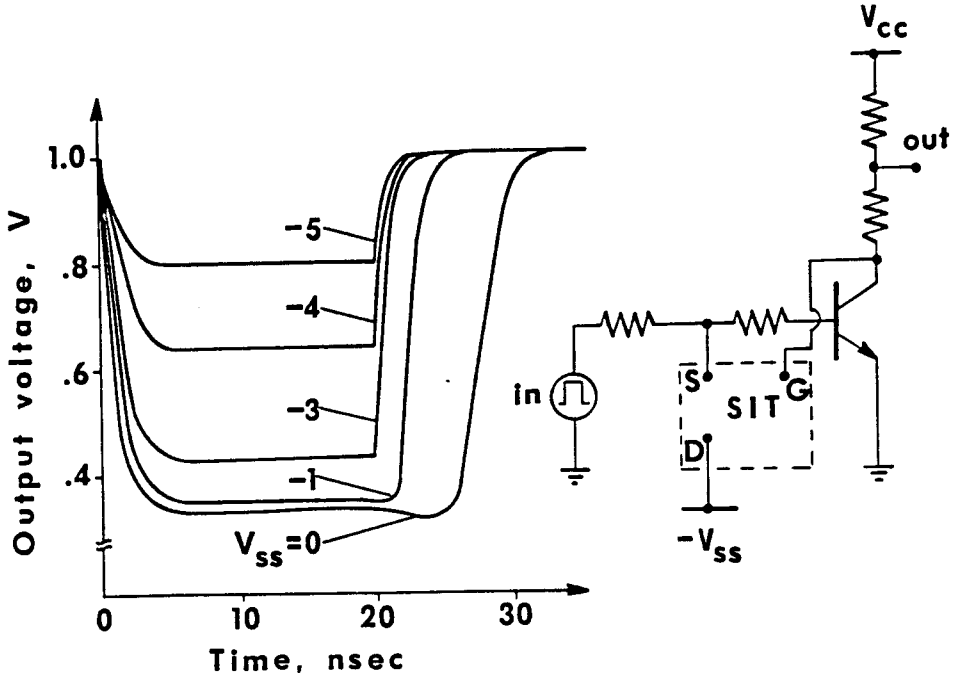


- A TRIPLE DIFFUSED NPN BIPOLAR TRANSISTOR WITH SIT PROTECTION

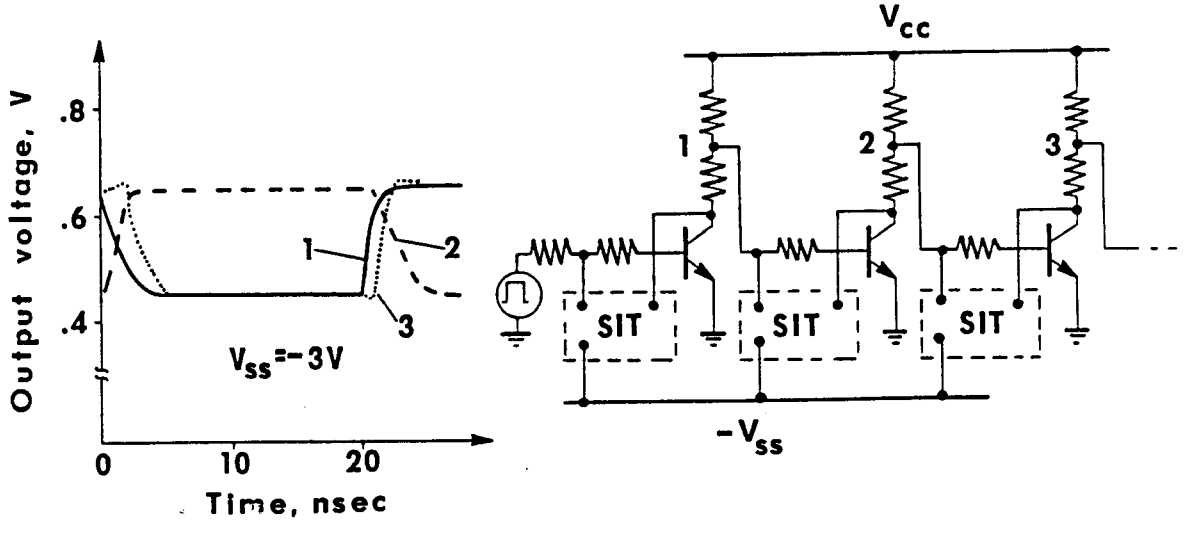




- SIMULATION RESULTS
  - * OUTPUT WAVEFORMS FOR A SINGLE STAGE UNLOADED INVERTER WITH AN SIT PROTECTED BIPOLAR TRANSISTOR

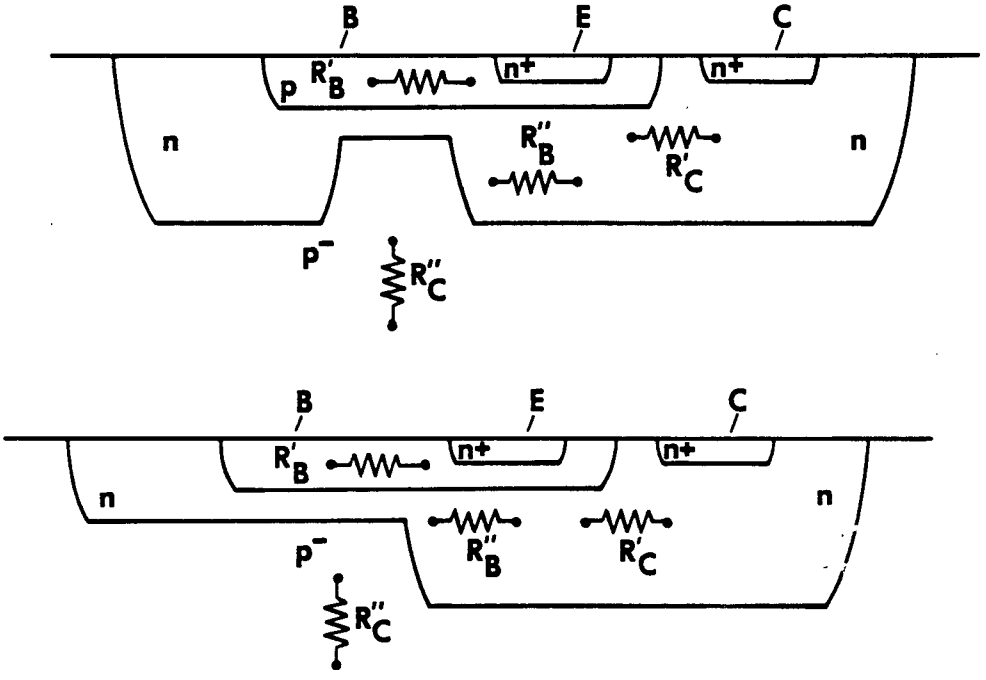


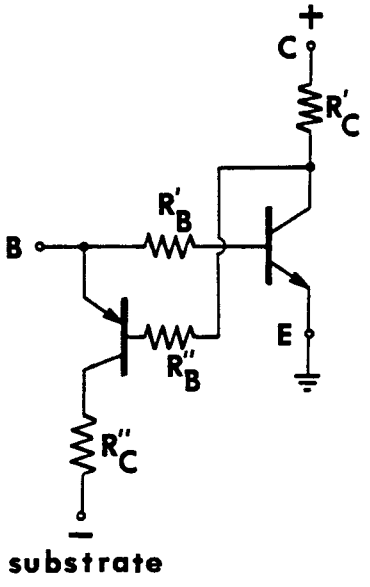
  - * OUTPUT WAVEFORMS FOR A CHAIN OF INVERTERS WITH SIT PROTECTED BIPOLAR TRANSISTORS



2.2 The PNP Saturation Protected Bipolar Transistor (SPT/PNP)

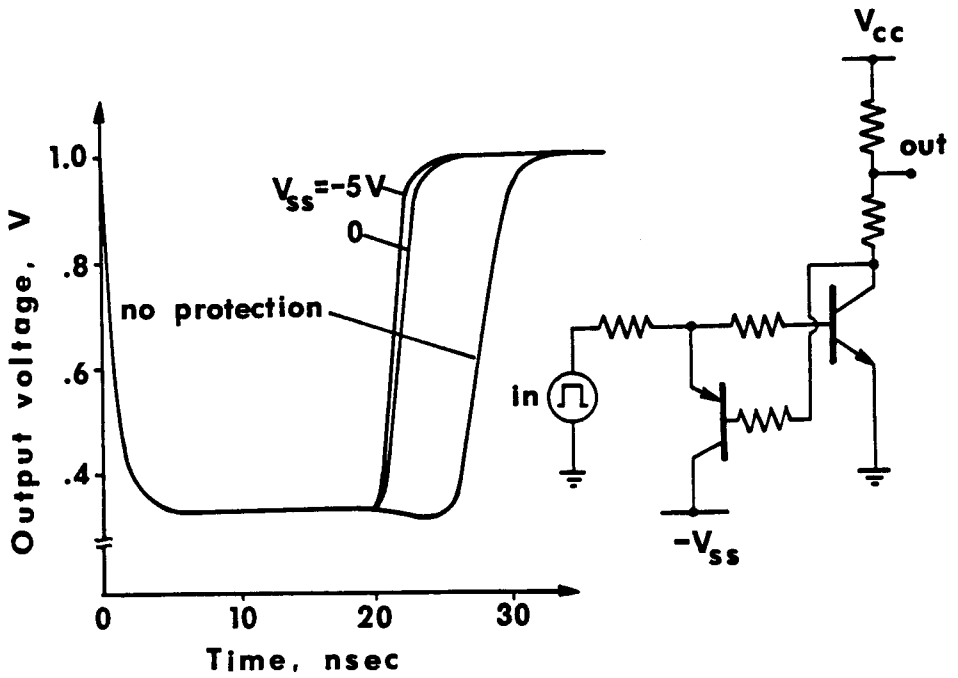
- An alternative approach
- Quadruple diffused NPN bipolar transistor structures with PNP protection



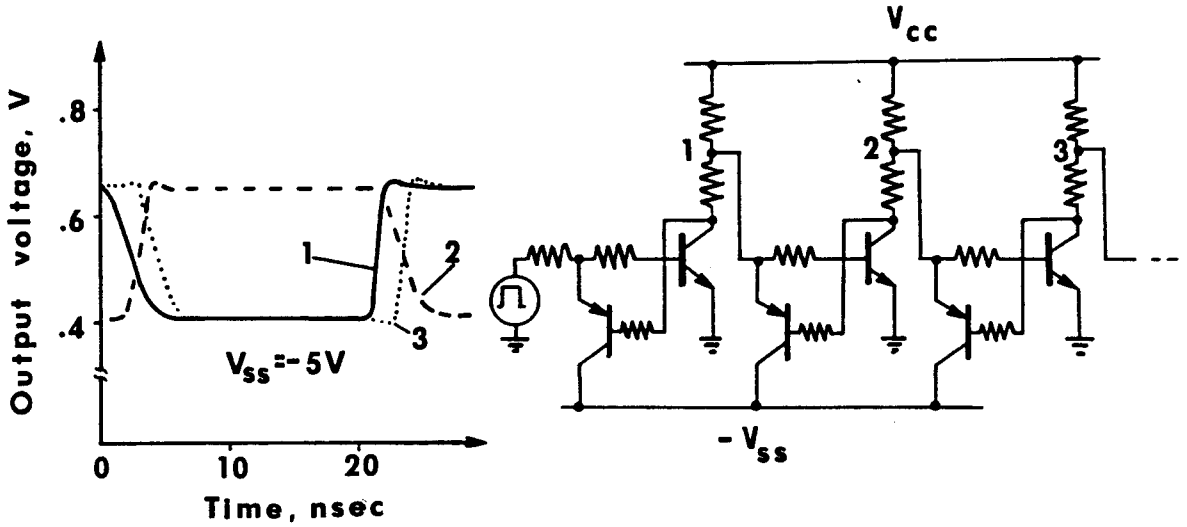


- SIMULATION RESULTS

  * OUTPUT WAVEFORMS FOR A SINGLE-STAGE UNLOADED INVERTER WITH A PNP PROTECTED BIPOLAR TRANSISTOR

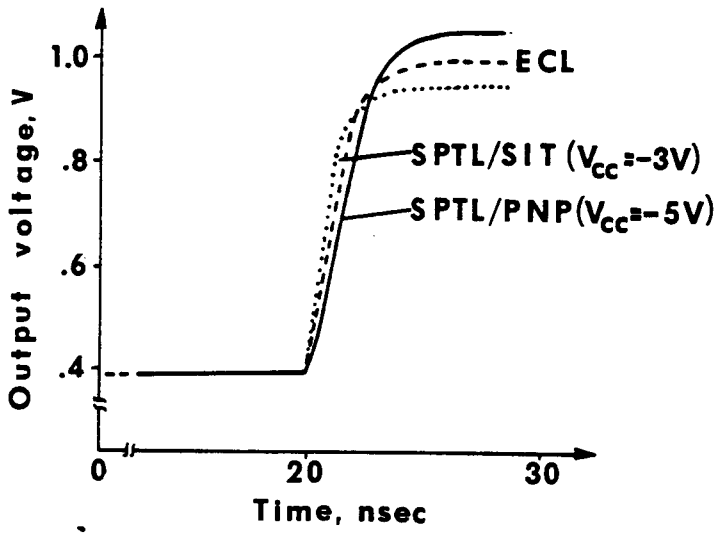


  * OUTPUT WAVEFORMS FOR A CHAIN OF INVERTERS WITH PNP PROTECTED BIPOLAR TRANSISTORS



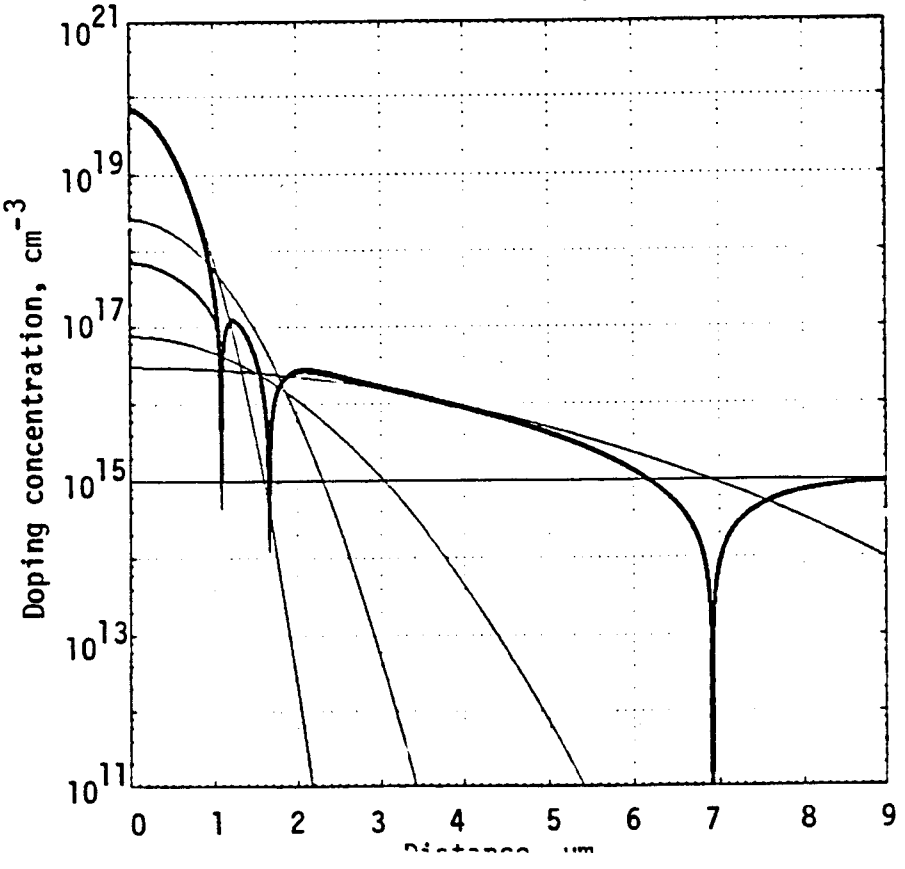
2.3 Conclusions

- Improved switching times for SPT/SIT and SPT/PNP gates when compared to similar gates without protection; charge-storage eliminated
- SPT/SIT: Sensitive to substrate biasing which effects voltage swing and delay time
- SPT/PNP: Somewhat inferior to SPT/SIT in speed but can operate with zero bias; practically insensitive to substrate biasing
- RTL Gates: Protected by SIT or PNP, operate with speed of ECL gates, but with smaller power consumption

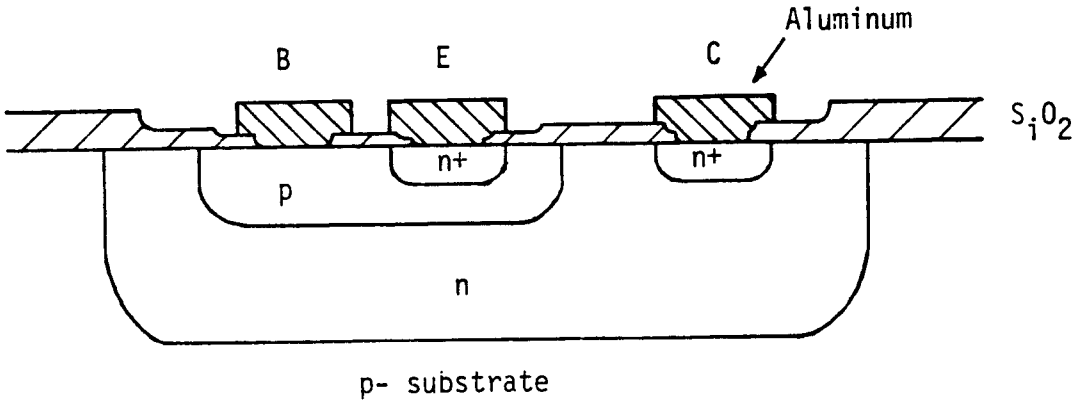


2.4 Device Fabrication

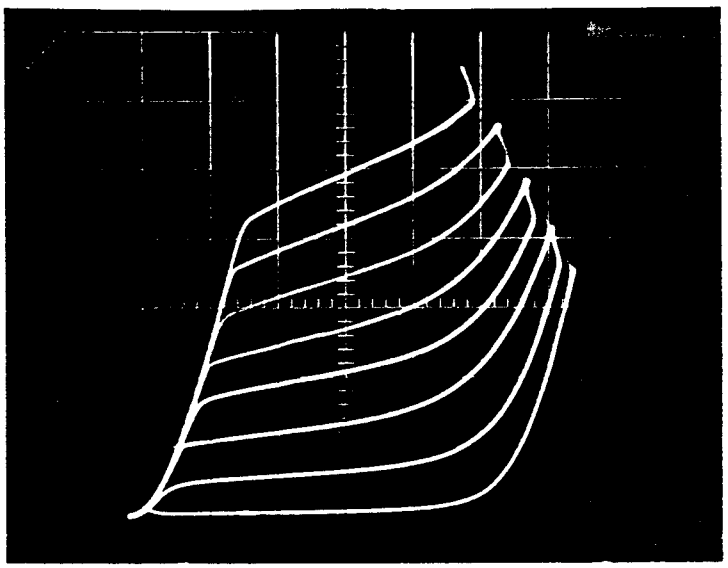
- Bitras (BIpolar TRAnsistor Simulator);
  - * Developed to support technological implementation of triple/quadruple diffused structures;
  - * Allows a process designer to accurately simulate silicon fabrication technologies;
  - * Combines technological and electrical parameters of devices;
  - * Program input: Fabrication parameters such as times, temperatures and doses;
  - * Program output: Simulated one dimensional impurity profile plots, and device technological and electrical parameters;
  - * Example doping profiles of a quadruple diffused structure



- THIN BASE TRANSISTORS

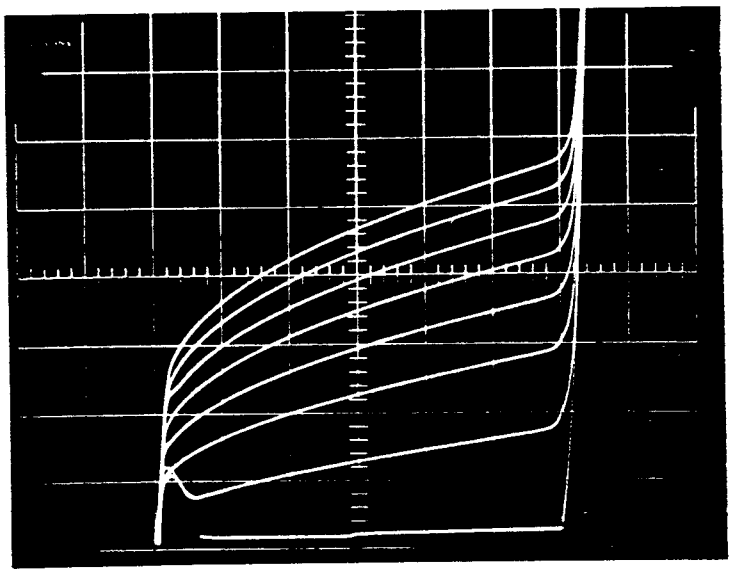


THIN BASE NPN TRANSISTOR FABRICATED IN 4 μM TO 6 μM N-WELLS (WHICH PROVIDE ISOLATION)



VERT.: .2MA/DIV
HORIZ.: 1V/DIV
0.001MA/STEP

I-V CHARACTERISTICS FOR A TYPICAL DEVICE WITH 0.6 μM BASE-EMITTER AND 0.9 μM BASE-COLLECTOR JUNCTIONS

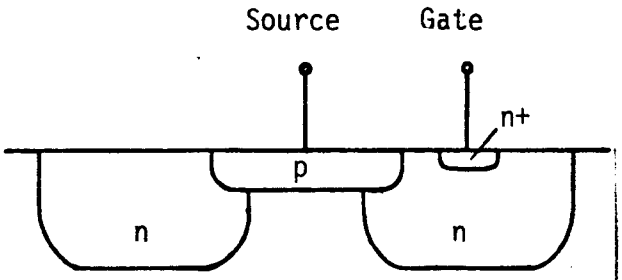


VERT.: 1MA/DIV
HORIZ.: 2V/DIV
.1MA/STEP

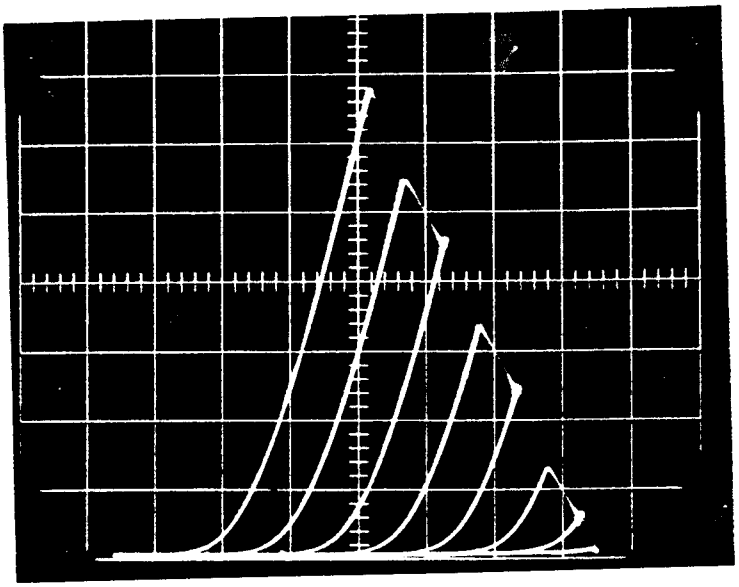
I-V CHARACTERISTICS FOR A SIMILAR DEVICE (WITH N-TYPE SUBSTRATE INSTEAD OF N-WELL) PROCESSED WITH A PHOSPHORUS DOPED POLISILICON EMITTER

- STATIC INDUCTION TRANSISTOR

  * P-SUBSTRATE



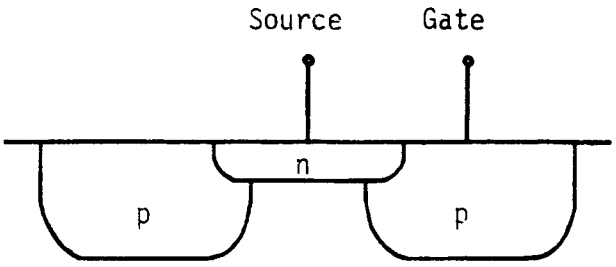
p- substrate drain



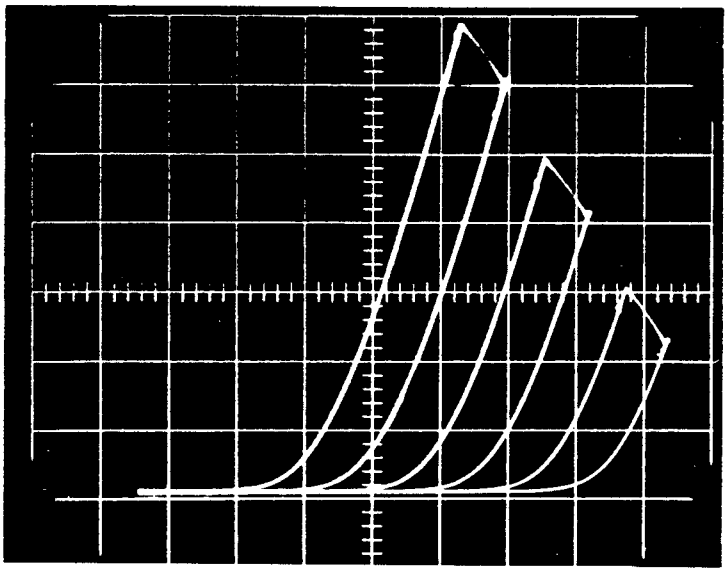
VERT. .2MA/DIV., HORIZ. 1V/DIV

1 MA/STEP, 6 μM WINDOW, R = 1 KΩ

  * N-SUBSTRATE

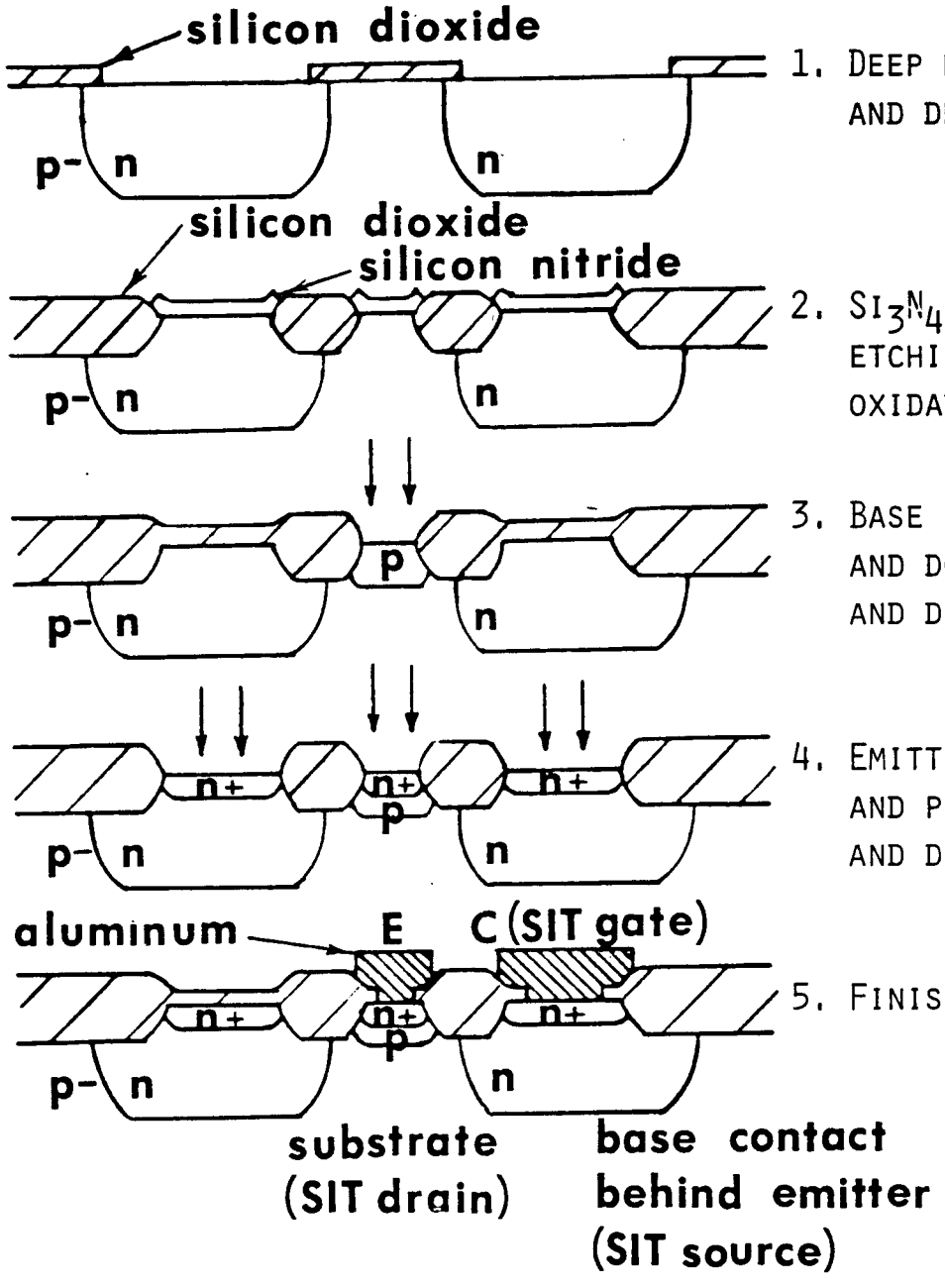


n- substrate drain



VERT. .1MA/DIV., HORIZ. 0.5V/DIV

0.5 MA/STEP, 6 μM WINDOW, R = 1 KΩ



1. DEEP N-TYPE IMPLANT AND DRIVE.

2. Si_3N_4 DEPOSITION AND ETCHING, AND LOCOS OXIDATION.

3. BASE PHOTOLITHOGRAPHY AND DOUBLE BORON IMPLANT AND DRIVE.

4. EMITTER PHOTOLITHOGRAPHY AND PHOSPHORUS IMPLANT AND DRIVE.

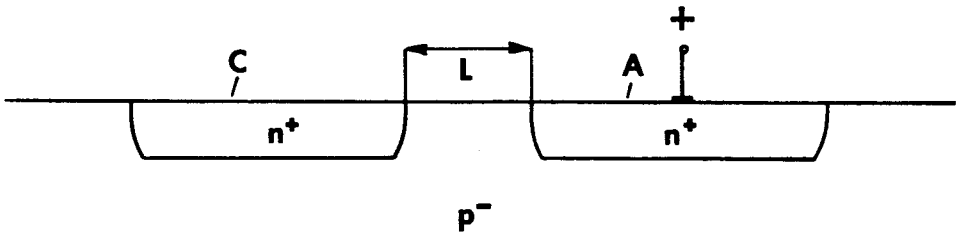
5. FINISHED DEVICE.

ISOPLANAR PROCESS FOR NPN-BIPOLAR TRANSISTOR WITH S.I.T. PROTECTION AGAINST SATURATION

3. PUNCH-THROUGH SPACE-CHARGE LIMITED LOADS

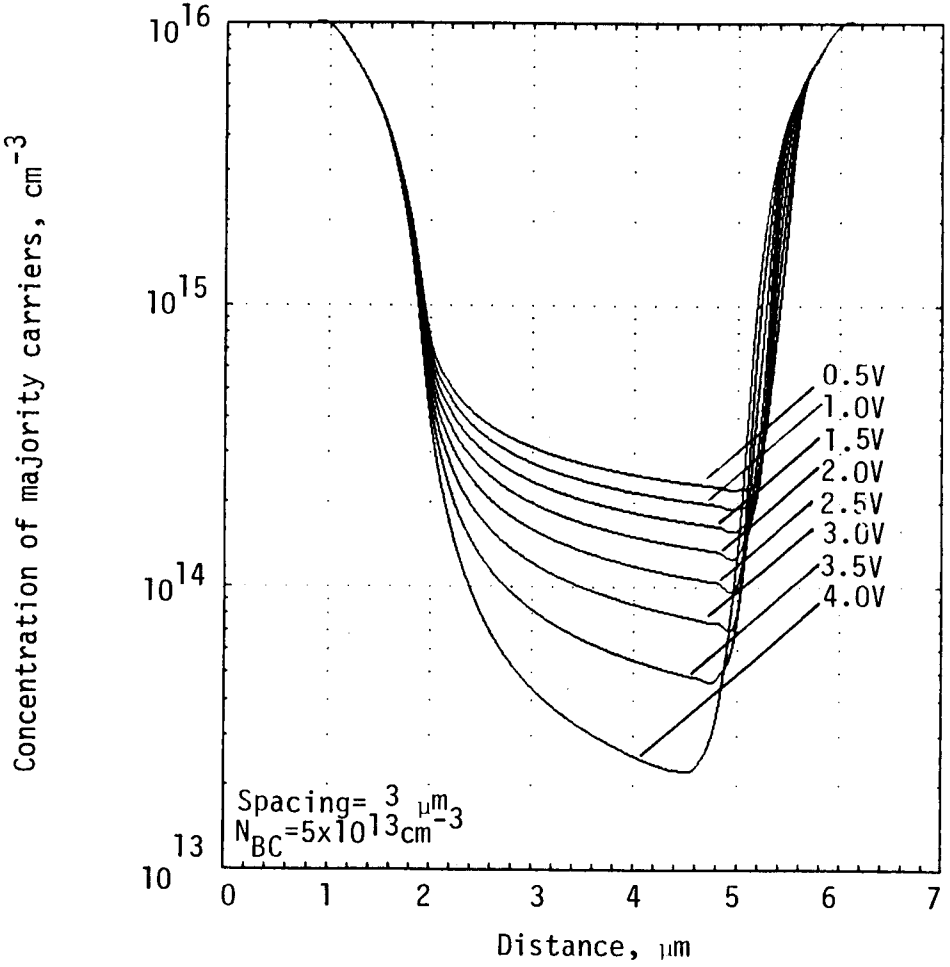
- PUNCH-THROUGH AND SPACE-CHARGE PHENOMENA: COMPLICATED IN NATURE, A COMPUTER SIMULATION NECESSARY TO FULLY INVESTIGATE AND UNDERSTAND. THUS A GENERAL ONE-DIMENSIONAL DEVICE PERFORMANCE SIMULATION PROGRAM (GESIM1) WAS DEVELOPED
  - * NO SIMPLIFYING ASSUMPTIONS
  - * SIMULATES STATIC AND DYNAMIC PERFORMANCE
  - * INPUT DATA: IMPURITY CONCENTRATION DISTRIBUTION AND APPLIED TERMINAL VOLTAGE
  - * PROVIDES INFORMATION ABOUT INTERNAL DETAILED TRANSIENT BEHAVIOR OF SIMULATED DEVICES (POTENTIAL, ELECTRIC FIELD, CHARGE, HOLES, ELECTRONS, HOLE CURRENT, ELECTRON CURRENT, RECOMBINATION CURRENT, FERMI POTENTIALS)

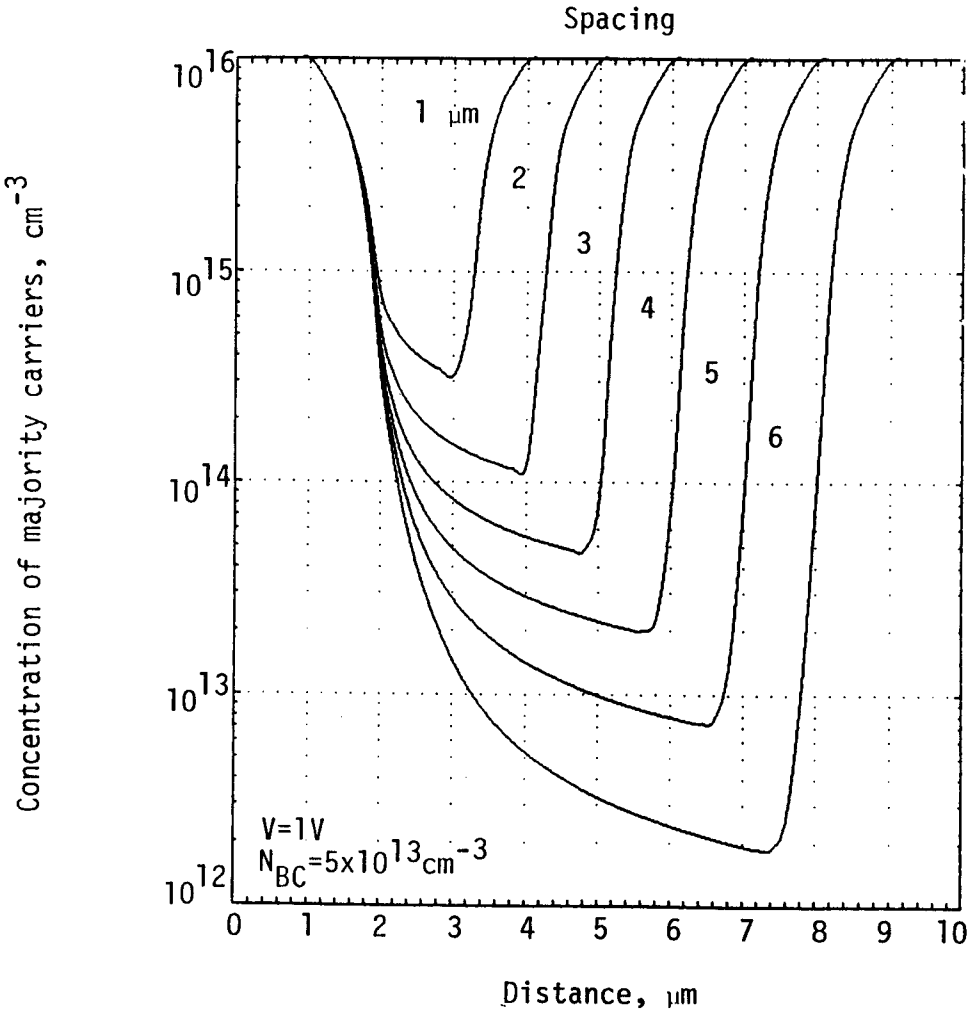
- OPERATING PRINCIPLES
  - * A PUNCH-THROUGH SPACE-CHARGE-LIMITED STRUCTURE

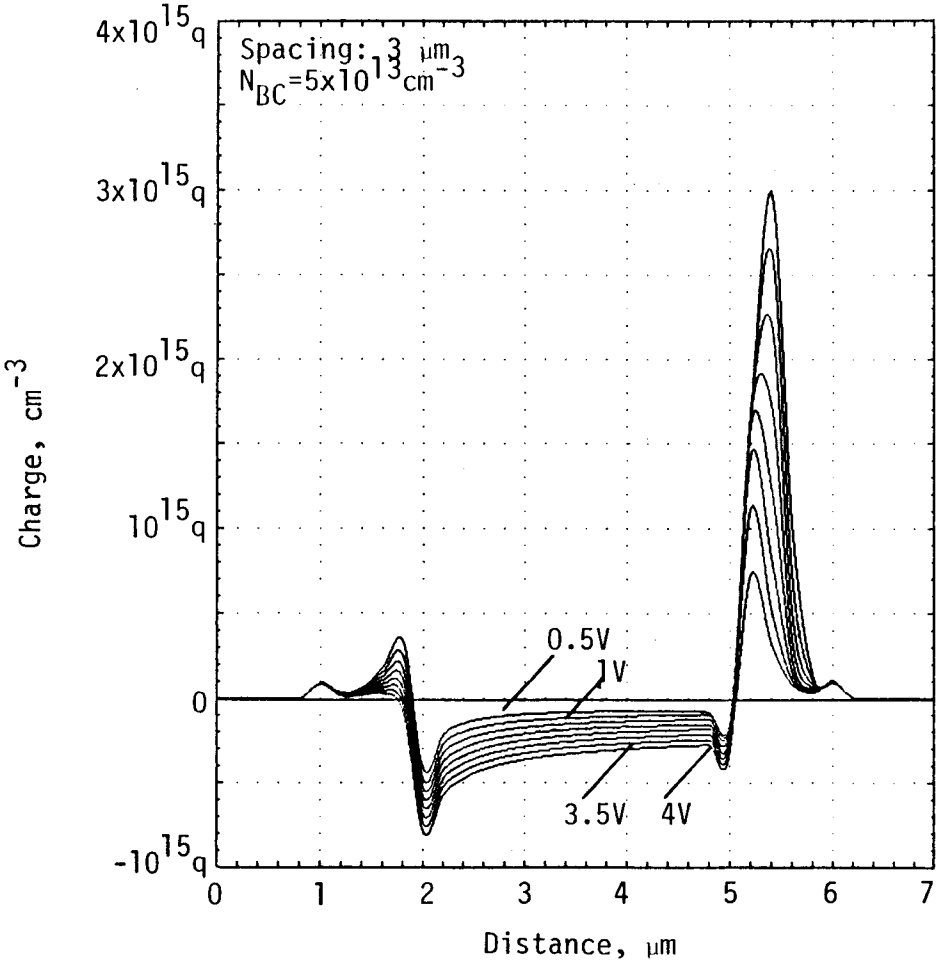


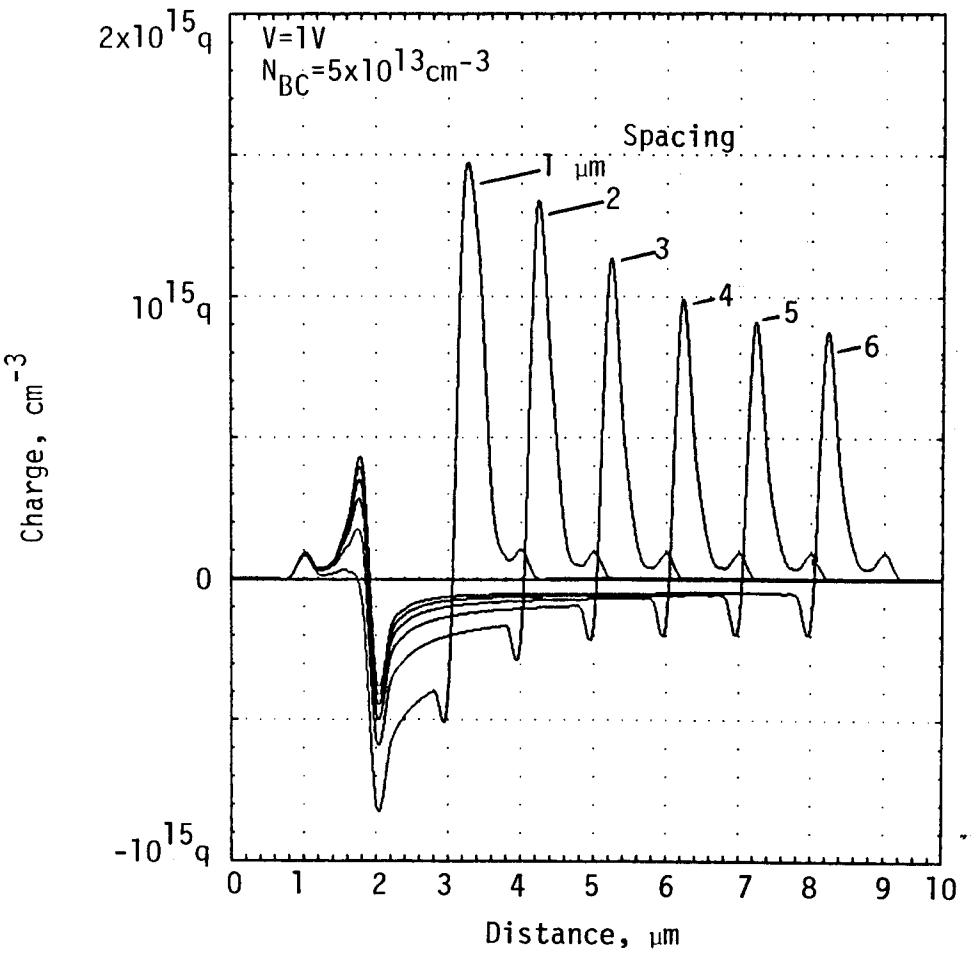
- PUNCH-THROUGH SPACE-CHARGE LIMITED STRUCTURES AS A REPLACEMENT FOR DIFFUSED RESISTORS

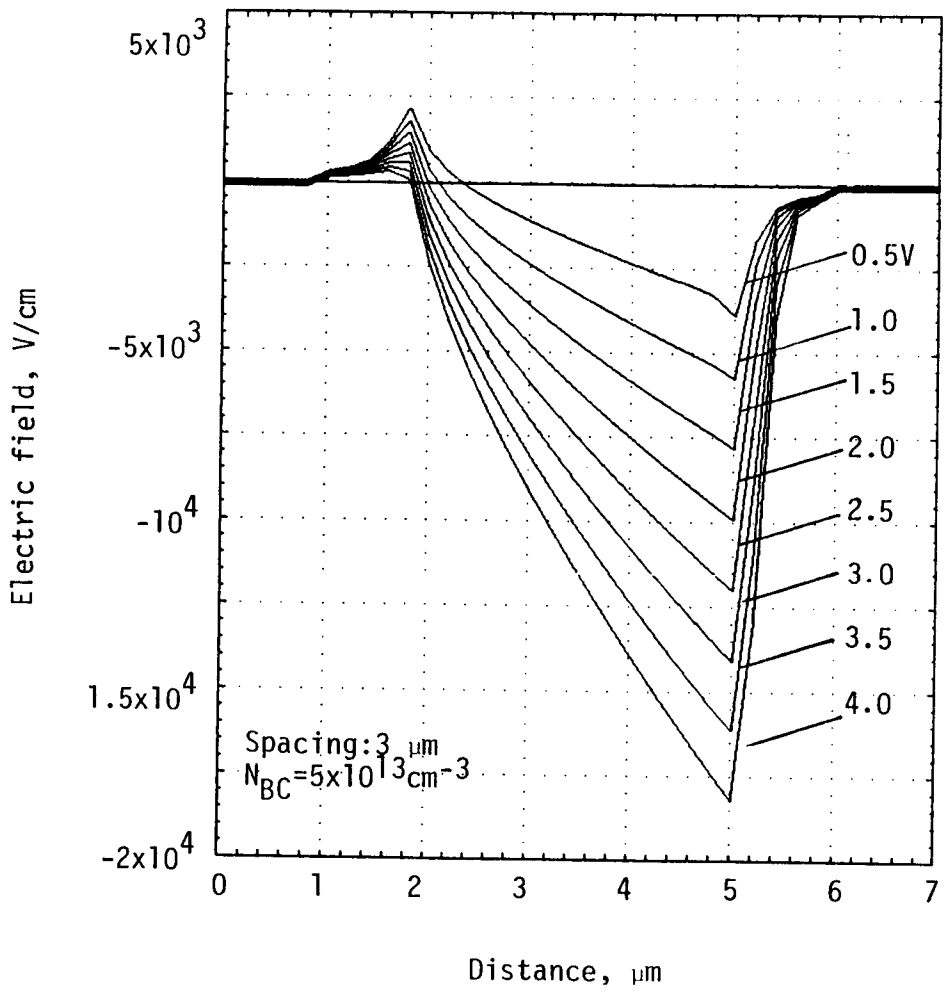
3.1 Device Simulation

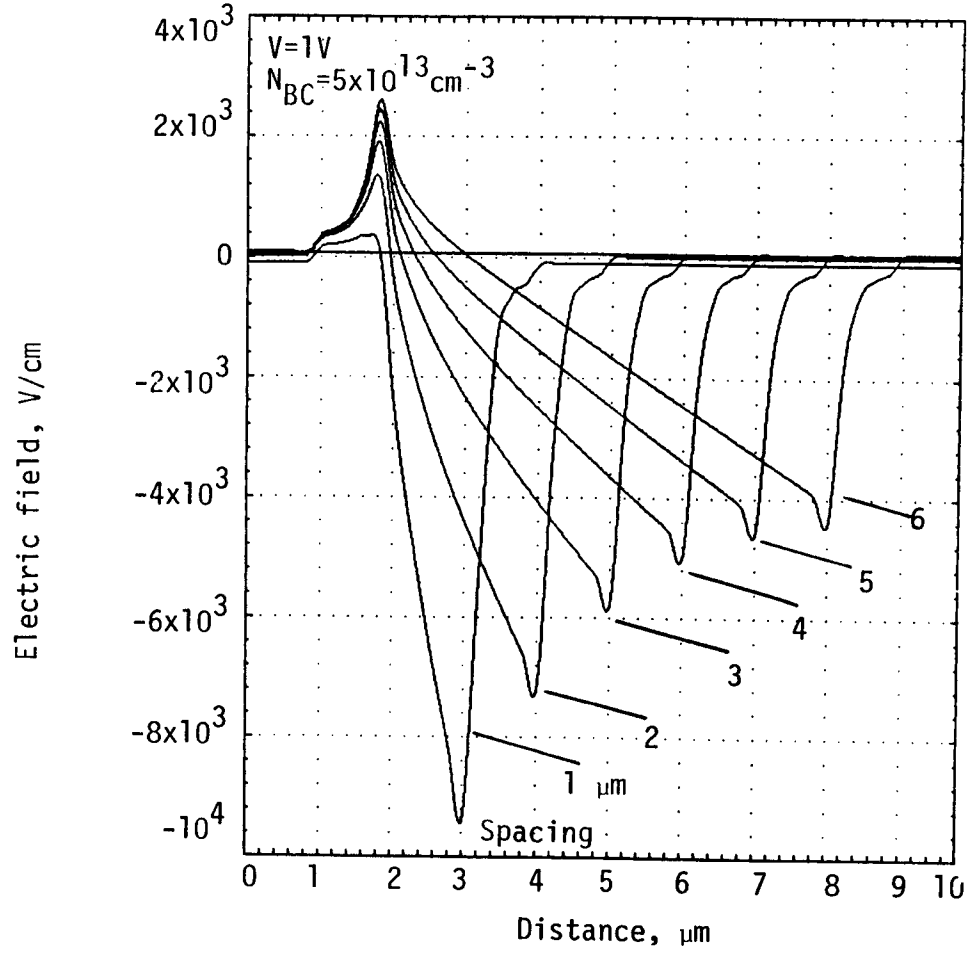

Concentration of majority carriers, cm^{-3}
10^{16}
10^{15}
10^{14}
10^{13}
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
Spacing= 3 μm
N_{BC}=5x10^{13}cm^{-3}
0 1 2 3 4 5 6 7
Distance, μm

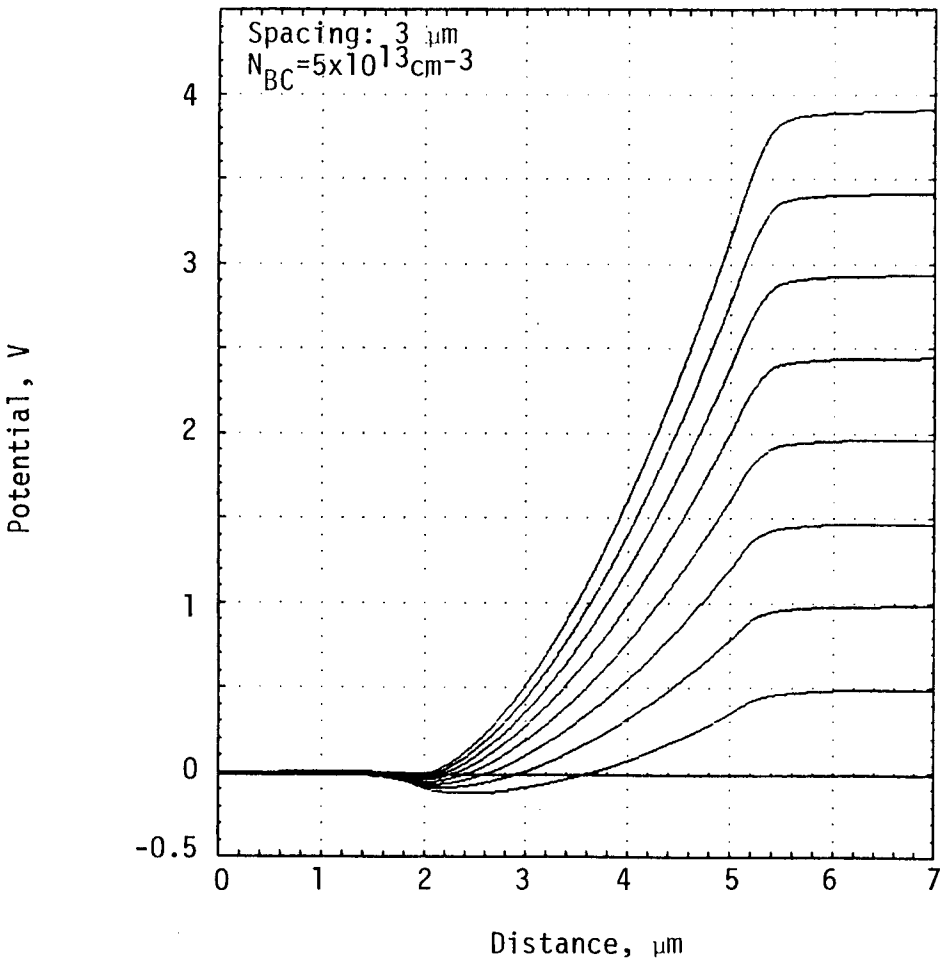

Spacing
Concentration of majority carriers, cm^{-3}
10^{16}
10^{15}
10^{14}
10^{13}
10^{12}
1 μm
2
3
4
5
6
V=1V
N_{BC}=5x10^{13}cm^{-3}
0 1 2 3 4 5 6 7 8 9 10
Distance, μm

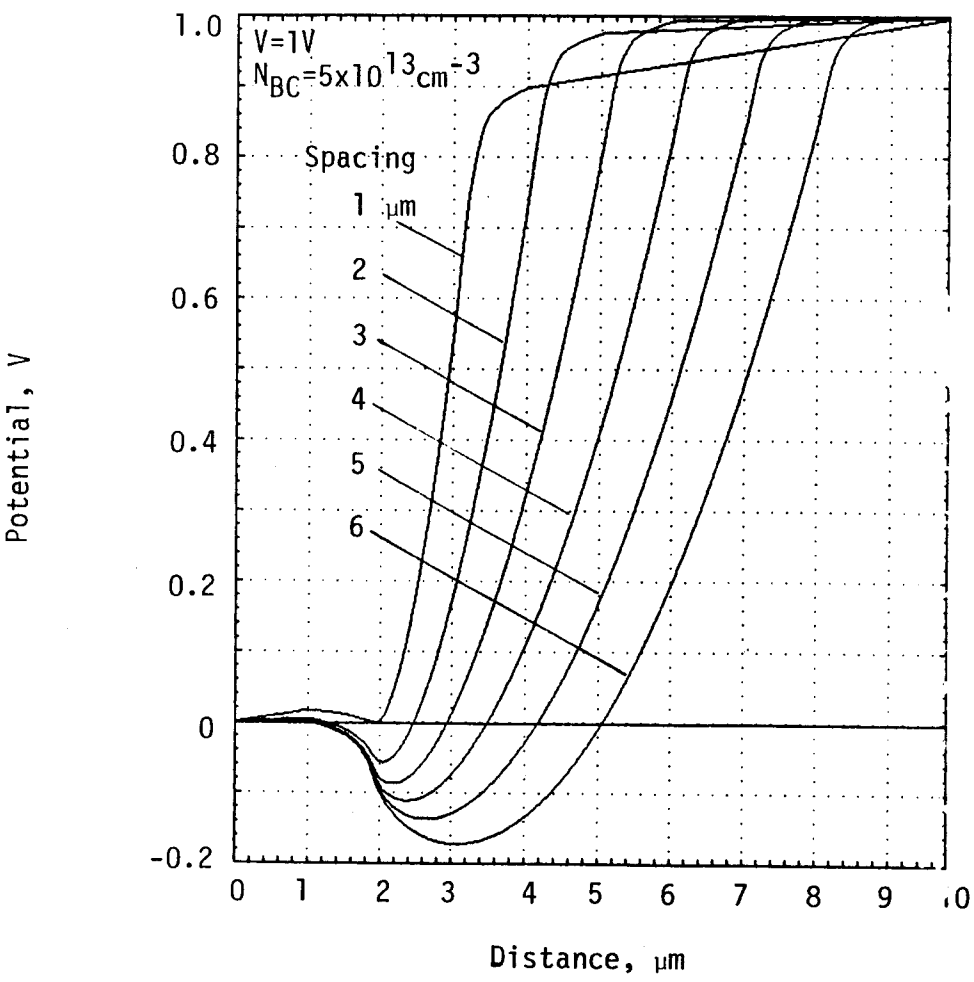

Spacing: 3 μm
N_{BC}=5x10^{13}cm^{-3}
4x10^{15}q
3x10^{15}q
2x10^{15}q
10^{15}q
0
-10^{15}q
Charge, cm^{-3}
0.5V
1V
3.5V
4V
0 1 2 3 4 5 6 7
Distance, μm


V=1V
N_{BC}=5x10^{13}cm^{-3}
Spacing
1 μm
2
3
4
5
6
2x10^{15}q
10^{15}q
0
-10^{15}q
Charge, cm^{-3}
0 1 2 3 4 5 6 7 8 9 10
Distance, μm


5x10^3
-5x10^3
-10^4
1.5x10^4
-2x10^4
Electric field, V/cm
0
1
2
3
4
5
6
7
Distance, μm
0.5V
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Spacing:3 μm
N_BC=5x10^13cm^-3

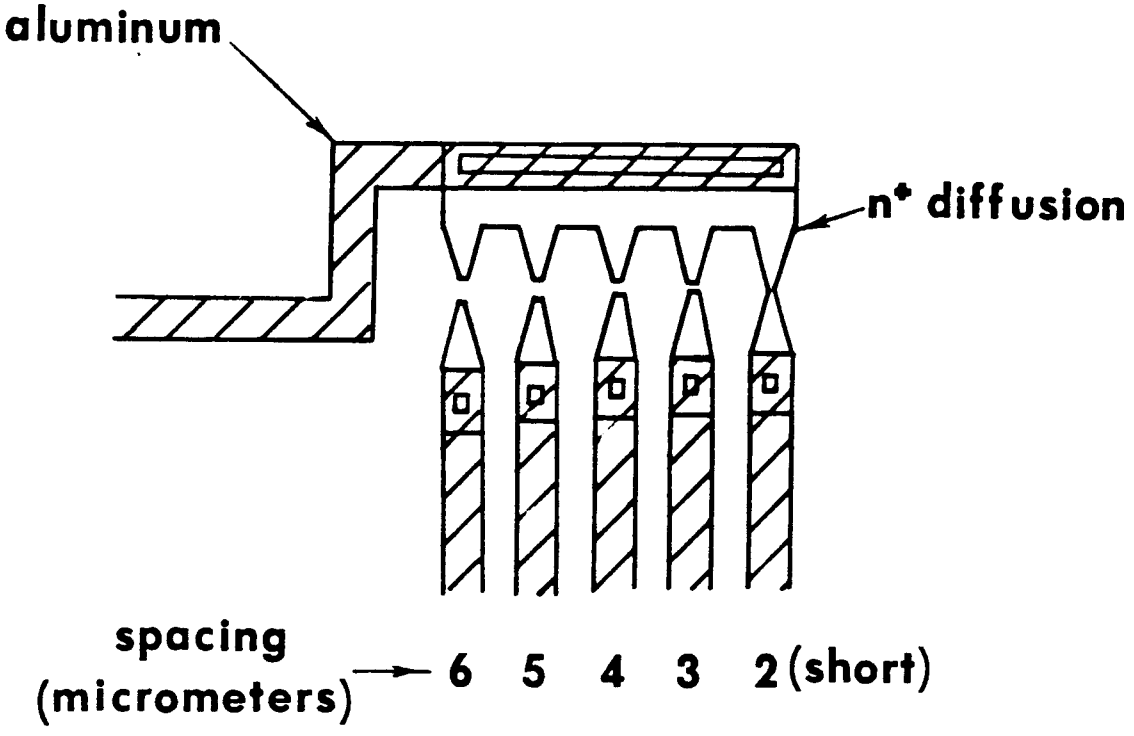

4x10^3
2x10^3
0
-2x10^3
-4x10^3
-6x10^3
-8x10^3
-10^4
Electric field, V/cm
V=1V
N_BC=5x10^13cm^-3
0
1
2
3
4
5
6
7
8
9
10
Distance, μm
1 μm
2
3
4
5
6
Spacing


Spacing: 3 μm
N_{BC}=5x10^{13}cm^{-3}
Potential, V
Distance, μm
4
3
2
1
0
-0.5
0
1
2
3
4
5
6
7

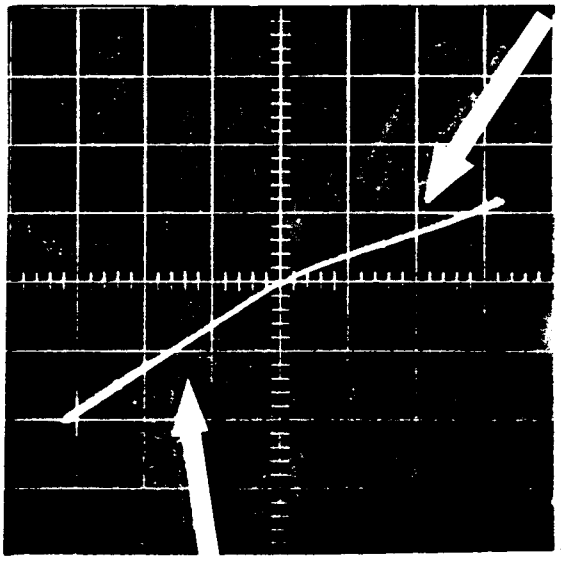

V=1V
N_{BC}=5x10^{13}cm^{-3}
Spacing
1 μm
2
3
4
5
6
Potential, V
Distance, μm
1.0
0.8
0.6
0.4
0.2
0
-0.2
0
1
2
3
4
5
6
7
8
9

3.2 Device Fabrication

- Space-charge limited load test structures
  - * Preliminary design



~60 KΩ



~33 KΩ

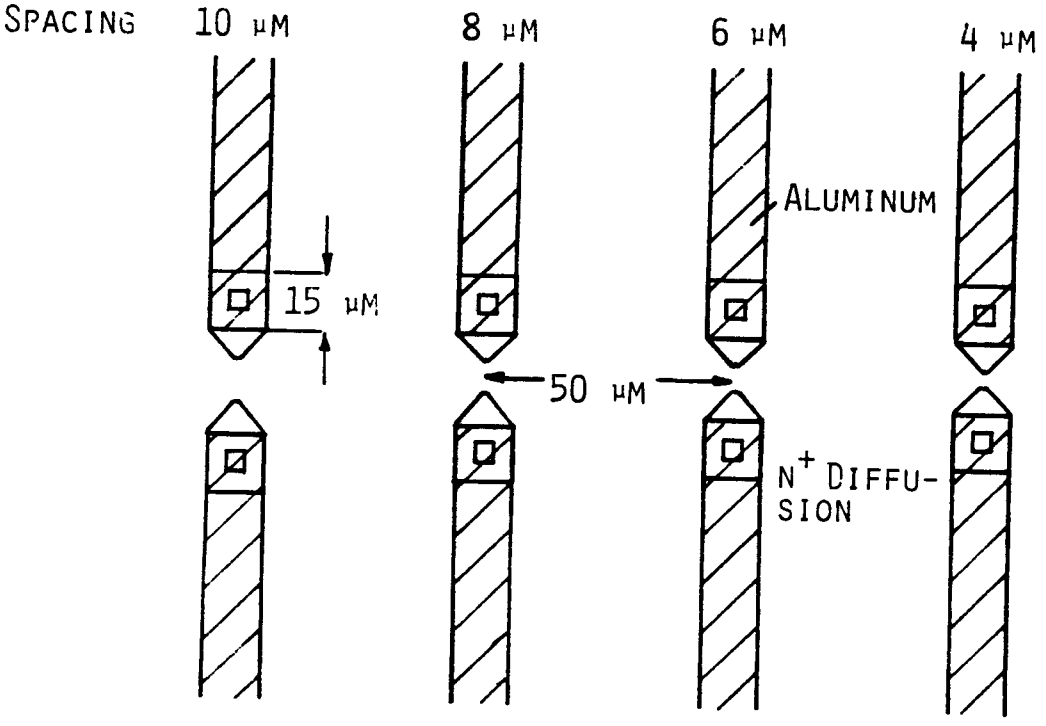
Horiz.: 10V/Div

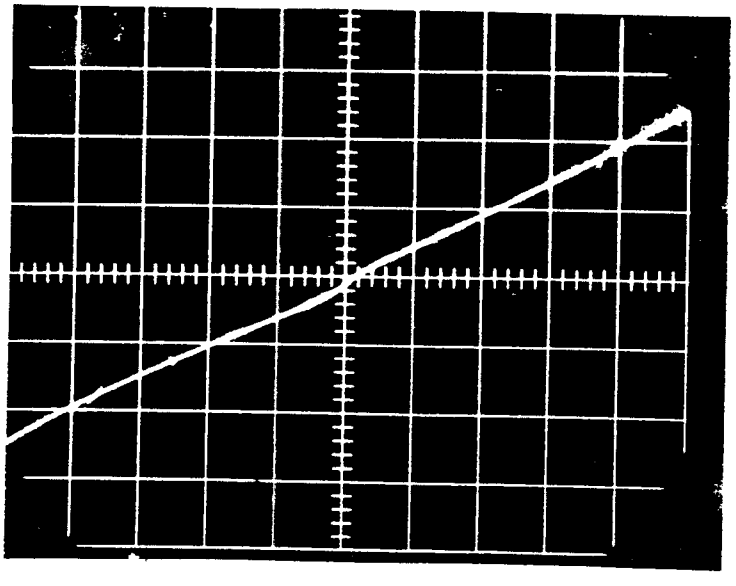
Vert.:.5 mA/Div

6 μM

$N_{BC}=5x10^{13}cm^{-3}$

- SPACE-CHARGE LIMITED LOAD TEST STRUCTURES
  - * REVISED DESIGN





4 μM

$N_{BC}=6.5\times10^{13}CM^{-3}$

HORIZ.: 5V/DIV

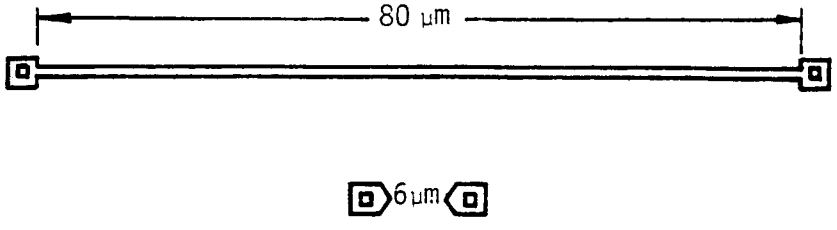
VERT.: .1MA/DIV

R ~105 KΩ

EXAMPLE

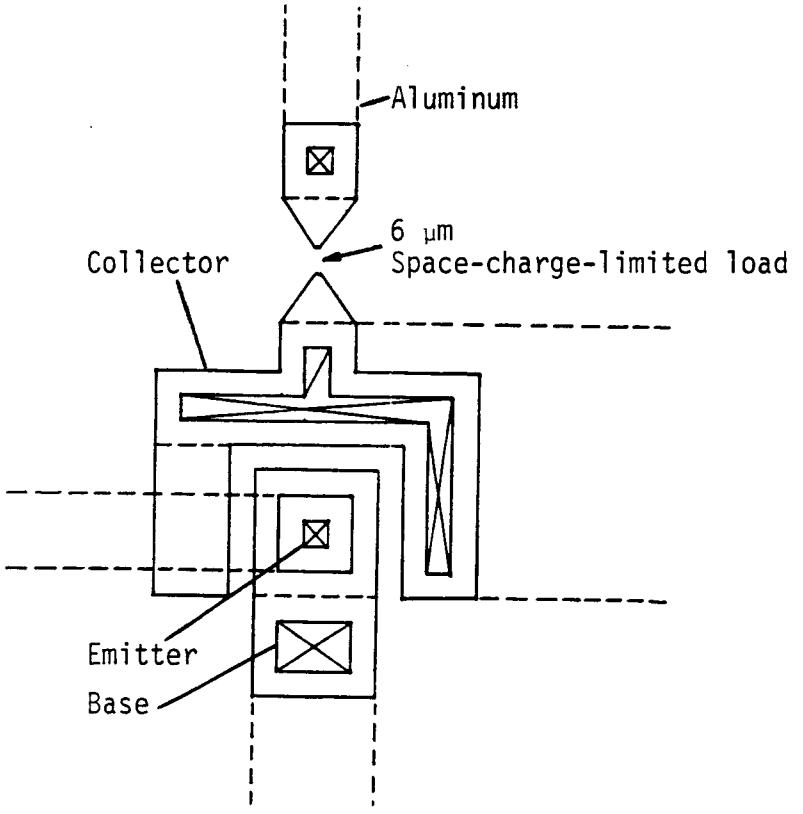
SPACE-CHARGE LIMITED LOAD SPACING (μM)	RESISTANCE VALUE (KΩ)
10	~140
8	~125
6	~120
4	~105

COMPARISON OF A 120.KΩ SPACE-CHARGE LIMITED LOAD WITH A 120.KΩ DOGBONE RESISTOR USING 1 μM GEOMETRIES. AN 80.Ω/□ (EMITTER) PHOSPHORUS DOPED REGION DEFINES THE SCLL. A 1.5 KΩ/□ (BASE) BORON DOPED REGION DEFINES THE DOGBONE RESISTOR. THE SUBSTRATE SHEET RESISTANCE IS 4.KΩ/□ ($6.5 \times 10^{13} CM^{-3}$ IMPURITY CONCENTRATION). BESIDES REDUCED CHIP AREA, THE SCLL ALSO HAS LESS SIDEWALL CAPACITANCE.

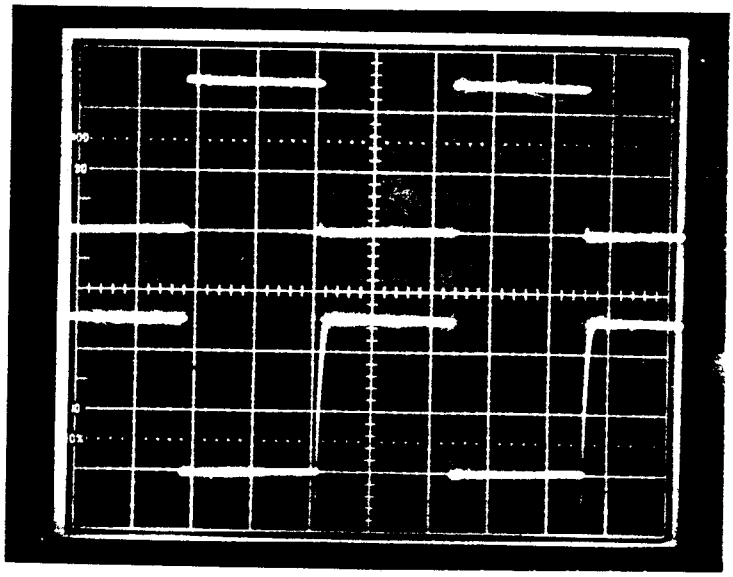


A SIMPLE INVERTER UTILIZING A SPACE-CHARGE-LIMITED LOAD WAS FABRICATED WITH THE LAYOUT SHOWN IN FIGURE A ON A P-TYPE SUBSTRATE (WITH $6.5 \times 10^{13} CM^{-3}$ IMPURITY CONCENTRATION). FIGURE B SHOWS THE INPUT 1.KHZ SQUARE WAVE (UPPER TRACE) AND THE INVERTED OUTPUT (LOWER TRACE) WITH NO PROTECTION AGAINST SATURATION OF THE TRANSISTOR. THERE WERE NO ADVERSE EFFECTS NOTED FROM THE SUBSTITUTION OF THE SPACE-CHARGE-LIMITED LOAD IN PLACE OF A CONVENTIONAL RESISTIVE LOAD.

A



B



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HORIZ.: .2MSEC/DIV

4. SUMMARY AND CONCLUSIONS

- A NOVEL CONCEPT FOR TRANSISTOR FABRICATION WAS INVENTED, INTRODUCING AN IDEA FOR PROTECTION AGAINST SATURATION. IT INVOLVES THE USE OF A STATIC INDUCTION TRANSISTOR OR A PNP SUBSTRATE TRANSISTOR AND WAS DEVELOPED BASED ON TRANSISTORS DESIGNED FOR A TRIPLE/QUADRUPLE DIFFUSION FABRICATION TECHNIQUE. SIMULATION SHOWED FASTER SWITCHING TIMES WHEN COMPARED TO SIMILAR GATES WITHOUT PROTECTION AND OPERATION COMPARABLE TO SPEED OF ECL GATES BUT WITH SMALLER POWER CONSUMPTION. FABRICATION OF SIT AND PNP SATURATION PROTECTED NPN BIPOLAR TRANSISTORS IS IN PROGRESS.

- PUNCH-THROUGH SPACE-CHARGE-LIMITED LOADS HAVE BEEN INVESTIGATED AND FABRICATED. RESISTANCES UP TO 150 KΩ ON THE AREA LIMITED PRIMARILY BY THE CONTACTS WERE OBTAINED.

- TWO COMPUTER PROGRAMS AS RESEARCH TOOLS WERE DEVELOPED:
  - A GENERAL ONE-DIMENSIONAL SEMICONDUCTOR DEVICE PERFORMANCE SIMULATION PROGRAM
  - BIPOLAR TRANSISTOR SIMULATOR PROGRAM