The SIT Saturation Protected Bipolar Transistor

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Abstract—A novel concept for a transistor was invented, introducing an idea for protection against saturation. It involves the use of a static induction transistor (SIT). Simulation showed encouraging switching times when compared to similar gates without protection, while the charge storage was practically eliminated.

I. INTRODUCTION

INTEGRATED circuits such as emitter coupled logic (ECL) using bipolar devices will retain their superiority for high-speed applications as dimensions are scaled down [1], [2]. Such circuits require relatively complicated processing, including thin epitaxial layers and buried n^+ layers. Some less complex high-speed bipolar IC processes have been developed [3], [4], including Schottky transistor logic (STL) and integrated Schottky logic (ISL).

For saturating logic gate arrays, a novel concept for transistor fabrication is proposed in this letter. The basic idea is to protect against saturation by using a static induction transistor (SIT) [5].

II. OPERATING PRINCIPLES

The operating principles of the SIT saturation protected bipolar transistor are best understood by considering the operation of a series of devices. Fig. 1 shows the cross section of a lateral collector device. The spacing between the base and the collector of this device can be made quite small using a simple double diffusion process. A positive bias applied to the collector creates a depletion region, which reaches the base region of the transistor as shown by the dashed line. A very high electric field exists between the "internal" collector and the lateral one after the depletion region is established. Carriers are swept at velocities close to saturation velocities through the depletion region, and high-speed performance results.

There are two disadvantages of such a structure. First, threshold collector voltage is required to deplete the collector region. Second, the base is shorted to the p^- substrate. The latter problem can be easily overcome by surrounding the base with an n-region as shown in Fig. 2(a). The base is then completely isolated from the substrate by a depleted region as shown by the dashed line. The device will not operate properly if the collector voltage is too low because the depletion region is not formed properly. To prevent such improper operation, the substrate should be connected to a negative potential thereby creating a permanent depletion region.

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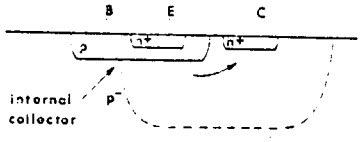
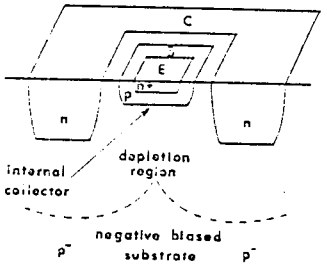
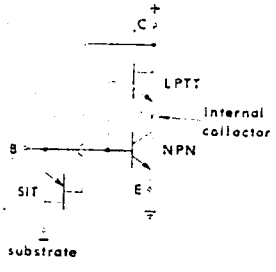


Fig. 1. A simplified bipolar structure for VLSI.



(a)



(b)

Fig. 2. (a) A modified bipolar structure for VLSI. (b) Its equivalent lumped model.

In this structure, in addition to the basic bipolar n-p-n transistor and the lateral punchthrough transistor (LPTT) [6], a p-channel static induction transistor [5] between the base and the substrate can be identified. The equivalent lumped model is shown in Fig. 2(b). The p-type base of the n-p-n transistor is the source of SIT, the n-type collector region is the gate of SIT, and the negatively biased substrate is the drain of SIT.

For large positive collector (gate of the SIT) voltages, the SIT transistor is off. If the base current of the n-p-n transistor is increased, the collector voltage decreases. As this happens, the SIT transistor will start to conduct thereby clamping the n-p-n collector voltage out of saturation by directing the excess n-p-n transistor base current to the substrate. The current flow between the n-p-n base and the substrate is determined by the potential distribution in the depletion region under the base. The potential barrier in the SIT transistor is lower than in the bipolar transistor for the same gate (base) voltage. This

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was proven experimentally [7]. The SIT and n-p-n barriers are in parallel. Because of the lower SIT barrier, the current will start to flow in the SIT before the n-p-n collector junction is driven into saturation and minority-carrier injection occurs in the collector p-n junction. The resulting clamping voltage is a function of the substrate voltage. A large negative substrate voltage will result in virtually no minority-carrier storage in the collector region. As the negative substrate voltage is increased toward zero, the minority carriers stored in the collector region increase because of the increase of the barrier potential in the SIT transistor.

The dc characteristics of SIT saturation protected bipolar transistors show no significant differences, with one exception, when compared to the characteristics of conventional n-p-n transistors. In the quasi-saturation region, the characteristics are sensitive to substrate biasing.

III. CIRCUIT SIMULATION SIT PROTECTED TRANSISTORS

A lumped transistor model is not adequate for modeling the device structure presented in Fig. 2(a). This device requires an advanced two-dimensional numerical simulation model in order to obtain reliable results. Such simulations are not available as yet. However, in the structure shown in Fig. 3(a) no direct interaction between carriers of the SIT and n-p-n transistors occurs. Therefore, the lumped model shown in Fig. 3(b) can be used to simulate the device.

The widely used SPICE2 circuit simulation program [8] was applied to the model of Fig. 3(b). A model for the SIT transistor was developed. It is based on formulas given below [5]

$$I_d = I_s[\exp(\psi_0/V_T) - 1] \tag{1}$$

where I_d is the device current, I_s is the saturation current, ψ_0 is the potential barrier height, and V_T is the electrostatic potential.

Equation (1) is valid both for an SIT transistor as well as a bipolar transistor, I_s and ψ_0 are given by formulas [9]-[11] with all subscripts referring to the four-layer bipolar transistor model of Fig. 3(b).

—For the p-channel SIT transistor

$$I_s = q\,D\,N_B\,\frac{A_{\mathrm{SIT}}}{W_{\mathrm{eff}}} \qquad \psi_0 = -\eta\left(V_C - \frac{1}{\eta}\,V_S\right) + V_Q \tag{2}$$

—For a p-n-p substrate bipolar transistor

$$I_s = q\,D\,N_C\,\frac{A_{\mathrm{p\text{-}n\text{-}p}}}{\int N_B\,dx/N_B} \qquad \psi_0 = V_{CB} + V_T \ln(N_B N_C/n_i^2) \tag{3}$$

where

- q electron charge,
- D carrier diffusivity,
- N doping concentration,

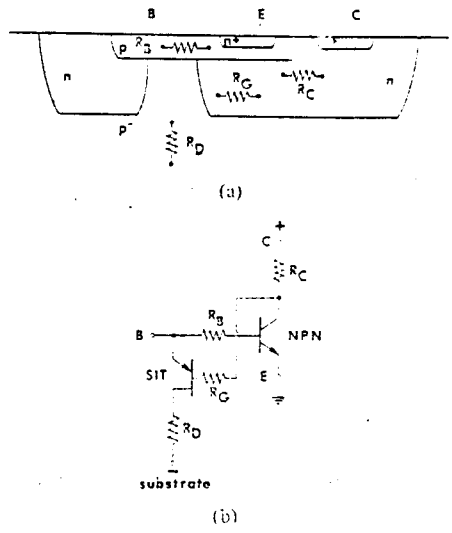

Fig. 3. (a) A triple diffusion bipolar transistor structure with SIT protection. (b) Its equivalent lumped model.

- A area,
- W_{eff} effective width of the potential barrier,
- η gate efficiency (0.1-0.4),
- V voltage,
- μ amplification factor,
- V_Q voltage drop on the space charge,
- n_i intrinsic concentration.

The amplification factor μ depends on the geometry of the device and can be calculated using empirical relations given in [11]

$$\mu = 2.5\exp(\pi D/2Z) - 1 \tag{4}$$

where D and Z are the depth and the spacing between the lateral collectors, respectively, ($\mu = 5.4$ for $D = 3\ \mu$m and $Z = 5\ \mu$m).

A simple circuit with the SIT saturation protected transistor was simulated. Encouraging switching times when compared to similar gates without protection were obtained. Fig. 4(a) shows the calculated output waveforms for an unloaded inverter when a 20-ns input pulse was applied and Fig. 4(b) presents results for a chain of such inverters subject to the same input pulse.

It has been found that the output voltage swing and the delay time of a single device are sensitive to substrate biasing. For zero substrate biasing, the storage time of a single unloaded inverter was 8 ns, but with biasing of −3-V storage time was practically eliminated. The output waveform delay was due to parasitic capacitances resulting in switching times of 1.2 ns.

The delay between the waveforms labeled 1 and 3 of the 3-stage loaded inverter was 1.4 ns for the same negative substrate biasing. Thus the propagation delay time per gate was 0.7 ns and the power delay product was less than 1 pJ. The collector voltage swing for this case was 200 mV, while the internal collector voltage swing was larger, equal to 470 mV. These results were obtained for a non-optimized structure, utilizing no Schottky clamp diodes or gold doping. The fabrication process can be simple with no epitaxial or buried layers. The structures

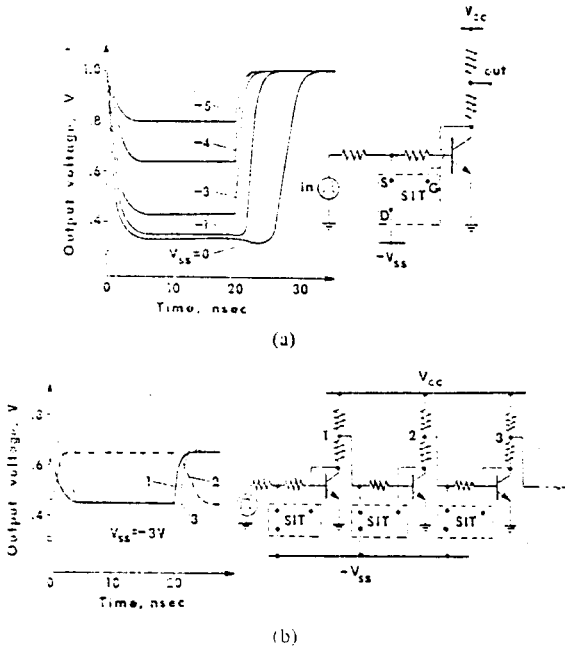

Fig. 4. (a) Output waveforms for a single-stage unloaded inverter with an SIT protected bipolar transistor. (b) For a chain of inverters with SIT protected bipolar transistors.

assumed used a 4-μm geometry. With smaller geometries, even better results are expected to be achieved.

IV. CONCLUSIONS

Simulation showed encouraging switching times for the SIT saturation protected transistor gates when compared to similar gates without protection. The collector charge-storage effect was practically eliminated. The SIT protected transistor is a substrate transistor placed under the base contact requiring no extra space. The structure is sensitive to substrate biasing. The biasing affects the voltage swings and the delay times of the gates.

SIT saturation protected bipolar transistors are being fabricated and the results will be reported elsewhere.

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