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The Punch-Through Transistor with MOS Controled Gate

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The possibility of using the subsurface punch-through mechanism controlled by MOS gate is studied. The subthreshold conduction and the punch-through are usually considered undesirable effects in MOS devices. The described device takes advantage of these effects to achieve faster operation with higher voltage. This device is suitable for integration since gate is not shorted to the substrate like in the lateral punch-through transistor described in earlier work. Two devices with 7 and 10 μm channels were fabricated and operating voltages are relatively high. The space-charge-limited current flow is the dominant mechanism in these devices.

Die Bedingungen für eine Kontrolle des Punch-through-Mechanismus unterhalb der Oberfläche durch ein MOS-Gate werden diskutiert. Die unterschwellige Leitfähigkeit und der Punch-through sind normalerweise unerwünschte Effekte in MOS-Bauelementen. Im beschriebenen Bauelement werden diese Effekte zur Verbesserung der Schaltgeschwindigkeit bei höheren Spannungen benutzt. Dieses Bauelement ist für IC-Anwendungen geeignet, da das Gate nicht mit dem Substrat verbunden ist wie in dem lateralen Punch-through-Transistor, der in früheren Veröffentlichungen beschrieben wurde. Zwei Transistoren mit 7 und 10 μm Kanallänge werden hergestellt, deren Arbeitsspannungen relativ hoch liegen. Der raumladungsbegrenzte Stromfluß ist der dominierende Mechanismus in diesen Bauelementen.

1. Introduction

The simple reduction of device geometry leads to the increase of switching time if the device current density remains the same. This effect is due to increase of the unit parasitic capacitances when dimensions are reduced [1]. Therefore, some modifications of the transistor structure or other mechanism of operation need to be analyzed. Recent work in this area has included study of the MOS analog of the Schottky gate FET [2]. This class of devices is called the subsurface or buried-channel MOS [3 to 7]. The advantage of the subsurface channel MOS device over the Schottky FET is that the subsurface channel MOS device can be fabricated as normally "off", so that its application for logic circuits is very simple. The voltage gain of this device however, is lower than that of Schottky FET transistors because of an additional potential drop across the MOS oxide. Also, as the channel becomes shorter, the voltage amplification factor becomes lower [6]. Because the carrier injection over the potential barrier known as subthreshold conduction and the space-charge-limited current becomes dominant mechanisms, and other design approach should be considered.

The semiconductor device, which has a carrier injection over an electrostatically induced potential barrier, and the space-charge-limited mechanism for normal operation is known as the static induction transistor (SIT), [8]. A very similar mechanism of operation was observed in the punch-through transistor (PTT)

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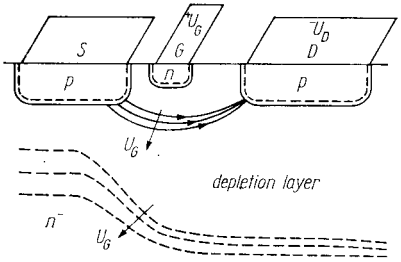

Fig. 1. The lateral punch-through transistor [3]; S source, G gate, D drain

described by Ohmi [9]. The lateral version of the Punch-Through Transistor was recently published [10] (Fig. 1). However in this device the gate is normally shorted to the substrate, and as a result, its application is limited. In this paper the buried punch-through MOS transistor which overcomes this limitation is introduced.

2. Device Structures

Subthreshold conduction and punch-through are usually considered as the undesirable effects in MOS devices. The buried punch-through MOS transistor takes advantage of these effects for normal device operation. The basic transistor structure is shown in Fig. 2. Two MOS transistors, one with a p-type channel and the other with a n-type channel share a common gate but have perpendicular channels. The surface n-type channel of one of these transistors acts as a gate for the other transistor with a subsurface p-type channel. In the case of the device described here, the buried p-type channel transistor operates in a punch-through (or SIT) mode. During normal opera-

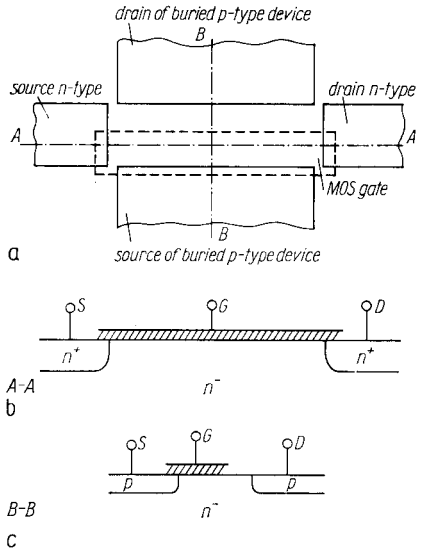

Fig. 2

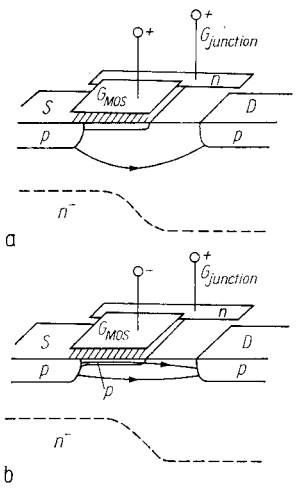

Fig. 3

Fig. 2. The buried punch-through MOS transistor. a) Top view, b) cross section of the n-channel surface device, c) cross section of the p-channel buried punch-through device

Fig. 3. Two modes of operation of buried transistor. a) Punch-through mode, b) accumulation and punch-through mode

tion, the n-type substrate, source, and drain of the surface n-channel MOS transistor are shorted and connected to a positive voltage. The source of the p-channel buried transistor is grounded and its drain is connected to a negative voltage.

For various voltages on the top MOS gate, the device has different modes of operation (Fig. 3). With a positive voltage on the MOS gate, an n-type channel is induced which is positively biased by internal connection to its drain or source (Fig. 3a). This n-type channel operates as a gate similar to the lateral punch-through transistor [10] where the n-type channel is fabricated by diffusion process (Fig. 1). The voltage for the punch-through between the p-type device source and drain is controlled by the positive voltage on the n-type induced gate (channel) which is also the substrate voltage. Changes in this n-type channel voltage thus will modulate the current flow between the p-type source and drain. A similar effect was observed by Richman [11], but the induced gate effect was not considered and the results were interpreted as an effect of direct substrate interaction.

If a negative voltage is applied to the MOS gate, the surface will be inverted to p-type, the n-type positively biased channel will not exist, and the punch-through current will flow for relatively small voltages between the p-type device source and drain. In addition to the punch-through current, current may also flow in the MOS p-type surface channel near the surface. The device will operate in the accumulation-punch-through mode [12].

3. Theoretical Considerations

In punch-through the device current may be determined using the space charge conduction law. For small and moderate electrical fields, the device drain current I_D, is given [10] by:

$$I_D = \frac{9}{8} \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3} U_D^2 , \tag{1}$$

where μ = electron mobility, L = effective distance between source and drain of p-type device, $A = ZW$ = effective area of current flow, Z = p-type channel width, W = effective area depth of p-type channel.

In high electrical field, where the velocity of the carriers are equal to the saturation velocity, the drain current I_D is given [10] by:

$$I_D = 2\varepsilon_{Si}\varepsilon_0 v_s \frac{A}{L^2} U_D , \tag{2}$$

where v_s = saturation velocity of carriers. The transconductance G_m can be calculated as:

$$G_m = m \frac{dI_D}{dU_D}, \tag{3}$$

where m = amplification factor (depends on device geometry). Using (3) and (1):

$$G_m = m \frac{3}{\sqrt{2}} \sqrt{I_D \frac{\mu \varepsilon_{Si} \varepsilon_0 A}{L^3}} . \tag{4}$$

One can see that the transconductance is a function of the drain current much like an MOS transistor, whose G_m is given by:

$$G_m = \sqrt{I_D \frac{2C_0 \mu Z}{L^2}} , \tag{5}$$

where $C_0 = \varepsilon_{0x}\varepsilon_0/X_{0x}$; Z channel width, L channel length, X_{0x} gate oxide thickness.

For still higher electrical fields, using (3) and (2), one may see that G_m is no longer a function of drain current, and depends on device geometry only:

$$G_m = m \frac{2\varepsilon_{Si}\varepsilon_0 v_s A}{L^2} \tag{6}$$

It is interesting to compare G_m for MOS and punch-through Transistors (PTT). Using (4) and (5) one can obtain an expression for the ratios of the G_m's of two device types, K:

$$K = \frac{G_{m\text{PTT}}}{G_{m\text{MOS}}} = \frac{3}{2} m \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{0x}} \frac{X_{0x} W}{L^2}} . \tag{7}$$

Since $\varepsilon_{Si}/\varepsilon_{0x} = 3$, and if we assume that effective channel depth W is equal $W = L/2$ [3] then:

$$K = \sqrt{\frac{27}{8}} m \sqrt{\frac{X_{0x}}{L}} . \tag{8}$$

Usually the G_m for MOS transistors will be much higher than the G_m for the PTT. However, if the only channel length L of the PTT is reduced and the device geometry is such that the amplification factor m is large; therefore, the G_m of the PTT will be comparable to or even higher than that of the MOS transistor. The MOS oxide thickness can be also reduced; however, this reduction is limited by applied voltages and the unit parasitic capacitances increase significantly at same time.

4. Experimental

Two buried p-type device structures with different geometries were fabricated (Fig. 4). The fabrication facilities available limited the devices to relatively large geometries. Therefore, in order to observe the desired effects a very low substrate background impurity concentration with high resistivity (600 Ωcm) was chosen. Device No. 1 had a source–drain spacing equal to 7.5 μm covered by the MOS gate. The source–drain spacing in device No. 2 was 10 μm and only part of this region close to the source was covered by the MOS gate. The drain characteristics for both structures are shown in Fig. 5a and b. The device No. 1 has lower operation voltages; also the voltage gain is smaller. The same characteristics with a log-linear scale are shown in Fig. 6a and b. In the low current range, subthreshold conduction is observed. The I–U characteristics follow the exponential law and the carriers flow through the electrostatically induced potential barrier [13]. In the higher current range the space-charge-limited flow is the dominant mechanism. In both regions the characteristics are similar to the characteristics of the lateral punch-through transistor [10] rather than MOS type transistor.

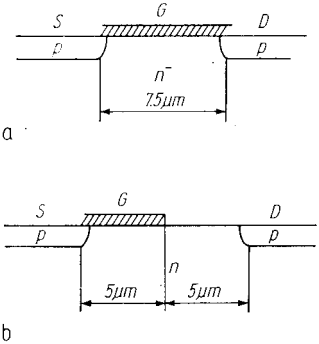

Fig. 4. The cross section of fabricated devices. a) Device No. 1 with 7.5 μm spacing, b) device No. 2 with 10 μm spacing and partly covered channel

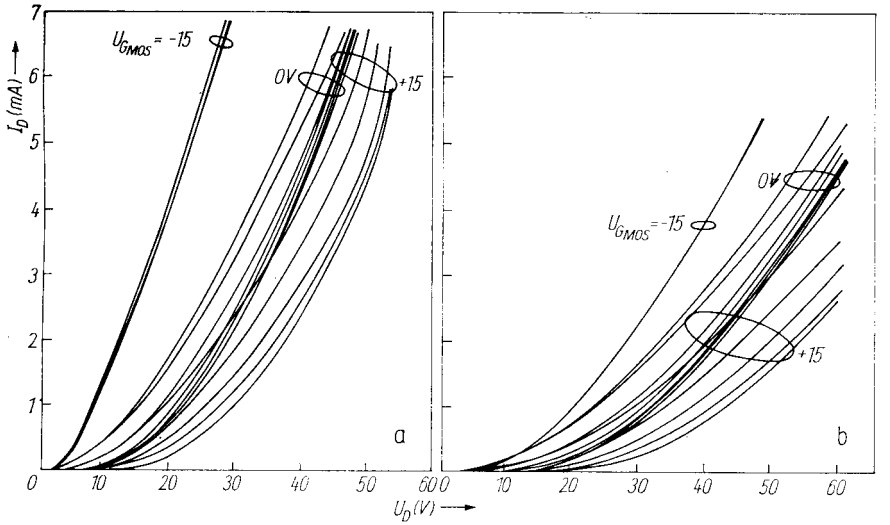

Fig. 5. The drain characteristics with the MOS gate voltages equal +15, 0, −15 V and the n-type gate voltages as parameters (2 V per step). a) Device No. 1, b) device No. 2

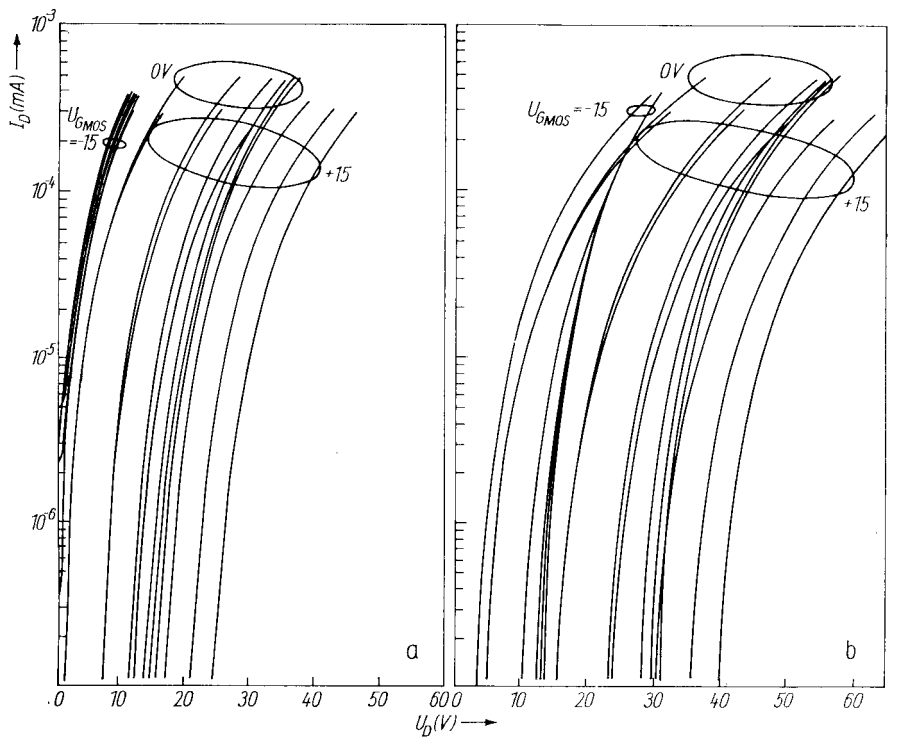

Fig. 6. The drain characteristics drawn in log-lin scale with the MOS gate voltages equal +15, 0, −15 V and the n-type gate voltages as parameters (2 V per step). a) Device No. 1, b) device No. 2

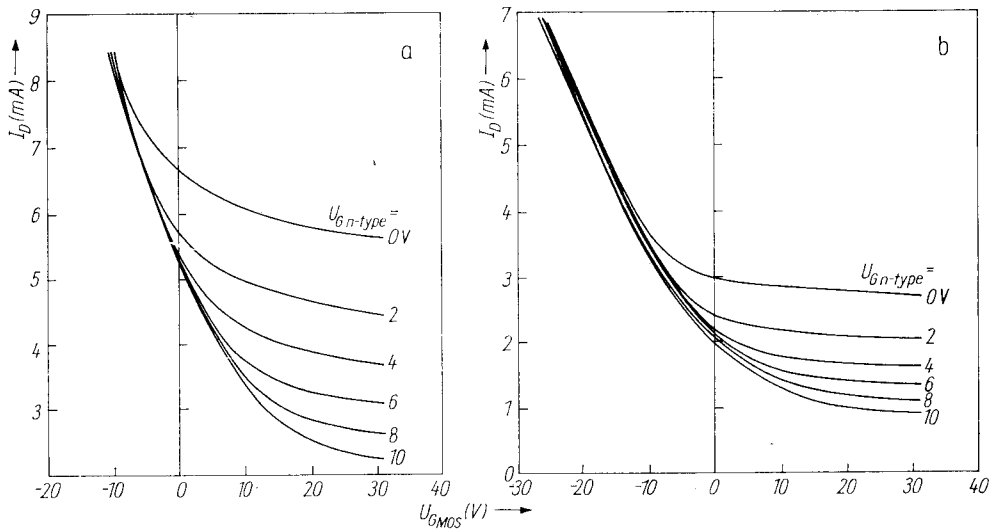

Fig. 7. The MOS gate characteristics with the n-type gate voltages as parameters and the fixed drain voltage equal 40 V. a) Device No. 1, b) device No. 2

To investigate various modes of transistor action, it is convenient to draw the gate characteristics for fixed drain voltage. Such characteristics of device No. 2 are shown in Fig. 7b. For negative voltages on the MOS gate, the drain current is almost independent of the substrate (drain and source of n-type device) voltage, but the MOS gate voltage has a strong effect on drain current. This is the case when the MOS gate controls the space charge limited drain current (Fig. 3b) [6 to 8].

For positive voltages on the MOS gate, the n-type region is induced under the surface and acts as an additional gate. This induced region is positively biased by the substrate (drain and source of n-type device) voltage. The terminal voltages induce a potential barrier whose height is controlled by the these voltages and a carrier space charge, which is proportional to the current density. This mode of operation is similar to that of lateral punch-through transistor (Fig. 3a) [10], in which the variation of the large positive voltages on the MOS gate has almost no effect on drain current.

5. Discussion

Two modes of operation of buried MOS punch-through transistor have been shown. The real advantage of this device can be expected to be seen when dimensions will be scaled down to the submicron range. Then the biasing voltages will be lower even if the impurity doping level will increase. Two device geometries were considered (Fig. 4). The device with an additional space between gate and drain (Fig. 4b) has the larger voltage gain. In this device between the gate and drain the space-charge region of moving carriers exists. This space charge reduces the effect of drain voltage and leads to higher transistor gain, and it should not limit the device speed since the carrier transit time across this space charge region is extremely small. (Assuming saturation velocity, it is 10 ps/μm of gate–drain distance). In case of the standard MOS device, the punch-through phenomenon limits the device dimensions; this effect can be significantly reduced by increasing the impurity concentration in the substrate. This, however, leads to large parasitic capacitances and to lower speed

of operations, because the unit capacitances increase even more than from simple shrinkage of devices. The subsurface punch-through MOS transistor does not have this limitation because the parasistic capacitances are very small. It may be considered as an interesting alternative for the VLSI integrated device structure. The methods to improve voltage gain of this transistor are under current investigation.

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