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Education for Microelectronics Manufacturing

abstract

This presentation by the head and faculty members of the Department of Electrical and Computer Engineering at the University of Arizona, Tucson, Arizona describes the courses in microelectronics offered by the department. These courses constitute an internationally recognized educational program in microelectronics aimed at providing students with the comprehensive knowledge needed for the design, fabrication and use of microelectronic components. The theoretical background is augmented by practical experience gained in fabrication of integrated circuits in the department's microelectronics laboratory, and by design projects pursued in the well-equipped Computer Engineering Research Laboratory.

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Microelectronics manufacturing is fueling the information handling and processing revolution which is sweeping the world by impacting on virtually all aspects of human endeavor. Universities have not been able to provide enough properly prepared microelectronics manufacturing engineers to meet the needs of industry. Therefore, it is most appropriate that a tutorial session of the SME ETMAS '83 Conference be devoted to this important and timely topic. The objectives of this presentation are to provide the listeners with: 1) the results of a survey to show what is happening nationally in microelectronics manufacturing education, 2) specifics about the internationally recognized UA program in this area, and finally 3) to seek advice, suggestions, and aid from the practitioners regarding future emphasis, programs and plans.

The session will be presented in 9 parts as outlined below:

1. Dr. Roy H. Mattson, Professor and Head of the University of Arizona Electrical and Computer Engineering Department will summarize the results of a survey of all EE Department Heads in the U.S. The survey requested information about courses being offered in microelectronics manufacturing and the number of students involved. He will also discuss the basic concepts guiding the UA program which will be described by the rest of the speakers.

2. Dr. James N. Fordemwalt, Director of the UA Microelectronics Laboratory, will describe UA microelectronics education as related to processing as well as the facility itself.

3. Dr. Bogdan Wilamowski, Visiting Professor of ECE, will describe the devices oriented aspects of the educational program.

4. Dr. William J. Kerwin, Professor of ECE, will present the circuits related parts of the program.

5. Dr. Jakob H. Hohl, Adjunct Professor of ECE and an IBM Advisory Engineer, will describe the integrated circuit engineering related parts of the program.

6. Dr. Fredrick J. Hill, Professor of ECE, will describe the Computer Aided Design aspects of the program as related to VLSI design.

7. Dr. Olgierd Palusinski will describe the CAD-Simulation aspects of the program with emphasis on circuit simulations.

8. Dr. Douglas J. Hamilton, Professor of ECE, will describe the new M.S. degree granting program in Electronic Packaging Engineering which will become an integral part of the microelectronics manufacturing educational program.

9. Dr. John S. Ramberg, Professor and Head of the Systems and Industrial Engineering Department, will describe the existing educational program in that department as well as plans for the future.

INTRODUCTION AND SURVEY RESULTS

The consensus opinion of educators concerned with microelectronic manufacturing is that optimization of such manufacturing requires an intimate relationship between all aspects of the chip design and fabrication activities. Thus, microelectronics manufacturing education must show the students how engineering design relates to manufacturing. This has been a basic tenet of the UA program. Other institutions would usually do the same thing except for the lack of talent and resources needed to create the necessary laboratory environment. Industry has recognized this problem and is initiating actions to deal with it such as the AEA Fellowship Program, the Semicon-

ductor Research Council Program of the SIA, and the IBM Manufacturing Technologies Program. These will soon have a major impact on microelectronics manufacturing education.

MICROELECTRONICS MANUFACTURING EDUCATION IN THE USA

A brief questionnaire was sent to 300 EE department heads in the USA asking for information about their courses in microelectronics manufacturing. The information requested was for the number of courses, the number of students and a one sentence course description. There were 95 responses and 36 of these had no courses in microelectronics manufacturing.

One of the respondents from Rochester Institute of Technology reported on a unique B.S. degree granting program in Microelectronic Engineering.

> "The object of the Microelectronic Engineering program is to provide the students with the basic skills in optics, chemistry, photoscience, electrical engineering, computers, statistics and mathematics needed to be productive employees in a microelectronics processing facility. We intend to emphasize the photolithographic aspects of I.C. processing. Due to RIT's expertise in photographic science, RIT can offer a truly unique program with a photolithographic emphasis.
>
> Most of the courses in the curriculum emphasize basic principles of microelectronic processing. Only one of the courses is primarily concerned with technology (I.C. Processing Lab). As a result we feel that graduates of the program will have the broad technical background necessary to continue their study of microelectronics in graduate school as an alternative to immediate industrial employment."

The rest of the departments, 58 in all, reported offering courses in microelectronics manufacturing. Of these 43 reported courses with laboratory involvement. The other 15 reported lecture courses only.

The most extensive of these 58 reported 8 courses with 320 students involved at San Jose State University with laboratory experiences included. Nine of the institutions with laboratories reported emphasis on hybrid activities such as thick film processing. Eight of the institutions reported using the Carver-Meade material on VLSI design.

The 58 institutions offer 98 courses with 2187 students involved. Thus, the average institution offering such courses has about 38 students in 1.69 courses. If the same number of courses and students are distributed over the 95 respondents, then about 23 students enroll in about 1 course per institution.

It is interesting to note that as many as 58 institutions feel they should offer 98 courses in microelectronics manufacturing with a result of over 2,000 students involved. Five institutions reported plans for adding such courses and Worchester Polytechnic reported plans to use an industrial laboratory as part of the program. Some respondents expressed concern about the availability of resources and talent to develop such a course.

I.C. PROCESSING COURSES

Dr. James N. Fordemwalt

The University of Arizona offers two courses in microelectronics processing. The first of these, EE 457, Introduction to IC Laboratory, is a senior elective. It may also be taken by entry level graduate students who did not take it or an equivalent course as an undergraduate. It is not assumed that the students have any prior experience in fabricating silicon integrated circuits, so taped lectures on the fundamentals of IC processing constitute the first few meetings of the lab. After that the students perform seven experiments in the laboratory. Of these the first six are relatively short, taking from one to three lab periods. In these the students learn the basic fundamentals of processing. These experiments encompass wafer cleaning, diffusion and diffusion evaluation, oxidation and oxidation evaluation, metallization and photolithography. The first six experiments take approximately the first half of the semester. The seventh experiment is the fabrication of an ECL gate. The students are given a set of wafers with an epitaxial layer already grown and set of masks. The balance of the semester is spent fabricating and testing the ECL gates.

An intensive, two-week version of EE 457 is offered as a "hands-on" wafer processing course for anyone desiring to learn the basics of IC processing. It is offered for credit or non-credit by arrangement anytime during the year. This course has proven particularly popular with attendees from not only many places in the USA but also from Germany, UK, India, China, Korea and Japan.

The Advance IC Laboratory Course, EE 558, is offered second semester each year only. It is a non-structured project oriented course. In this course students are organized into project groups in which they "start from scratch." They determine the circuit function they wish to perform then decide on the process technology to be used. From there they design the circuit, computer simulate it to confirm operation, lay out the chip, cut the rubylith, make the masks and process the wafers. Finally, they test the wafers and confirm operation. The process technologies presently available in the lab include bipolar linear and digital (ECL), metal & Si gate CMOS, and metal & Si gate N-MOS with enhancement and depletion mode transistors.

BETTER UNDERSTANDING OF SOLID STATE DEVICES TO IMPROVE MANUFACTURING PROCESSES

Dr. Bogdan M. Wilamowski

The University of Arizona's teaching program in the field of semiconductor device design can be divided into four different levels. First, the basic level course (351) gives our students the general knowledge about the most commonly used semiconductor devices, terminal characteristics and mathematical models for the purpose of circuit analysis and design.

Students interested in microelectronics can take advanced undergraduate courses at the second level (452, 457, 458). One of these courses, 452, is the Solid State Device Design where basic device physics and design methodology are presented. The manufacture process variation is also analyzed so the optimal design can be proceeded. Self-alignment methods using different techniques (local oxidation of silicon, poly silicon, silicon nitride, dopped silicon oxide and others) are presented in order to improve device parameters and yield of integrated circuits. The special device geometry and the special mask design rules are also discussed. Obtaining integrated circuits insensitive to mask alignment, even if the self-alignment process is not

used, is possible because the external parameters of IC are rather function areas ratio of internal devices, not device parameters.

At the graduate level, the courses for better understanding of microelectronic and other electron devices are offered. The Microelectronics course (551) deals with the circuit aspect of device design. The Physical Electronics course (556) helps students to understand the physics of such manufacturing processes as diffusion, plasma etching and deposition- low pressure effects and others. It is our hope that after this course the engineer will be able to modify the basic manufacturing process in order to improve the device and IC parameters, as well as to improve the yield.

The most advanced device aspect course (653) deals with the basic physical phenomena in semiconductors; each of the phenomenon can create useful semiconductor devices. For example, carrier velocity lowering with increasing the electrical field is used in the Gunn diode. Limited carrier velocity allows us to create microwave oscillators (IMPATT and TRAPATT diodes). The depletion layer thickness variation with applied voltage plays a basic role in varicap and varactor diodes, and in JFET as well. The carrier-injection over the potential barrier is the basic mechanism in the bipolar transistor, but also the other devices like Static Induction Transistor or Punch-Through Transistor may use the same mechanism for their operation. Also, in the case of a VLSI short channel MOS transistor in subthreshold mode, the carrier injection over a potential barrier is the main conduction mechanism.

The purpose of the advanced level device is to prepare our students not only to understand all useful and parasitic effects in existing devices, but also to be able to create novel devices which will use new combinations of physical phenomena in semiconductors.

CIRCUITS EDUCATION PROGRAM

W. J. Kerwin

The circuits education program in the Electrical Engineering Department at the University of Arizona begins with EE 101 as a freshman first course in electrical engineering. This is an introductory course in electrical engineering emphasizing the practice of electrical engineering. The second course is EE 171 emphasizing digital circuits and including computer organization. This is followed by EE 221, the first course devoted specifically to steady state AC and DC circuit analysis, and it includes some work on magnetic circuits and transformers.

In the junior year, EE 321a,b complete the required undergraduate circuit analysis curriculum. This series introduces the Laplace transform, the Fourier series and transform methods in general. A beginning in passive and active network synthesis is included in 321b and an introduction to sensitivity is included. This is, of course, of great importance to manufacturability.

At the conclusion of EE 321b, the computer program SPICE is introduced and used to analyze networks for both steady state and transient response, and in particular to study the effects of component tolerances and temperature coefficients and the widely different element sensitivities in both passive and active circuits. The effect on manufacturability of terminated vs. unterminated networks is also included.

Concurrent courses to EE 321a,b, are EE 351a,b which include the design of electronic circuits with emphasis on practical modeling of active devices and including amplifiers, rectifiers, modulators and oscillators. These are also required courses.

Senior elective courses in circuits are EE 422 on active and passive filter design, which includes sections on passive and active element sensitivity, and EE 426 on signal processing which also includes a study of active RC circuits and their sensitivities.

At the graduate level, EE 552 and EE 553 study the practical design (that is, low sensitivity design) of broad band active low pass circuits (EE 552) and active band pass circuits (EE 553). EE 552 and EE 553 also include feedback amplifier design and control system design. Another circuit course emphasizing sensitivity (manufacturability) is EE 522, on active RC filters. This course emphasizes computer aided design and computer use in sensitivity matrix calculations.

INTEGRATED CIRCUIT ENGINEERING AND LAYOUT

Dr. Jakob H. Hohl

Integrated circuit design is different in many ways from design with discrete components. In integrated circuits the selection of circuit components is limited to transistors, diodes, resistors and small capacitances. The cost relations between these elements are entirely different, favoring integrated transistors very strongly over integrated resistors or capacitors. The element parameters within a chip can be expected to be highly uniform, while large variations of their characteristics from chip to chip occur. Also, integrated circuits contain an abundance of parasitic elements, which have no counterparts in circuits with discrete components.

The results of the circuit design activities are typically represented by schematic diagrams and mathematical expressions. These descriptions emphasize the conceptual and functional aspects of the design, while they are usually incomplete inasmuch as they disregard most parasitic elements, which will be present in the integrated circuit.

The layout can be considered as the overlap of the design and the fabrication process of the integrated circuit. While the wafer processing steps establish the global physical and electrical parameters, the layout determines the characteristics of the individual components and of the parasitic elements of the physical circuit. On the surface the layout activity may appear simply as that of cramming a given number of components into the smallest area possible, but in reality it comprises many diverse, crucial, and often intricate considerations of circuit design. The layout also must be compatible with the capabilities of the fabrication steps in order to ensure a reasonable yield of good, reliable circuits. The processing limitations are reflected by the layout ground rules, which specify all minimum dimensions of islands and spaces in the masks for the photolithographic process steps.

The Integrated Circuit Engineering and Layout course has the objective of acquainting the students with the engineering problems associated with the layout of integrated circuits in both, bipolar and MOSFET technologies, and of teaching them the methods for avoiding or solving these problems.

The course starts out with a review of the theory of semiconductor devices and integrated circuit processing steps, with emphasis on mask-making and photolithography, using the processes practiced at the University of Arizona Microelectronics Laboratory as an example. In these lectures the minimum structural dimensions for reliable circuit elements as well as the dimensional tolerances of the patterns photolithographically engraved onto the wafer are established.

These geometric parameters are then used to demonstrate the development of consistent layout ground rules for bipolar and MOSFET technologies for a "statistical three sigma design." This means that the statistical dependence or independence of dimensional tolerances is considered in determining cumulative tolerances and that the minimum feature sizes still allow for variations of the dimensions of the engraved patterns up to three standard deviations of the respective distributions.

Circuit design and layout techniques for bipolar circuits are studied mainly by the example of a commercial operational amplifier. We acknowledge the support of Burr Brown Research Corp. of Tucson, Arizona, who furnished schematic diagram, photomicrograph, and all mask drawings as well as process specifications for one of their operational amplifier designs. We also have been fortunate to obtain six video-taped guest lectures by William F. Davis, Senior Technical Staff Member, Motorola Semiconductor Products, Inc., Mesa, Arizona, on more subtle layout related problems in analog bipolar integrated circuits. (Video tapes of these lectures are available from MICROCAMPUS, University of Arizona.)

Circuit design and layout techniques for MOSFET circuits are taught mainly with examples of digital circuits. The students are introduced to computer-aided design (CAD) techniques by solving MOSFET circuit layout and design problems using UAMASK and SPICE, two programs residing on the CYBER computer at the University Computer Center. UAMASK is a simple graphics program, which provides an understanding of the basic principles of layout with interactive graphics systems. The circuit simulation program SPICE is used to calculate transient responses of simple MOSFET logic circuits, giving the student insight into the characteristics of these circuits as well as some appreciation of the realities of a CAD environment. Simulations of circuits at the limits of processing and geometrical tolerance ranges vividly demonstrate the trade-offs between yield of good circuits and tight performance tolerances.

The course is offered through IETS (Interactive Education Television System) and MICROCAMPUS of the University of Arizona to students from industry which do not have the opportunity to take it on campus.

CAD OF LOGIC

Dr. Fredrick J. Hill

Hardware Description Language and Function Level Simulation - Because of the ever increasing complexity of digital systems which can be realized on a single integrated circuit chip, interest in more efficient design and description of digital system continues to increase as well. One such description technique which is also suitable as a medium for function level simulation is the register transfer level language (RTL). An RTL, called AHPL, is introduced in both senior level and graduate level courses at the University of Arizona.

A function level simulator (HPSIM) for the language, AHPL, has been developed at the university. This simulator is used by students as a means of evaluating designs written in AHPL with respect to satisfaction of design objectives. This software has also been distributed to approximately 75 other institutions and electronics companies.

Under development as a research project is a program which will be capable of translating descriptions written in AHPL directly to a data base from which the masks necessary for integrated circuit realization of the described system can be generated. Once development of this program is complete it will be integrated into CAD coursework.

Test Generation for Digital Integrated Circuits - As digital integrated circuits increase in complexity, the problem of efficiently testing these circuits becomes one of ever greater concern. The fundamental concepts of both fault detection testing and fault location in digital systems are taught in a special graduate course at the University of Arizona. Special emphasis is placed on the application of artificial intelligence techniques to the generation of test sequences for digital integrated circuits.

Students have hands on experience with an automatic test generation program called SCIRTSS (sequential circuit test search system). This program which was developed at the university requires, as input, only an AHPL description of the circuit to be tested and values of certain hueristic guidance parameters.

CAD ACTIVITIES - SIMULATION TECHNIQUES

Dr. Olgierd A. Palusinski

Several software simulation tools are presented in the course "CAD TECHNIQUES FOR INTEGRATED CIRCUITS." Students use the programs in the series of small class projects. Each student participating in the course performs also more involved term paper. During the work on term paper students learns in depth about a particular tool and makes its modification or adaptation to new output devices.

The simulation programs presented range from hardware description on instruction and register levels to circuit and device simulation. The students learn about ISPS developed at the Carnegie-Mellon University and AHPL developed at the University of Arizona. Using our software they can generate device placement drawings which can be used as basis for layout. The layout is facilitated by the UAMASK program run in a batch mode on the CYBER 175 computer. This program is based on previous work done at the University of Florida. The hand copies of layouts are generated using raster or CALCOMP plotters. The CALCOMP plotter generates color copies, to help in visualizing different mask layers. Simulation on gate level is based on the use of LOGIC program supplied by the Western Design Center (WDC). Available logic states are low, high and undetermined. Allowed modelling elements are clocks, standard and clocked logic gates, ROMs, RAMs and PLAs.

On the circuit level we use CIRCUIT2 again supplied by WDC and SPICE2.G developed at Berkeley. In simulation we concentrate on circuits containing MOSFET's and we talk about standard models (10μ and larger geometries) and short channel effects.

The device simulation is based on MINIMOS program developed at the Technical University of Vienna. The program simulates MOS devices in 2-dimensions, assuming single rectangular geometries.

ELECTRONIC PACKAGING ENGINEERING

Dr. Douglas J. Hamilton

With the advent of high-speed systems of large complexity, electronic packaging is rapidly becoming an expensive aspect of system design. However, Electronic Packaging Engineering has received little attention in university curricula.

The Electrical Engineering Department of the University of Arizona is initiating a special program in Electronic Packaging Engineering, aimed at industrial users as well as on campus students. Courses being developed will address packaging

problems at all levels from the silicon chip to the complete system, and will include both theoretical and practical considerations. Several technologies, such as printed circuit boards, thick-films, thin-films and integrated electronics will be covered. Thermal, environmental, mechanical, electrical, CAD, and materials aspects will be considered at both the circuit and system levels.

Key elements of the program are course offerings for regular graduate credit; the use of MICROCAMPUS to video tape and deliver the courses; and participation by industrial representatives both in planning courses and giving lectures.

Long-term plans include the development of an M.S. program available to any student with a B.S. degree in engineering or science. This program would include a 3-course sequence on Electronic Packaging Engineering, together with additional courses in related disciplines. We also plan to develop a laboratory facility.

Short-term plans include the development of a 3-unit Electronic Packaging Applications course in the Electrical Engineering Department. This will be available for senior elective or graduate credit, and will be offered beginning in the fall semester 1983. The course is being planned with industrial assistance and lectures will be given by industry personnel. Care is being taken to avoid emphasizing a particular segment of industry or a particular technology.

Students at industrial sites remote from the University of Arizona -- indeed, anywhere in the world -- will be able to obtain regular graduate credit for this and other courses by taking them through the MICROCAMPUS program. MICROCAMPUS, a part of the Division of Media and Instructional Services, has been in operation for 10 years. It provides two "Candid Classroom/Studios" in which courses can be video taped or transmitted live on the Interactive Education Television System (IETS). MICROCAMPUS also provides all necessary equipment, personnel and coordination for video-production; video playback carrels for on campus use; and marketing and distribution service for delivering courses to users.

MANUFACTURING SYSTEMS ENGINEERING FOR MICROELECTRONICS

Dr. John S. Ramberg

From beginnings as the University Numerical Analysis Laboratory, through establishment in 1961 by A. Wayne Wymore as the nation's first Department of Systems Engineering, and including the 1972 addition of a modern, non-traditional, industrial engineering curriculum, the Department of Systems and Industrial Engineering has consistently emphasized and taught the interdisciplinary design of large-scale systems involving people, machines and software. Curricula stress the integrated application of the information technologies of computing, optimization, decision and control which are the necessary keys to exploiting advanced physical technologies for manufacturing.

The industrial engineering program was created in response to the growth of manufacturing in Arizona. Over the last two years, the Department has increased its long-term commitment to system design for manufacturing by hiring four new faculty holding doctorates in industrial engineering, and by developing an undergraduate industrial engineering program with an option in manufacturing systems engineering.

The roles of the modern manufacturing systems engineer are to design, install, implement, improve and manage computer integrated manufacturing systems. Such roles require specialized knowledge of systems and industrial engineering, as defined at the University of Arizona, with an interdisciplinary background in other engineering,

management and computing fields.

The Department of Systems and Industrial Engineering view the boundary of the manufacturing systems engineering program as beginning with order entry and ending with product shipment and consumer services. In particular, the aspects of manufacturing systems engineering with special reference to high technology fields that are emphasized are:

- general concept and design of computer integrated manufacturing systems through system design methodologies for manufacturing,
- optimization of manufacturing systems and optimal decision making in manufacturing,
- reliability, quality assurance, and testing for manufacturing systems,
- information systems design and management in manufacturing, and
- manufacturing process designs for high technology fields.

These aspects of the curriculum are intended to provide industry with highly trained graduates with a balanced view of theory and practice. The challenge will be the integration of these areas through laboratory projects and industrial experiences. The department is working closely with manufacturers, through an Industrial Advisory Committee to create a manufacturing systems curriculum responsive to the needs of industry.