Annual Report for Contract No. 83-01-012

BIPOLAR TRANSISTOR STRUCTURES and SPACE-CHARGE-LIMITED LOADS for VLSI APPLICATIONS

Prepared for

Semiconductor Research Corporation
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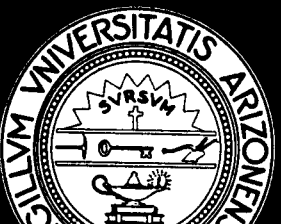

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ABSTRACT

The research goal was to investigate new high speed VLSI bipolar integrated structures using simple processing similar to MOS technology.

A novel concept for transistor fabrication was invented, introducing an idea for protection against deep saturation. It involves the use of a Static Induction Transistor or a PNP substrate transistor and was developed based on transistors designed for a triple or quadruple diffusion fabrication technique. Simulation showed improved switching times when compared to similar gates without protection, while the charge-storage was practically eliminated. Simple gates protected by SIT or PNP operate with the speed of ECL gates but with smaller power consumption. Punch-through space-charge-limited loads have been investigated and fabricated. Resistances in the range of 10 - 100 kohms on the area limited primarily by the contacts were obtained.

A GEneral one-dimensional semiconductor device performance SIMulation program (GESIM1) for the static and dynamic analysis has been developed. As the input data, the impurity concentration distribution and applied terminal voltages are required only. Also, a device and processing oriented BIpolar TRAnsistor Simulator program (BITRAS) has been developed. The program combines technological and electrical parameters of the device.

Develpment and modification of our local oxidation techniques has been completed. Parameters necessary to realize a self-aligning isoplanar process with 2.5 μm geometry have been established. The development of thin base bipolar transistors is in progress.

Future research plans are focused on device fabrication and the

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INTRODUCTION.

Bipolar integrated circuits will retain their superiority for high speed applications as dimensions are scaled down but require relatively complicated processing, including thin epitaxial layers and buried subcollectors. As a result of process complexity, VLSI high speed bipolar integrated circuits are more costly than MOS structures.

The research goal of this project was to investigate new high speed VLSI bipolar integrated structures using simple processing similar to MOS technology. Emphasis was put on simulation in order to theoretically verify the proposed ideas. Technological efforts were concentrated on development/modification of processing sequences as preliminary steps towards fabrication of the designed structures.

The accomplishments of the contract can be summed up as follows:

I. Device design and simulation.

1. A novel concept for bipolar transistor fabrication was invented, introducing an idea for protection against deep saturation, thus the name Saturation Protected bipolar Transistor (SPT). It involves the use of a Static Induction Transistor or a PNP substrate transistor as a clamp. Simulation showed improved switching times when compared to similar gates without protection because the charge-storage was practically eliminated. The protection methods use triple or quadruple diffusion fabrication techniques; by avoiding gold doping it is possible to fabricate both digital and analog circuits on the same chip. The simulated propagation delay times are comparable to ECL performance. However, ECL gates consume larger amounts of power than the saturation protected gates. SPT/SIT and SPT/PNP are discussed in chapter 1 of this

annual report.

2. Punch-through space-charge-limited loads as a replacement for diffused resistors have been investigated. The range of resistance values is large. The small dimensions lead to small capacitances and fast switching times. The topic is covered in chapter 2.

3. A GEneral one-dimensional semiconductor device performance SIMulation program (GESIM1), with no simplifying assumptions, has been developed for static and dynamic analysis. The only input data required is the impurity concentration distribution and applied terminal voltages. Also, a device and processing oriented BIpolar TRAnsistor Simulator program (BITRAS) has been developed. The program combines the technological and electrical parameters of the device. Both programs are discussed in chapter 3.

II. Technology/process development.

1. Development and modification of our local oxidation techniques has been successfully completed. The parameters necessary to realize a self-aligning isoplanar process with 2.5 μm geometry were established.

2. The development of thin base bipolar transistors is in progress. Experimental data including the surface concentration and diffusion lengths have been collected and appropriate concentration profiles have been established. Further progress in overcoming existing problems (low beta and punch-through of emitter-base junctions) is conditioned upon development of polysilicon emitter structures or replacing the phosphorus emitter diffusion with arsenic. The first approach of developing polysilicon emitters is given priority.

3. Punch-through space-charge-limited loads have been fabricated and

tested. Resistances in the range of 10 - 100 kohms on the area limited primarily by the contacts were obtained. All technological issues are discussed in chapter 4.

III. Future research plans.

Future research plans include continued development of CAD tools, the fabrication of quadruple diffused structures for a new family of high speed, low power, bipolar logic gate arrays with space-charge-limited loads.

PART I - DEVICE DESIGN AND SIMULATION

1. SATURATION PROTECTED BIPOLAR TRANSISTORS

1.1 Introduction

Integrated circuits such as Emitter Coupled Logic (ECL) using bipolar devices will retain their superiority for high speed applications as dimensions are scaled down [1.1, 1.2]. Such circuits require relatively complicated processing including thin epitaxial layers and buried n^+ layers. Some less complex high speed bipolar IC processes have been developed [1.3, 1.4]. Schottky Transistor Logic (STL) [1.4] provides improved speed by reducing carrier storage effects. It provides better performance than the gold doping technique previously used, but requires both low- and high-barrier Schottky diodes. Integrated Schottky Logic (ISL) [1.4] uses a PNP transistor as the NPN clamping device. Its performance is very similar to that provided by STL processing.

For saturating logic gate arrays, a novel concept for transistor fabrication is discussed in this report. The basic idea is to protect against deep saturation by using a Static Induction Transistor [1.5] or a PNP substrate transistor as a clamp. The function of the saturation protection is to prevent the switching transistor from entering into a deep saturation mode by limiting the charge stored in the collector. This will eliminate the collector minority carrier storage effect and result in faster switching speeds.

1.2 SIT Protected Bipolar Transistor

1.2.1 Operating principles

The operating principles of the SIT Saturation Protected bipolar Transistor (SPT/SIT) is best understood by considering the operation of a series of devices. Figure 1.1 shows the cross section of a lateral collector device. The spacing between the base and the collector of this device can be made quite small using a simple double diffusion process. A positive bias applied to the collector creates a depletion region which reaches the base region of the transistor as shown by the dashed line. A very high electric field exists between the "internal" collector and the lateral one after the depletion region is established. Carriers are swept at velocities close to saturation velocities through the depletion region, and high speed performance results.

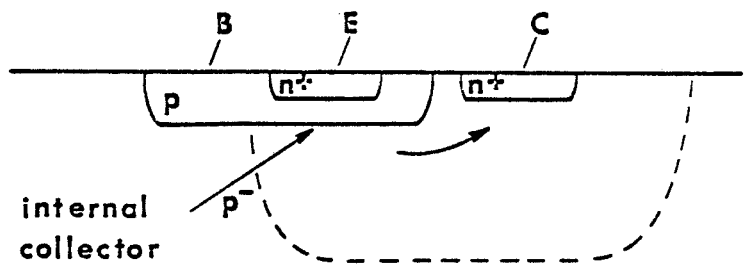


Fig. 1.1 A simplified bipolar structure for VLSI.

There are two disadvantages of such a structure. First, threshold collector voltage is required to deplete the collector region. Second, the base is shorted to the p^- substrate. The latter problem can be easily overcome by surrounding the base with an n-region as shown in Figure 1.2(a). The base is then completely isolated from the substrate by a depleted region as shown by the dashed line. The device will not operate properly if the

collector voltage is too low because the depletion region is not formed properly. To prevent such improper operation, the substrate should be connected to a negative potential, thereby creating a permanent depletion region. In this structure, in addition to the basic bipolar NPN transistor and Lateral Punch-Through Transistor (LPTT) [1.6], a p-channel Static Induction Transistor [1.5] between the base and the substrate can be also identified. The equivalent lumped model is shown in Figure 1.2(b). The p-type base of the NPN transistor is the source of SIT, the n-type collector region is the gate of SIT, and the negatively biased substrate is the drain of SIT. For large positive collector (gate of the SIT) voltages, the SIT transistor is off. If the base current of the NPN transistor is increased as in a logic circuit, the collector voltage decreases. As this happens, the SIT transistor will start to conduct, thereby clamping the NPN collector voltage out of saturation by directing the excess NPN transistor base current to the substrate. The current flow between the NPN base and the substrate is determined by the potential distribution in the depletion region under the base. The potential barrier in the SIT transistor, which is a function of drain and gate voltages, is lower than in bipolar transistors for the same gate (base) voltage. This was proven experimentally based on the results of temperature measurements [1.7]. The two barriers are in parallel. Because of the lower SIT barrier, the current will start to flow in the SIT before minority carrier injection occurs in the collector PN junction. The resulting clamping voltage is a function of the substrate voltage. A large negative substrate voltage will result in virtually no minority carrier storage in the collector region. As the negative substrate voltage is increased toward zero, the minority carriers storaged in the collector region increase because of the increase of the barrier potential in the SIT transistor.

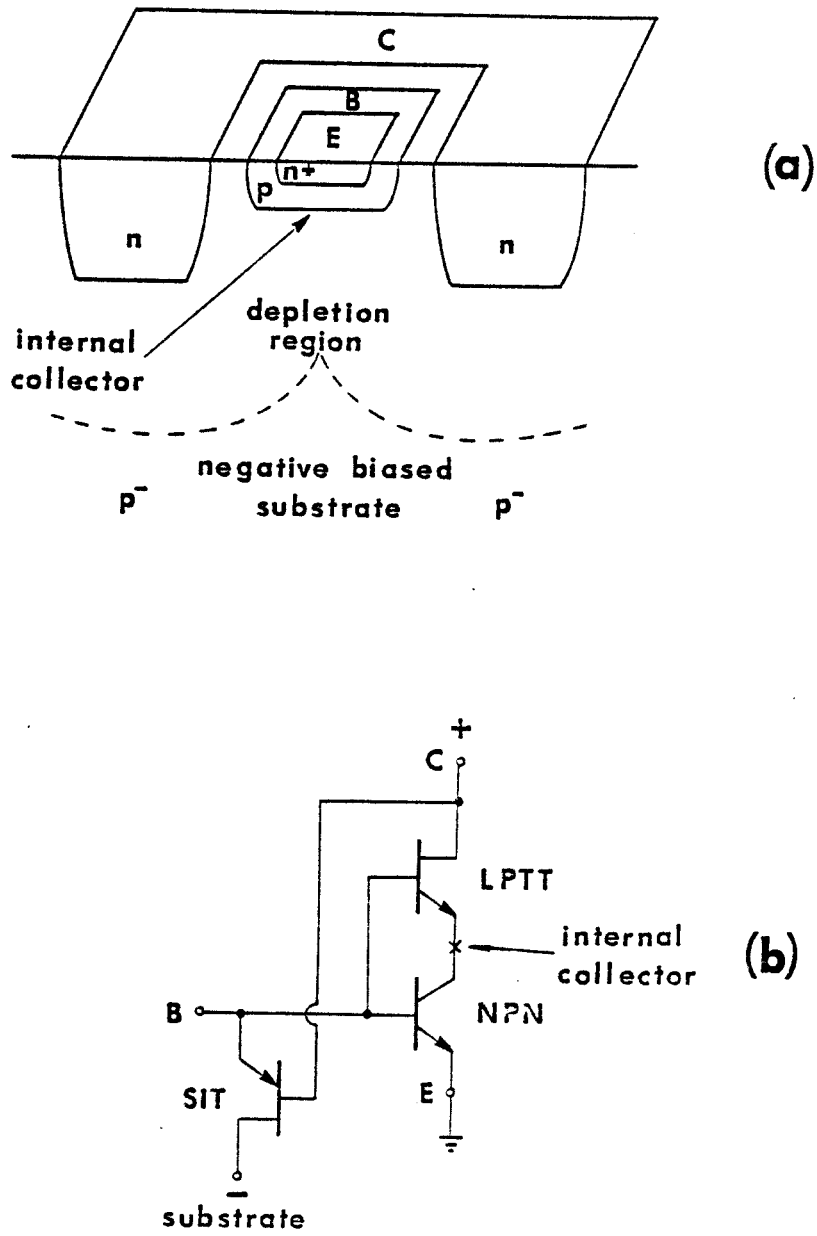


Fig. 1.2 A modified bipolar structure for VLSI, (a), and its equivalent circuit, (b).

1.2.2 Circuit simulation

A lumped transistor model is not adequate for modeling the device structure presented in Figure 1.2(a). This is due to interactions between carriers of LPTT and SIT, with the mechanism being quite complex. This device requires advanced two-dimensional numerical simulation models in order to obtain reliable results. Such simulations are not available as yet. However, in the structure shown in Figure 1.3(a), the SIT and NPN transistors are not merged. There is no direct interaction between the carriers of both transistors. Therefore, the lumped model shown in Figure 1.3(b) can be adequate for simulation of such devices. Also, the voltage drop on the space-charge of LPTT is usually much larger than the voltage drop on the semiconductor material, where the charge neutrality holds. The widely used SPICE2 circuit simulation program [1.8] was applied to the model of Figure 1.3(b). A model for the SIT transistor was developed based on formulas given below [1.5]:

$$I_d = I_s \left[\exp\left(\psi_o / V_T\right) - 1\right] \tag{1.1}$$

where: I_d is the device current, I_s is the saturation current, ψ_o is the potential barrier height and V_T is the electrostatic potential.

Equation (1.1) is valid both for an SIT transiator as well as a bipolar transistor. I_s and ψ_o are given by formulas [1.9, 1.10, 1.11] (with all subscripts referring to the four-layer bipolar transistor model):

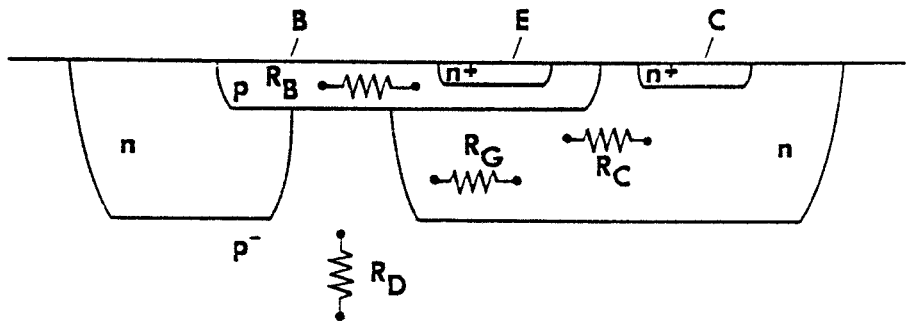
-for a p-channel SIT transistor:

$$I_s = q\, D\, N\, \frac{A_{SIT}}{B\, W_{eff}} \qquad \psi_o = -\eta\left(V_C - \frac{1}{\mu} V_S\right) + V_Q \tag{1.2}$$

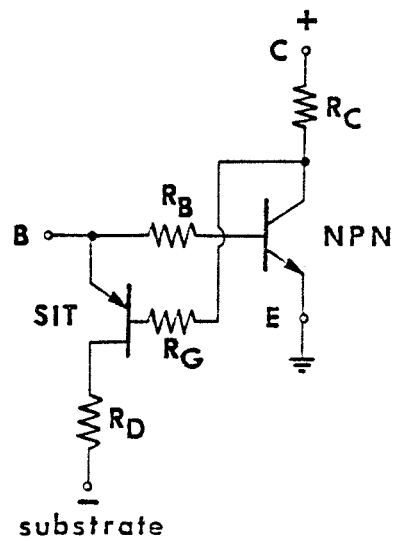
-for a p-n-p substrate bipolar transistor:

$$I_s = q\,D_C\,N_B\,\frac{A_{pnp}}{\int N_B\,dx/N_B} \qquad \psi_o = V_T + V_{CB}\ln(N_B N_C/n_i^2) \tag{1.3}$$

where: q - electron charge, D - carrier diffusivity, N - doping concentration, A - area, W_{eff} - effective width of the potential barrier, η - gate efficiency (0.1 - 0.4), V - voltage, μ - amplification factor, V_Q - voltage drop on the space-charge, n_i - intrinsic concentration.



(a)



(b)

Fig. 1.3 A triple diffused bipolar transistor structure with SIT protection, (a), and its equivalent circuit, (b).

The amplification factor μ depends on the geometry of the device and can be calculated using empirical relations given in [1.11]:

$$\mu = 2.5 \exp(\pi D/2\ Z) - 1 \qquad (1.4)$$

where: D and Z are the depth and the spacing between the lateral collectors respectively. Examplary value of $\mu = 5.4$ for $D = 3\ \mu m$ and $Z = 5\ \mu m$.

The model of the SIT protected bipolar transistor for SPICE2 simulation uses the diode model and controlled sources available in the program, and the effect of charge storage in the region between the source and the top of the potential barrier is included in the "diffusion" capacitances. Parameters for the SIT nonlinear transistor model and the resulting protected bipolar transistor were calculated from the device lumped model as shown in Figure 1.3(b).

A simple circuit with the SIT Saturation Protected bipolar Transistor (SPT/SIT) was simulated. Encouraging switching times, when compared to similar gates without protection, were obtained. Figure 1.4 shows the output waveforms for an unloaded inverter to which a 20 nsec input pulse was applied, and Figure 1.5 presents results for a chain of such inverters subject to the same input pulse. It has been found that the output voltage swing and the delay time of such a structure are sensitive to substrate biasing. For zero substrate biasing, the storage time of a single unloaded inverter was 8 nsec. With the biasing of -3 V, it was practically eliminated with slopes of the waveforms due exclusively to parasitic capacitances resulting in switching times of 1.2 nsec. The delay between the waveforms labeled 1 and 3 of the loaded inverter was 1 nsec for the same negative substrate biasing; thus, the propagation delay time per gate was 0.7 nsec, while the power delay product was less than 1 pJ. The voltage swing for the same case was only 200 mV, while the actual voltage swing on

the internal collector was larger and equal to 470 mV. These results were obtained for a non-optimized structure, utilizing no Schottky clamp diodes or gold doping, and for a very simple process with no epitaxial and buried layers and structures designed using 4 μm geometry. With smaller geometry, even better results are expected to be achieved.

In conclusion, simulation showed encouraging switching times for the SPT/SIT gates when compared to similar gated without protection, while the charge-storage was practically eliminated. The SIT protection transistor is, in fact, a substrate transistor placed under the base contact and does not require extra space. However, the structure is sensitive to substrate biasing which effects also the voltage swing and the delay time.

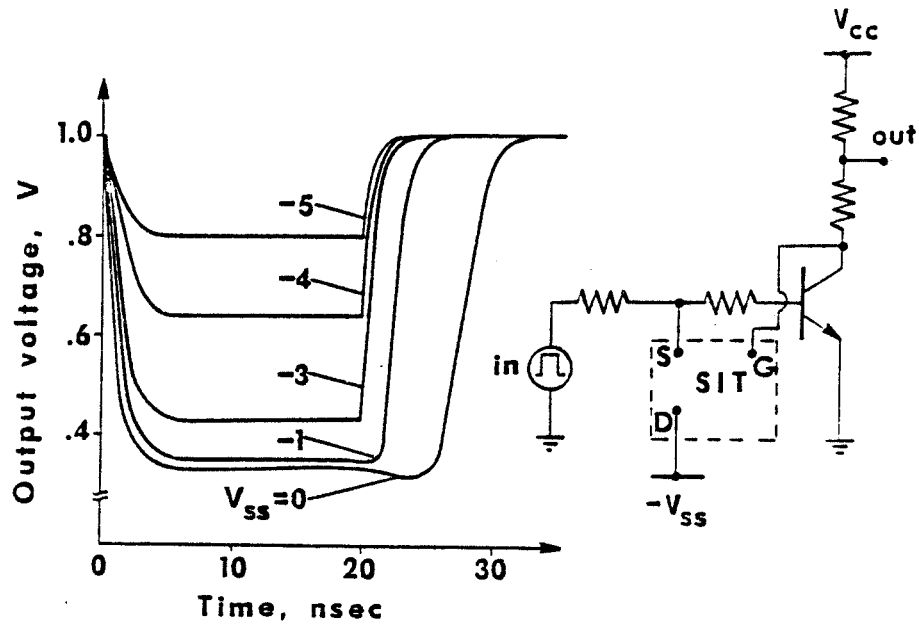


Fig. 1.4 Output waveforms for a single stage unloaded inverter with an SIT protected bipolar transistor.

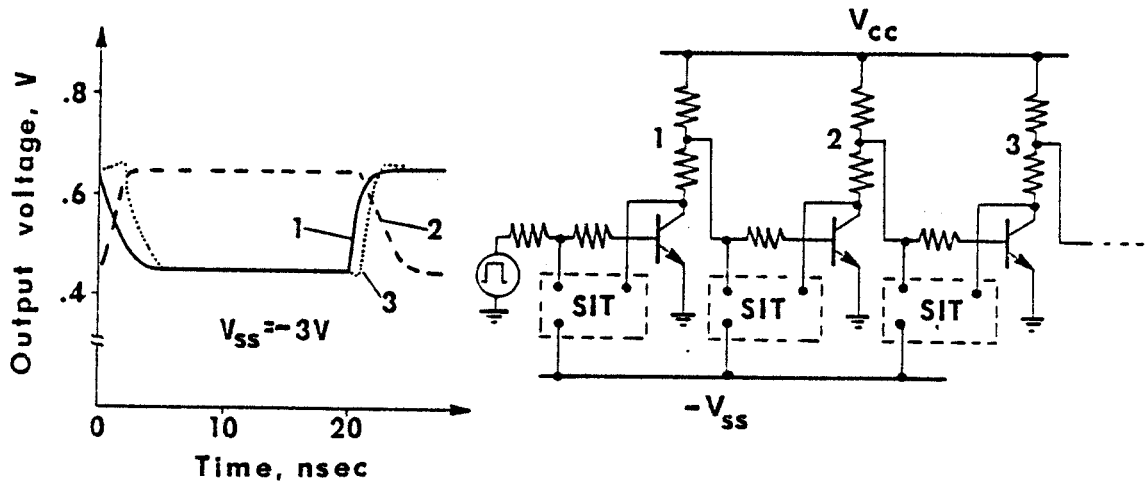


Fig. 1.5 Output waveforms for a chain of inverters with SIT protected bipolar transistors.

1.3 PNP Protected Bipolar Transistor

1.3.1 Operating principles

In searching for an alternative approach to SIT protection, the idea of a PNP protection transistor emerged. By introducing a thin n-type layer into the channel of the SIT, a PNP protection transistor can be fabricated. The excess NPN base current drive can be diverted to the substrate, thereby avoiding deep saturation. If properly designed, the collector minority carrier storage in the NPN will be minimized. This happens if the base of the PNP transistor is thin enough with a small value of the "Gummel number". Once the carriers reach the substrate, no storage effect is possible.

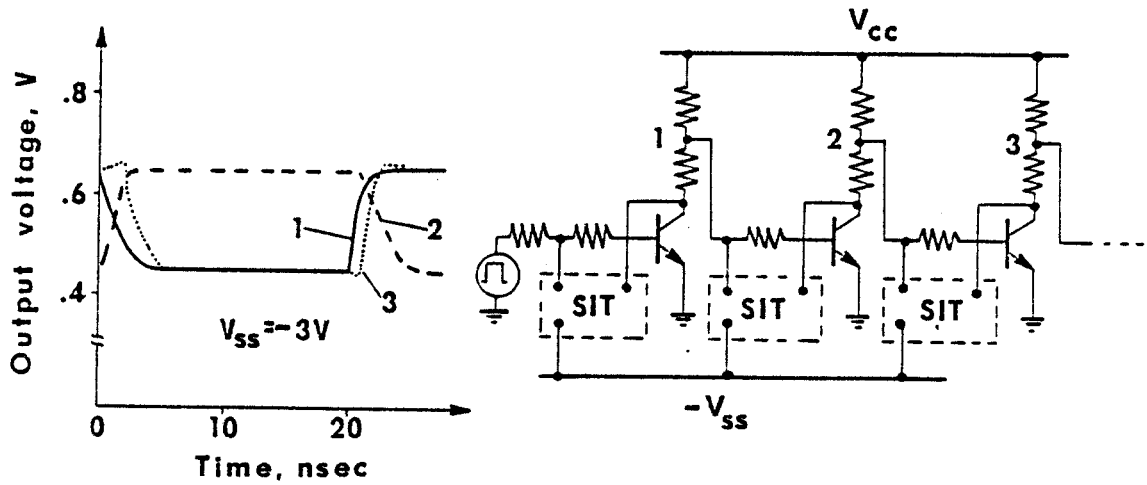


Fig. 1.5 Output waveforms for a chain of inverters with SIT protected bipolar transistors.

1.3 PNP Protected Bipolar Transistor

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Figure 1.6 shows cross-sections of two realizations of the PNP protected bipolar devices fabricated using a quadruple diffusion technique. Structure (a) is a variation of the SIT design, while structure (b) is a modified arrangement with no deep diffusion under the base on the left side resulting in smaller parasitic capacitances. The existing base series resistance R'_B of the NPN transistor can be very beneficial. If a large base current flows, there will be a voltage drop across the base region due to R'_B. Thus, the emitter-base junction of the PNP transistor will be more forward biased than the collector-base junction of the NPN transistor. Because of this series resistance effect, the PNP transistor will clamp the NPN transistor out of deep saturation. The clamping action does not rely on the base resistance effect. It will function as desired so long as proper fabrication procedures are used.

1.3.2 Circuit simulation.

The structure is simple to simulate, since the NPN switching and the PNP protection transistors can be separated and implemented in the SPICE2 simulation program. A lumped transistor model is shown in Figure 1.6(c).

Simple inverting gates with the PNP protection transistors were simulated. The effect of substrate biasing dependence was essentially eliminated. The PNP protection transistor can efficiently operate even with zero biasing. PNP protection is somewhat inferior to SIT protection as far as delay time is concerned, but it may find much wider applications (e.g. TTL gates). The voltage swing of the PNP clamp is larger. Some results for a single and multiple-stage gates are presented in Figures 1.7 and 1.8. The delay time was 2 nsec per gate and the delay power product was kept below 1.5 pJ.

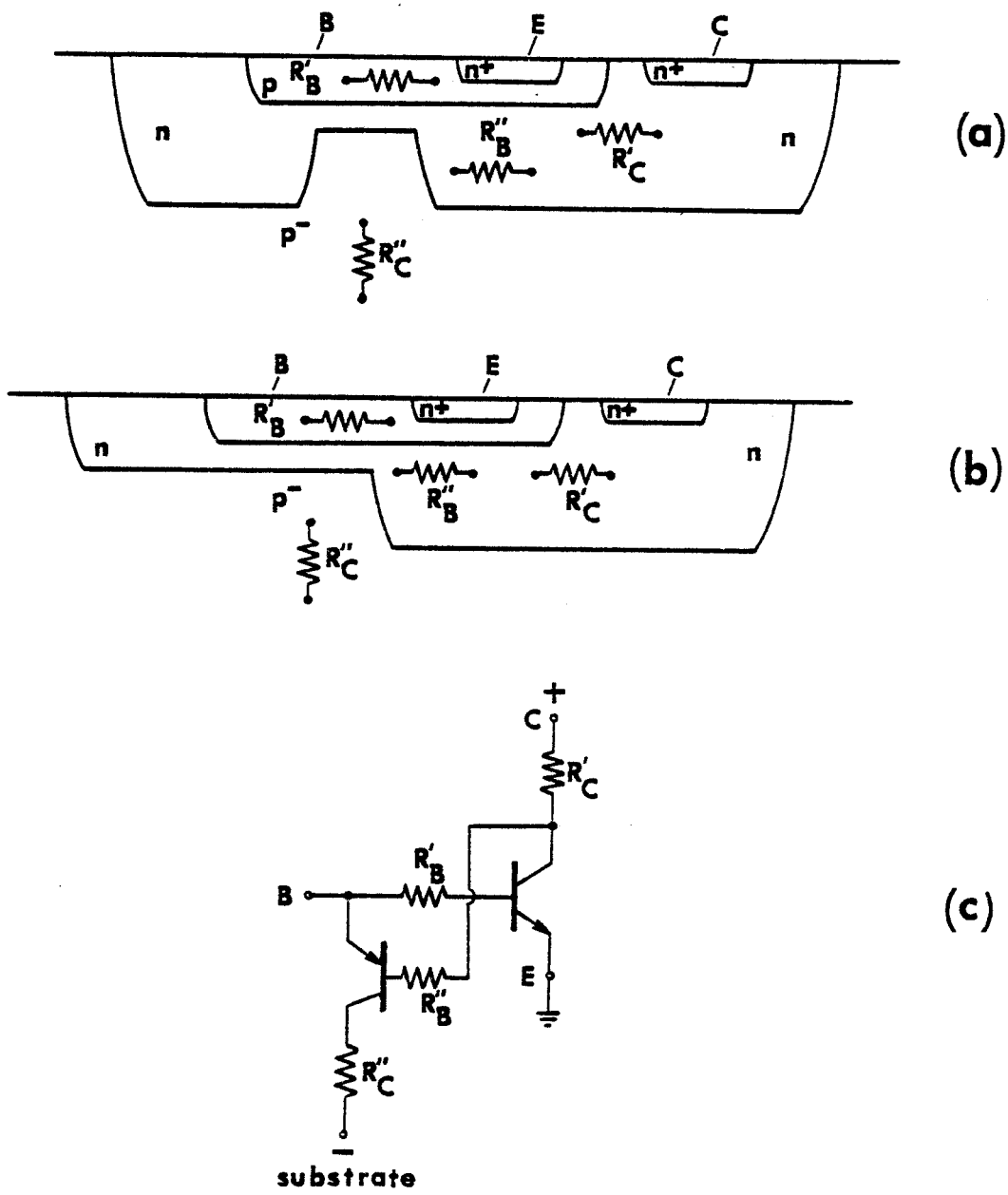


Fig. 1.6 Two realizations of PNP protected bipolar transistors, (a), and, (b), and the equivalent circuit, (c).

In order to increase the output voltage swing, the structure was modified to use two existing internal collector series resistances (Figure 1.9). With this double collector structure, the collector C1 can be connected directly to the positive bias voltage, while the second collector C2 will sense the voltage at the internal collector. Current flow towards the collector C2 is very small, so the voltage drop across this resistance is negligible and the potential on C2 follows the potential at the internal collector. Thus, the internal collector series resistances are beneficial as is the base series resistance of the PNP protection transistor, which was previously discussed.

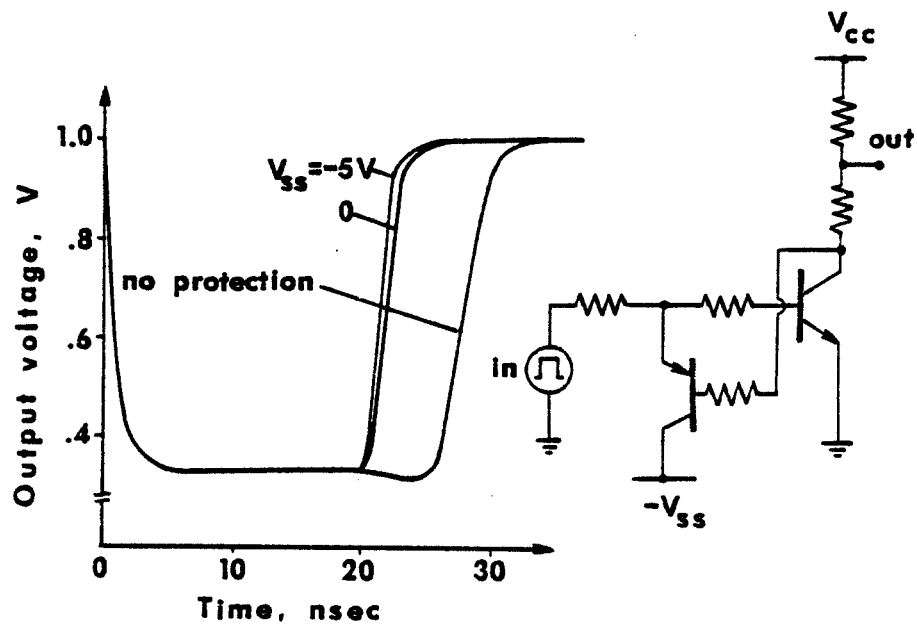


Fig. 1.7 Output waveforms for a single-stage unloaded inverter with a PNP protected bipolar transistor.

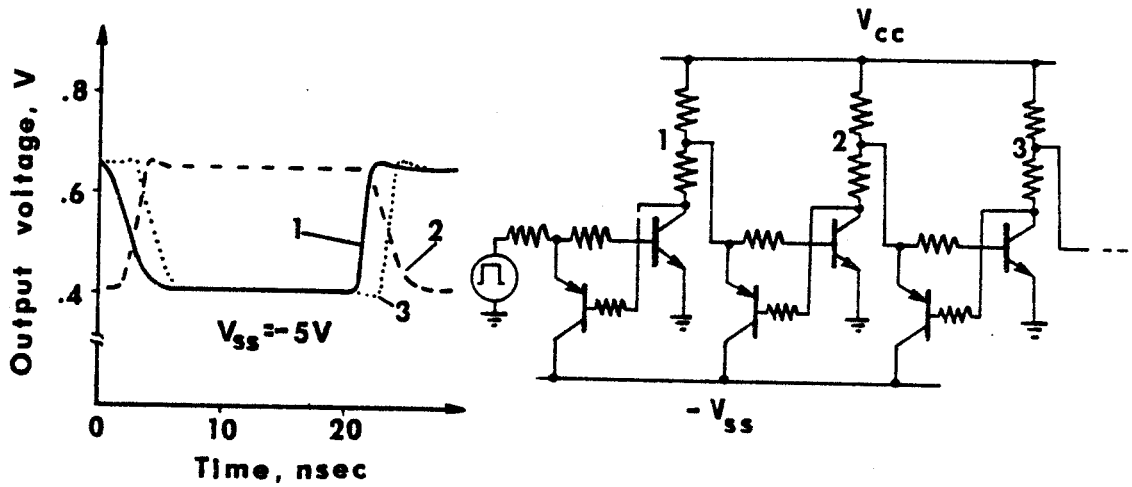


Fig. 1.8 Output waveforms for a chain of inversters with PNP protected bipolar transistors.

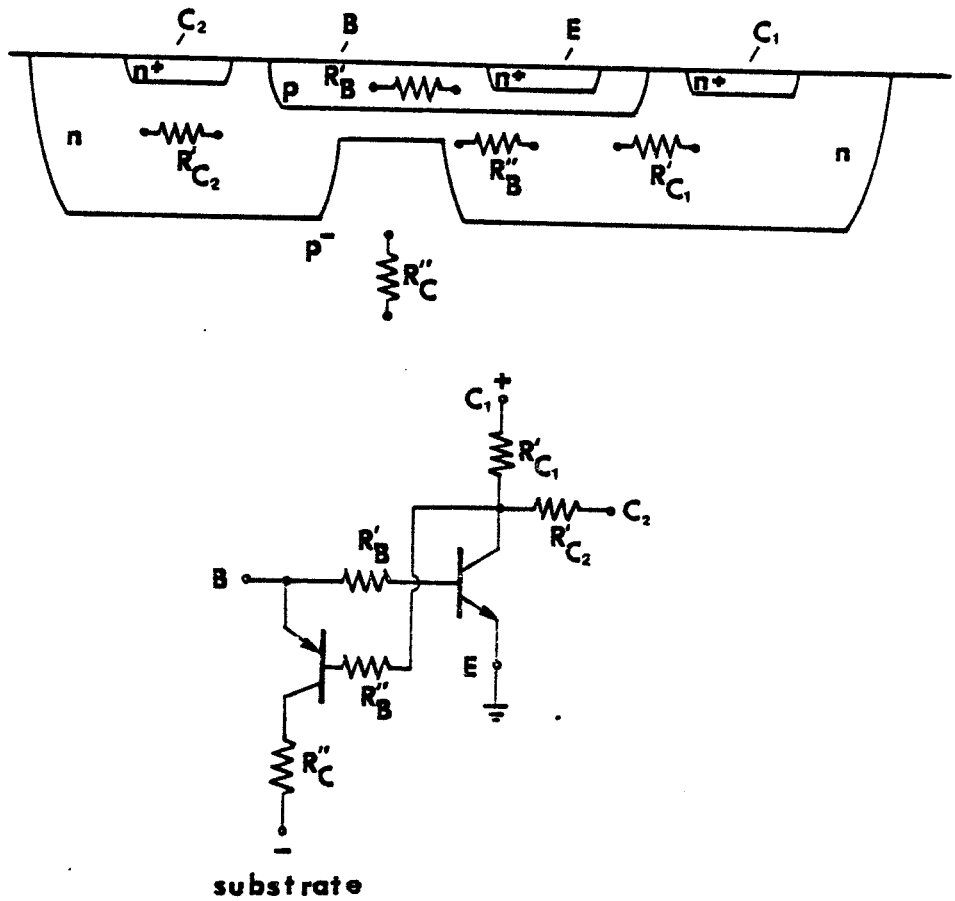


Fig. 1.9 A quadruple diffused P-N-P protected bipolar transistor structure with two collectors.

The idea of PNP protection transistors was next expanded to other logic gates. Interesting results were obtained for TTL gates. Simulation has been performed for standard TTL [1.12] gates with and without protection. In order to maintain reasonable values of resistances, in addition to small values of parasitic capacitances, transistors were individually designed. In all designs, except for the input multi-emitter transistor, pnp protection transistors were used. Investigations were focused on establishing model parameters and evaluation of the effect of substrate biasing, saturation current, beta, substrate concentration etc. TTL logic gates without protection, which were designed with wafers having high lifetimes (no gold doping), had delay times of the order of 25-30 nsec per gate. Using the pnp transistor protection, a significant reduction in the delay time (to about 4 nsec per gate) was observed. These results are for a non-optimized structure, utilizing no Schottky clamp diodes or gold doping. The devices can be fabricated with a very simple process without epitaxial layers. This performance compares very favorably with state-of-the-art TTL, and quadruple diffussed TTL gates require only 25% of the area of Schottky TTL. It is believed that with optimization, bipolar protected TTL logic is capable of outperforming other TTL structures.

Output waveforms of a single TTL gate with a standard load are shown in Figure 1.10. In addition to devices designed for 4 μm geometry, computations were made for devices designed for 2.5 μm geometry and, as expected, even better results were obtained. It is worth stressing that when using the triple/quadruple diffusion technique and avoiding gold doping, it is possible to fabricate both digital and analog circuits on the same chip. This can be an advantage in some cases.

A comparison of the performance of the SIT or PNP protected bipolar transistor gates with the fastest known logic gate - ECL [1.12] (also designed for the triple/quadruple diffusion fabrication) was performed. ECL gates are non-saturating logic gates and, therefore, do not require protection transistors. Figure 1.11 presents the results of the comparison. The output waveforms of unloded ECL and single-stage inverters with SIT/PNP protected transistors are presented. Comparable propagation delay times are observed. The ECL gates consume more power than the SIT Saturation Protected Transistor Logic gates (SPTL/SIT) or the PNP Saturation Protected Transistor Logic gates (SPTL/PNP).

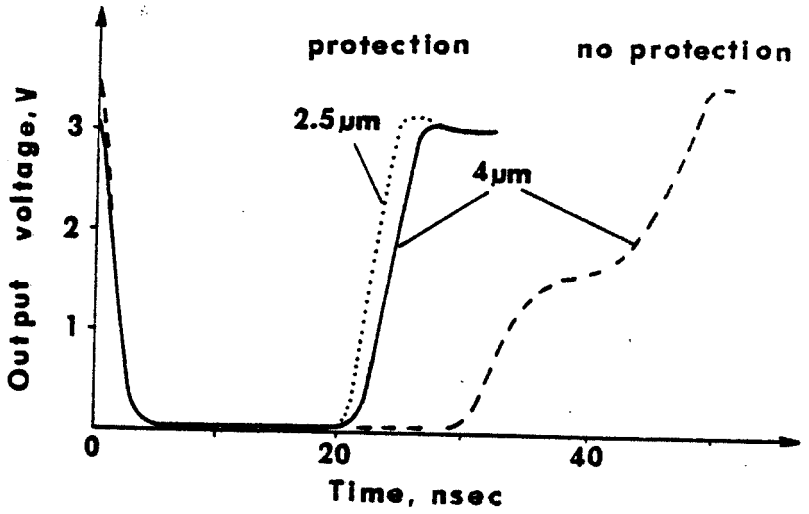


Fig. 1.10 Output waveforms for a single TTL gate.

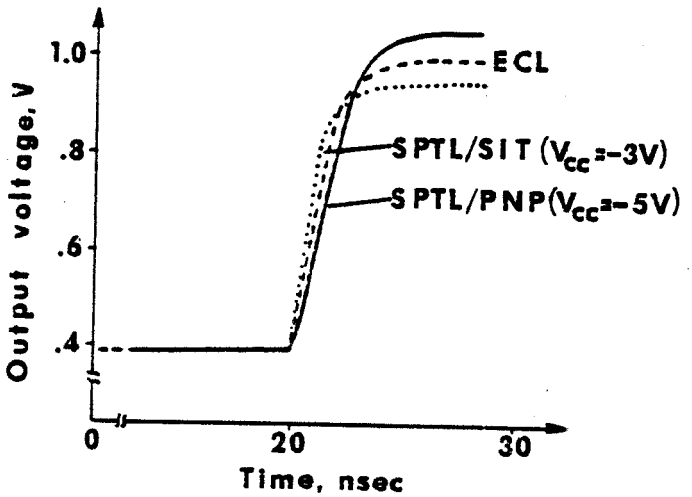


Fig. 1.11 Comparison of output waveforms of ECL and SIT/PNP protected transistor inverters.

2. PUNCH-THROUGH SPACE-CHARGE-LIMITED LOADS

2.1 Introduction

The performance of bipolar and MOS silicon devices is approaching limits imposed by device physics and dimensions. The physics imposed limits often relate to carrier diffusion phenomena limited transit times. The dimension imposed limits often relate to storage and depletion capacitances. Shrinking the device size and lowering power of a single stage usually lead to lower currents and the necessity of employing larger values of resistors. At the same time, the values of the sheet resistance and unit capacitance basically remain unchanged. This has caused device researchers to investigate devices based on different operating principles.

This part of the annual report discusses a device which operates in a punch-through condition with space-charge control of currents. The punch through condition in bipolar devices was identified some time ago as an undesirable condition to be avoided. It caused loss of control and gain in standard bipolar devices. Also, in the case of MOS devices, punch-through is considered as an undesirable effect. In order to avoid punch-through in small devices, a much higher impurity concentration than usual is required. This problem is especially important for micrometer and submicrometer geometries. Increasing impurity concentrations causes large parasitic capacitances and, therefore, lower device speed.

2.1 Operating principles

The theory for Space-Charge-Limited (SCL) current was given first by Mott and Gurney [2.1]. The SCL mechanism was reported in Shockley's Analog Transistor [2.2] and Teszner's Short Channel FET [2.3], Richman's MOS Transistor [2.4], Nishizawa's SIT Transistor [2.5] and Ohmi's Punch-Through

Transistor [2.6]. A lateral version of the Punch-Through Transistor was also published [2.7]. In the SIT transistor, the effect of series resistance seems to dominate [2.8]. A detailed theory of SCL for various devices is given in [2.9, 2.10].

Fig. 2.1 shows the cross section structure of an $N^+P^-N^+$ punch-through diode which can also be made as a $P^+N^-P^+$ structure. Positive voltage is applied to the anode A. With an increase of the voltage, the thickness of the depletion layer increases. When the depletion layer reaches the N^+ or cathode C region, current starts to flow. At the same time, injected electrons in the depletion region will create an internal space-charge which affects the potential distribution. This will control the current flow as the voltage is increased. The value of the threshold voltage can be controlled by geometry and substrate resistivity.

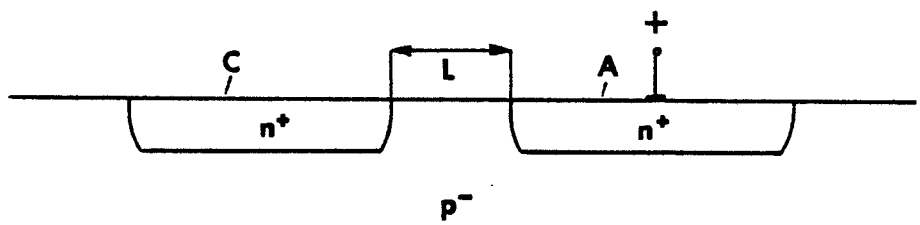


Fig. 2.1 A punch-through space-charge-limited (PTSCL) structure.

Once the punch-through is reached and voltage is increased, the diode performance can be predicted for two conditions, large and small electric fields. Both approximations are presented followed by computer simulated results.

The threshold punch-through voltage V_{pt} is given by:

$$V_{pt} = 7.5 * 10^{-16} * N * L^{2} \qquad (2.1)$$

where: N is the substrate doping in atoms/cm**3 and L is the channel length in microns.

For small electric fields, the diode current I is related to its voltage V as shown:

$$I = \frac{9}{8} \mu \epsilon \epsilon_o \frac{A}{L^3} V^2 \qquad (2.2)$$

where: μ is the carrier mobility, $\epsilon \epsilon_o$ - the permittivity, A - the area and L - the channel length.

For this condition, the dynamic resistance, R, is given by:

$$R = \frac{dV}{dI} = \frac{4}{9 u \epsilon \epsilon_o} \frac{L^3}{A} \frac{1}{V} = \frac{V}{2I} \qquad (2.3)$$

The carrier transit time, τ , and the carrier transit time at the threshold voltage, τ_t , are:

$$\tau = R C = \frac{4}{9} \frac{L^2}{\mu} \frac{1}{V} \qquad \tau_t = \frac{4}{3} \frac{L^2}{\mu} \frac{1}{V} \qquad (2.4)$$

Under conditions of high electric field, the carrier velocity is the saturation velocity v_s and the relationships become quite simple as shown below:

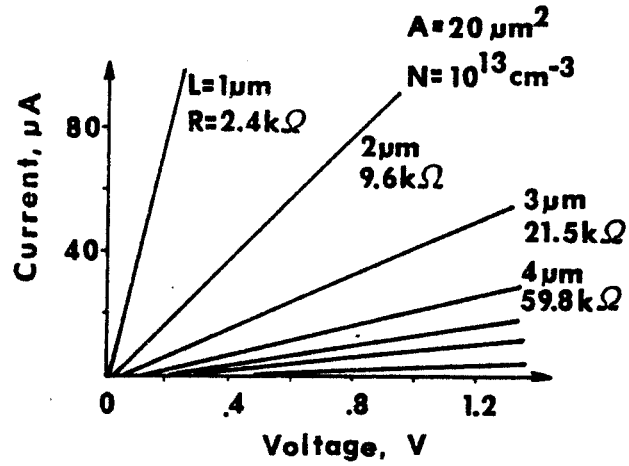
$$I = 2 v_s \epsilon \epsilon_o \frac{A}{L^2} V \tag{2.5}$$

$$R = \frac{1}{2 v_s \epsilon \epsilon_o} \frac{L^2}{A} \tag{2.6}$$

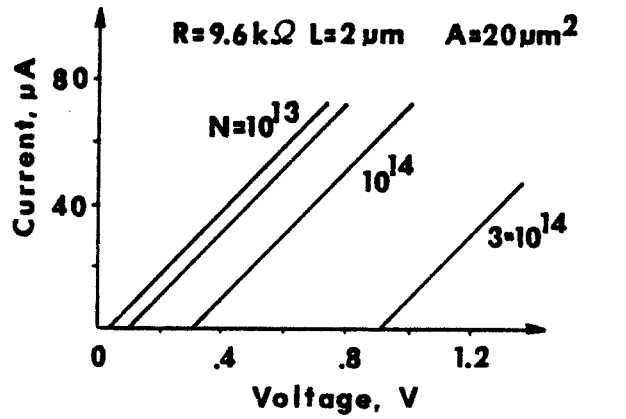
$$\tau = \frac{L}{2 v_s} \qquad \tau_t = \frac{L}{v_s} \tag{2.7}$$

Using the high electric field approximation which is reasonable for small dimensions, the relationship between I and V can be calculated as a function of doping for a 2 micron channel length and a 20 square micron area as shown in Figure 2.2(a). Figure 2.2(b) shows I vs. V for different channel lengths. Note that some small voltage is required to reach the punch-through condition. Exceeding that voltage, the device appears to be pure resistance. Equation (2.6) shows that R is a function of geometry only and, therefore, independently controllable.

This punch-through diode should have applications as a replacement for diffused resistors. Such resistors take considerable space to attain large values. Even polysilicon resistors have difficulties associated with them. These diodes can provide very small area resistors based on the space-charge limiting action of the device. Thus, they could also be called space-charge-limited loads. The range of resistance values is large as shown in Figure 2.2(b). The small dimensions result in small capacitances and fast switching times.



(a)



(b)

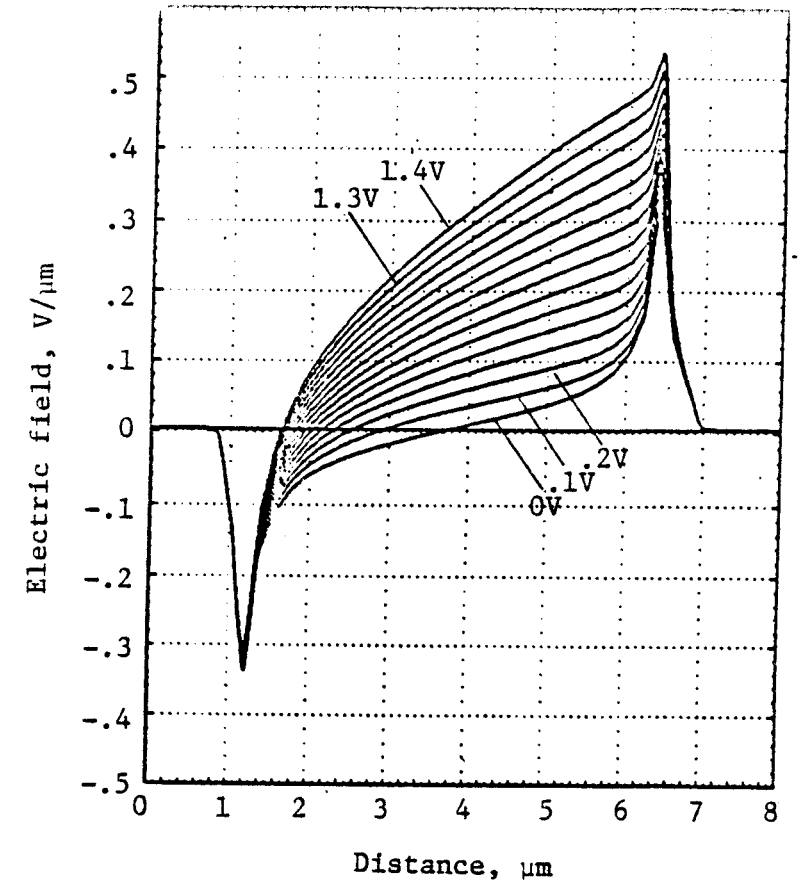
Fig. 2.2 Calculated I-V characteristics of PTSCL loads for various spacing between cathode and anode, (a), and for various substrate doping, (b).

2.3 Device simulation.

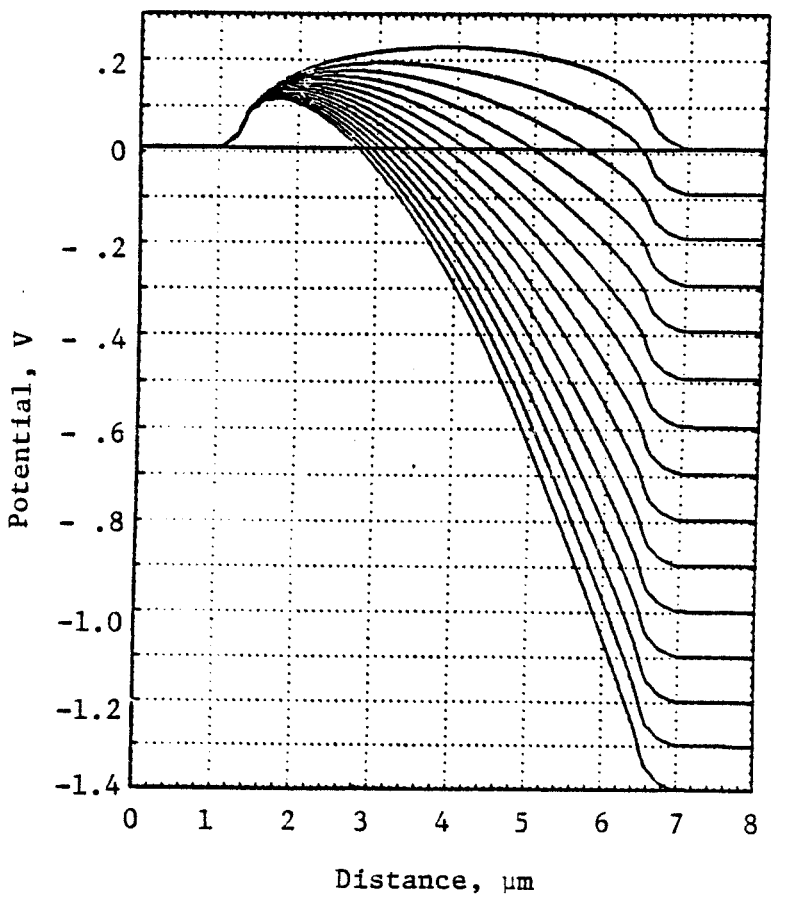
Punch-through space-charge limited loads were simulated using the general one-dimensional device performance simulation program GESIM1. It was developed as part of this research and is described in chapter 3 of this report.

Figures 2.3(a) through (f) resulted from the simulation and show the predicted static variations of electric field, potential, space charge, majority and minority carriers, and hole current for a relatively long (6 micron) $P^+N^-P^+$ diode as a function of distance along the channel for different bias voltages. It can be seen that a space-charge generated potential barrier exists very close to the cathode region. On the left side of the potential barrier, the electrical field is negative and is positive on the anode side of the barrier. A relatively large electric field condition exists in most of the region between the cathode and the anode. A small electric field region exists close to the cathode.

Simulating the dynamic performance of the same $P^+N^-P^+$ punch-through diode gave the results shown in Figures 2.4(a) through (f). They show that equilibrium after a turn on step was applied occurred in 30 psec. Figure 2.5(d) shows the distribution of holes vs. distance during switching from 2 V to 10 V as a function of time. The holes move swiftly across the channel attaining a level distribution in less than 0.5 nsec. Figure 2.5(e) shows that the hole current peaks close to the injecting junction at T = 0.03 nsec and the peak moves down the channel with time. This current is building up a space-charge which gives rise to the changing electric field.

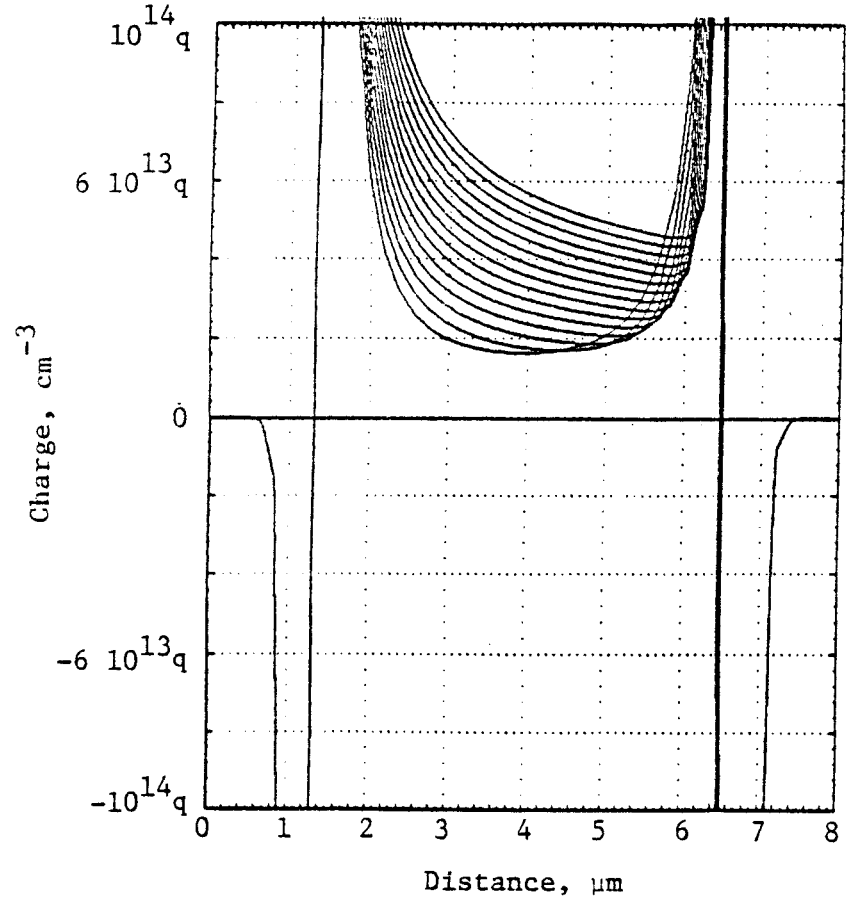


(a)

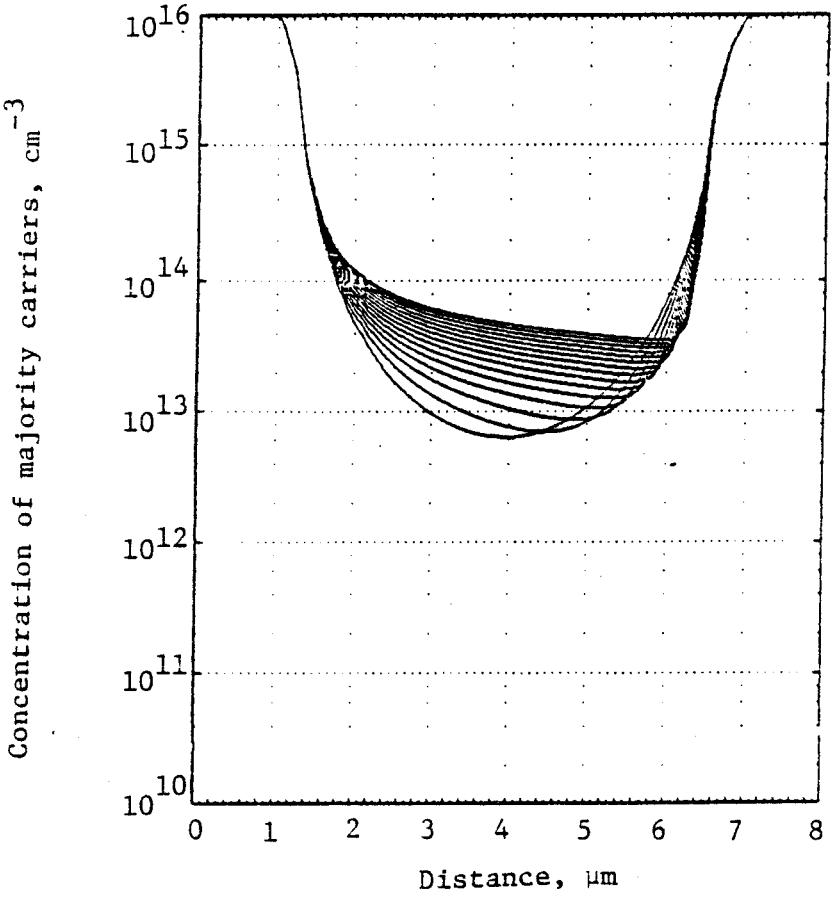


(b)

Fig. 2.3 Static analysis of a PTSCL diode for various biasing (.1V/step); electric field, (a), potential, (b).

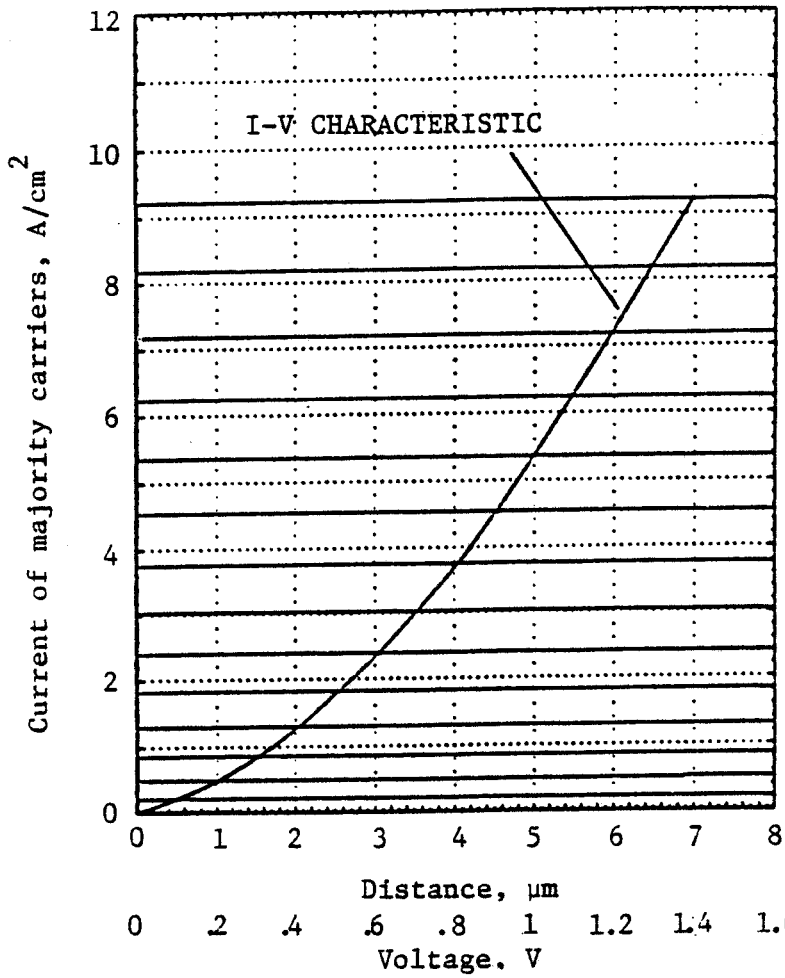


(c)

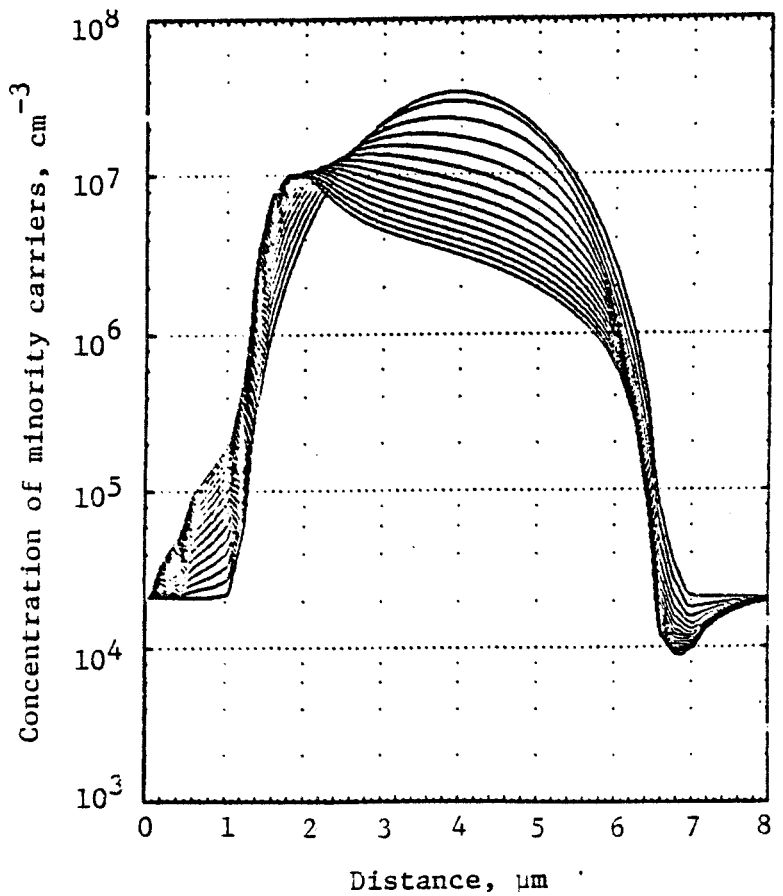


(d)

Fig. 2.3 (continued); charge, (c), concentration of majority carriers, (d).



(e)



(f)

Fig. 2.3 (continued); current of majority carriers, (e), concentration of minority carriers, (f).

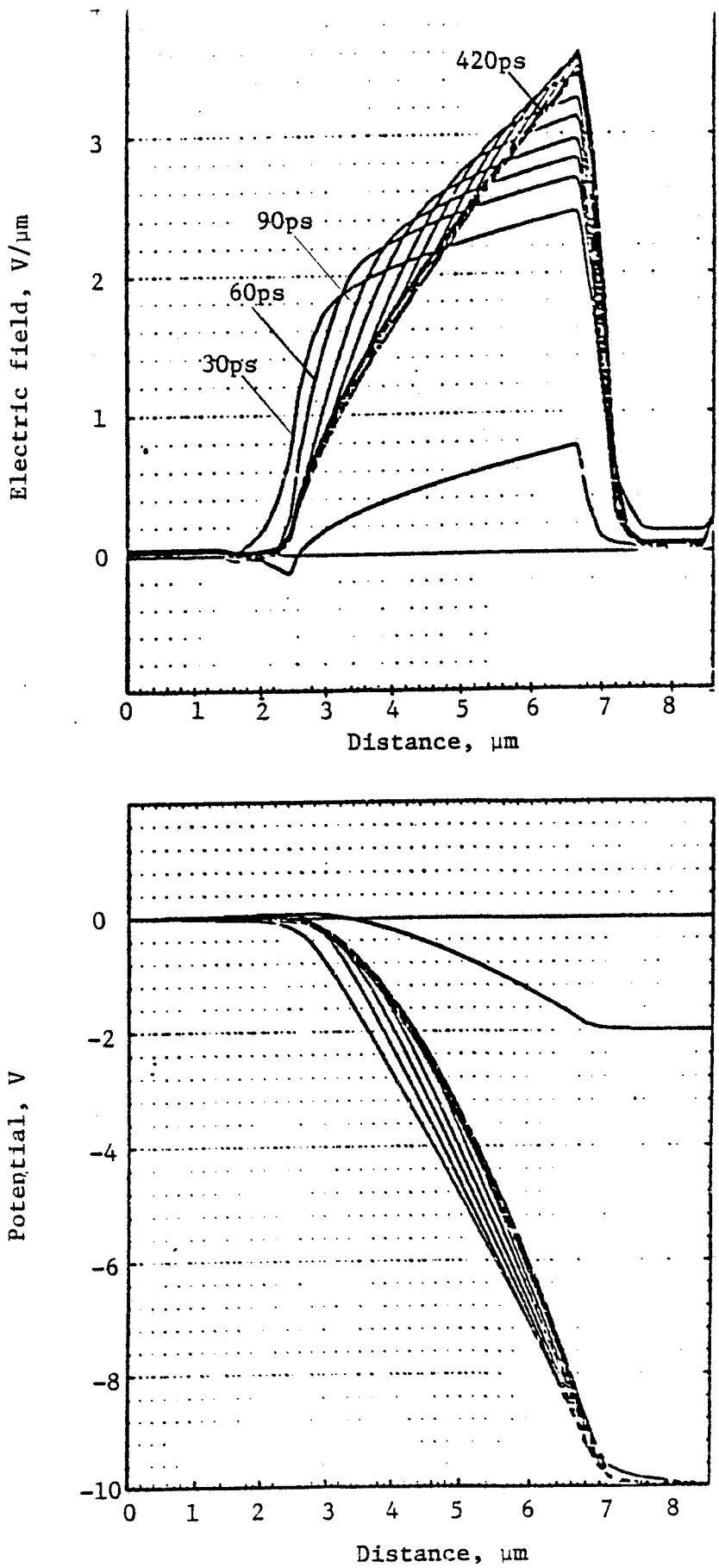
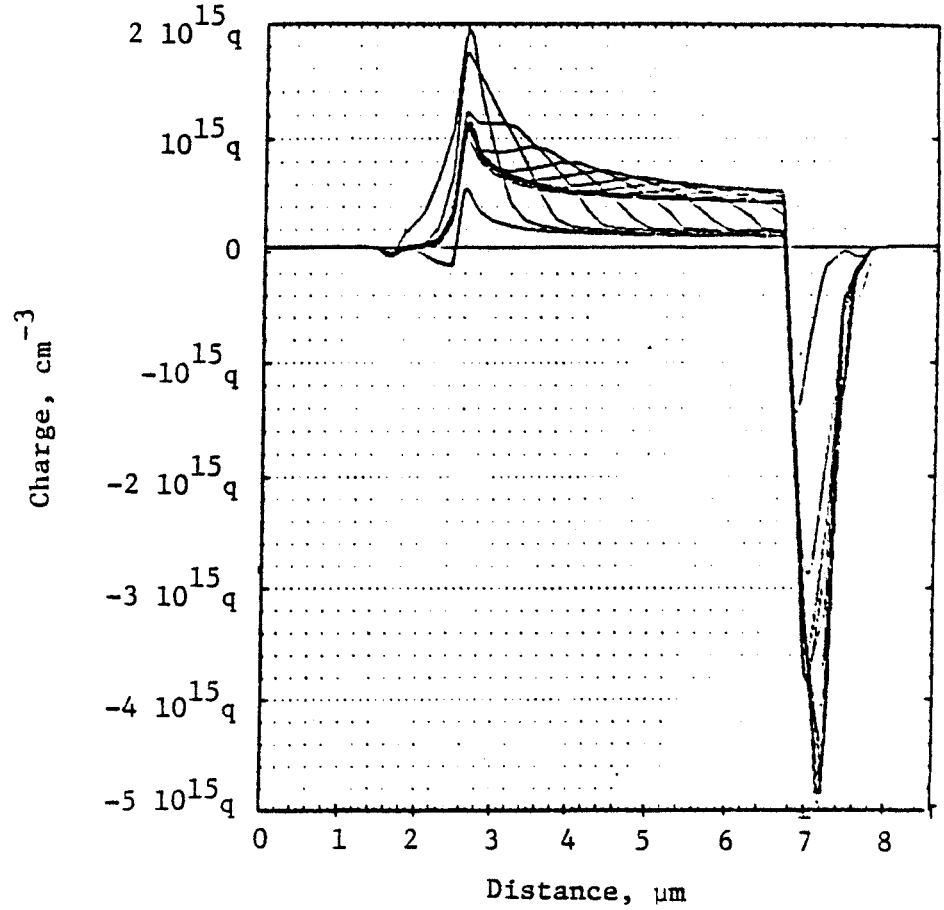
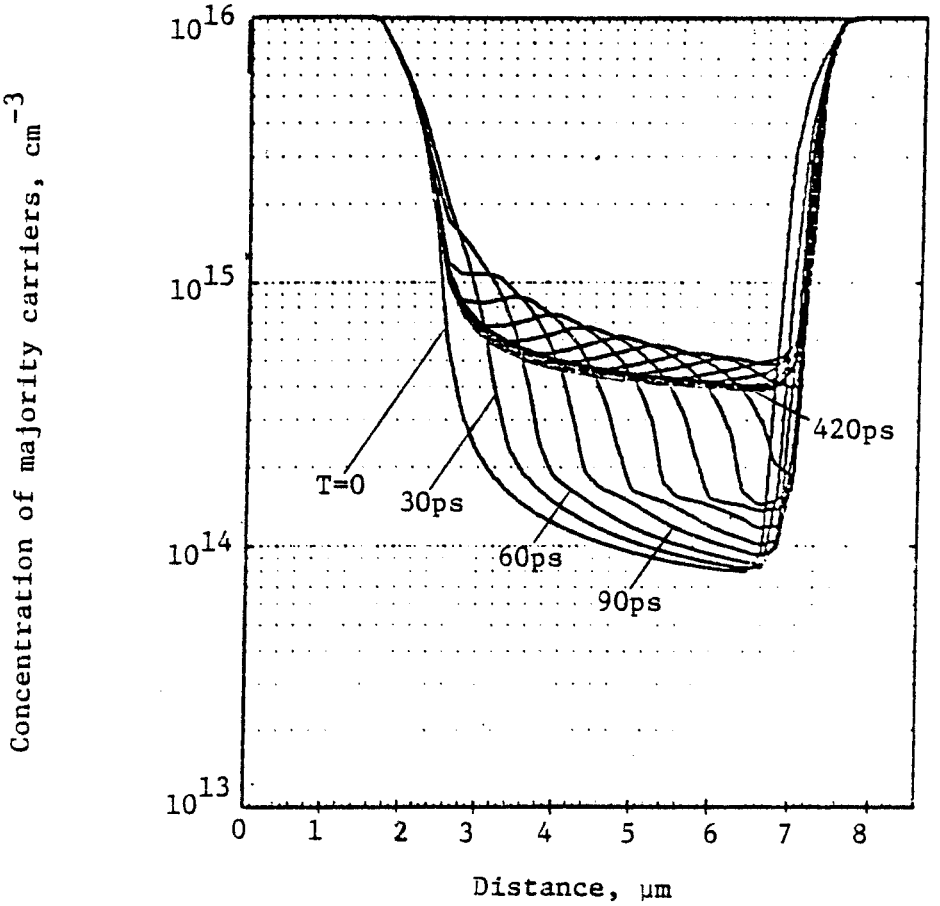


Fig. 2.4 Dynamic analysis of a PTSCL diode during switching from 2 V to 10 V (in 30 psec increments); electric field, (a), potential, (b).

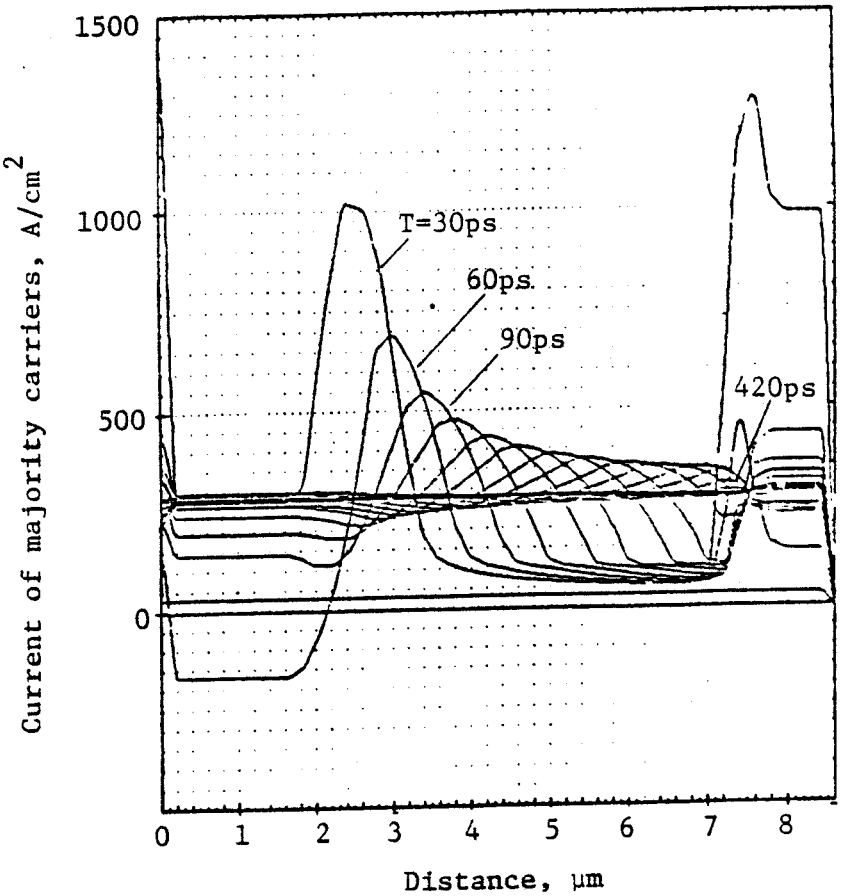


(c)

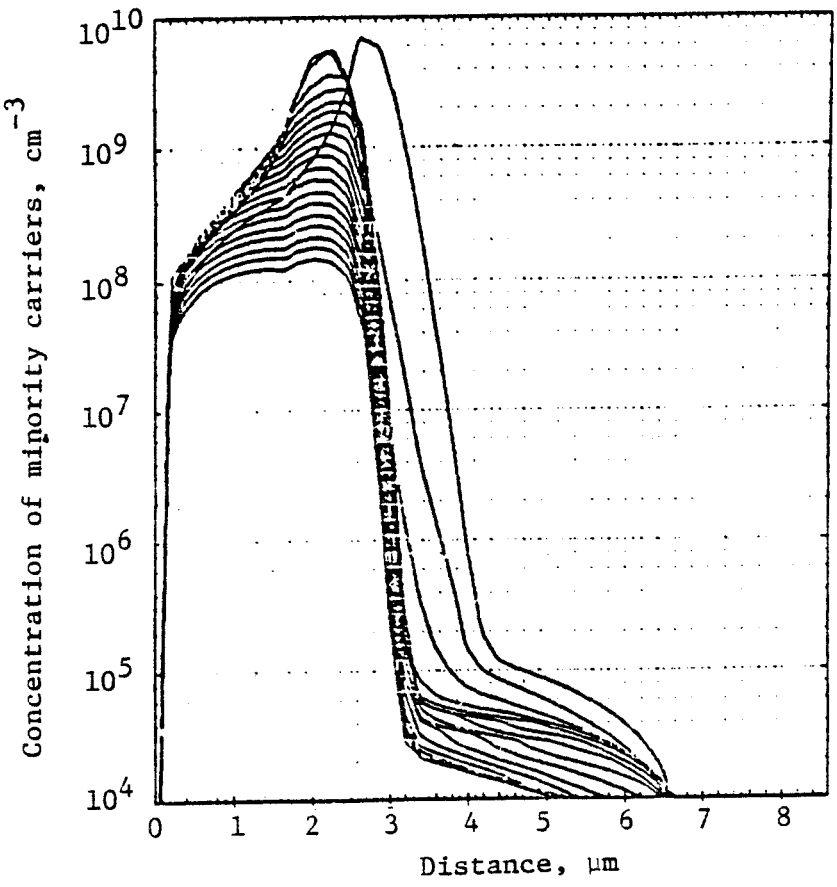


(d)

Fig. 2.4 (continued); charge, (c), concentration of majority carriers, (d).



(e)



(f)

Fig. 2.4 (continued); current of majority carriers, (e), concentration of minority carriers, (f).

3. DEVICE SIMULATION PROGRAMS

3.1 Introduction

Punch-through and space-charge phenomena are complicated in nature and, in order to fully investigate and understand their behavior, a computer simulation is necessary. Most of the existing computer simulation programs use simplified approaches, either neglecting space-charge or assuming charge neutrality [3.1]. In this way, computing time can be significantly reduced. However, for small geometry high speed devices for VLSI applications, such assumptions are not valid and a more general approach was needed. Thus, a GEneral one-dimensional semiconductor device performance SIMulation program (GESIM1) has been developed.

Technological implementation of triple/quadruple diffusion processing is critical to the investigated Saturation Protected Bipolar Transistors. To support such efforts, a BIpolar TRAnsistor Simulator program (BITRAS) has been developed. This specialized program simulates technology and performance of triple/quadruple diffused bipolar transistors and is more appropriate for the investigated specific, non-typical structures than the present versions of FABRICS [3.2] or SUPREM [3.3].

3.2 General one-dimensional device simulation program (GESIM1).

This program has been developed with no simplifying assumptions and allows the user to simulate the static and dynamic performance of a device. The GESIM1 simulation includes all parasitic effects and provides information about the internal detailed transient behavior of such devices. The input data required consists of the impurity concentration distribution and the applied terminal voltages. The steady-state solution is first found, and then transient analysis can be performed for any given voltage

excitation. It is also possible to incorporate the device to be simulated into a circuit. In this case transient circuit voltages and currents are determined from the simulation.

The program was written using five basic equations [3.4] given below:

- continuity equations:

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\,\mathrm{div}\,J_p + G_p - U_p \qquad (3.1\ a)$$

$$\frac{\partial n}{\partial t} = -\frac{1}{q}\,\mathrm{div}\,J_n + G_n - U_n \qquad (3.1\ b)$$

- transport equations:

$$J_p = -q D_p\,\mathrm{grad}\,p - q \mu_p\, p\,\mathrm{grad}\,\psi \qquad (3.2\ a)$$

$$J_n = q D_n\,\mathrm{grad}\,n - q \mu_n\, n\,\mathrm{grad}\,\psi \qquad (3.2\ b)$$

- Poisson's equation:

$$\mathrm{div}\,\mathrm{grad}\,\psi = -\frac{q}{\epsilon \epsilon_o}(N_d - N_a + p - n) \qquad (3.3)$$

where:

$$U_n = U_p = \frac{p\,n - n_i^2}{\tau_p (n + n_i) + \tau_n (p + n_i)} \qquad (3.4)$$

Instead of a standard finite difference method, a different approach was used. The device was divided into large regions with the number of mesh points being relatively small. Linearization is then performed and formulas

from analytical solution are applied. An explicit iterative procedure is used which is not as fast as the implicit method. However, it is easier to expand this one-dimensional program to a second dimension. Also, additional nodes will not seriously affect the computing time.

The structure of the program is shown in Figure 3.1 and examples of the program printout for a forward and reversed biased P-N junctions are presented in Figures 3.2(a) and (b). First, a summary of input data is printed (not shown here) and next, plots showing distributions of potential "V", electric field "E", charge "Q", holes "P", electrons "N", hole current "+", electron current "-", recombination current "R", Fermi potentials "*", "$", and decimal log of holes "@" and electrons "#".

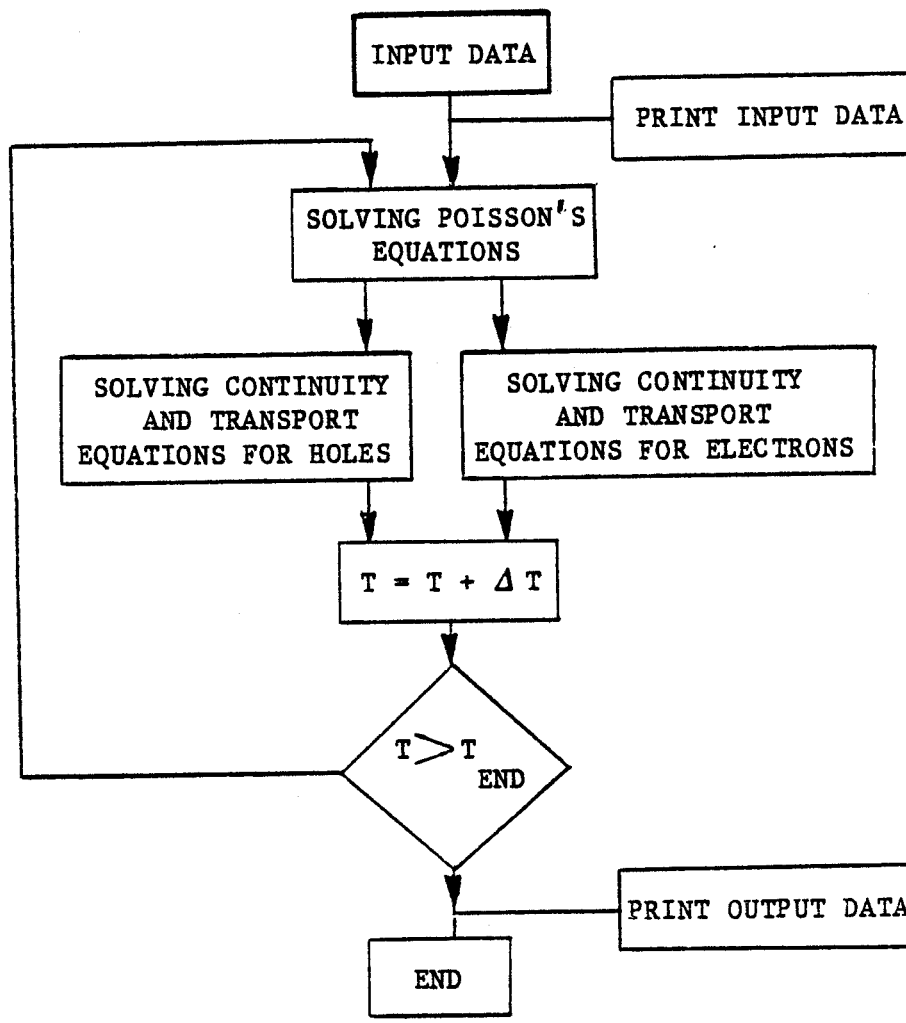


Fig. 3.1 Structure of GESIM1.

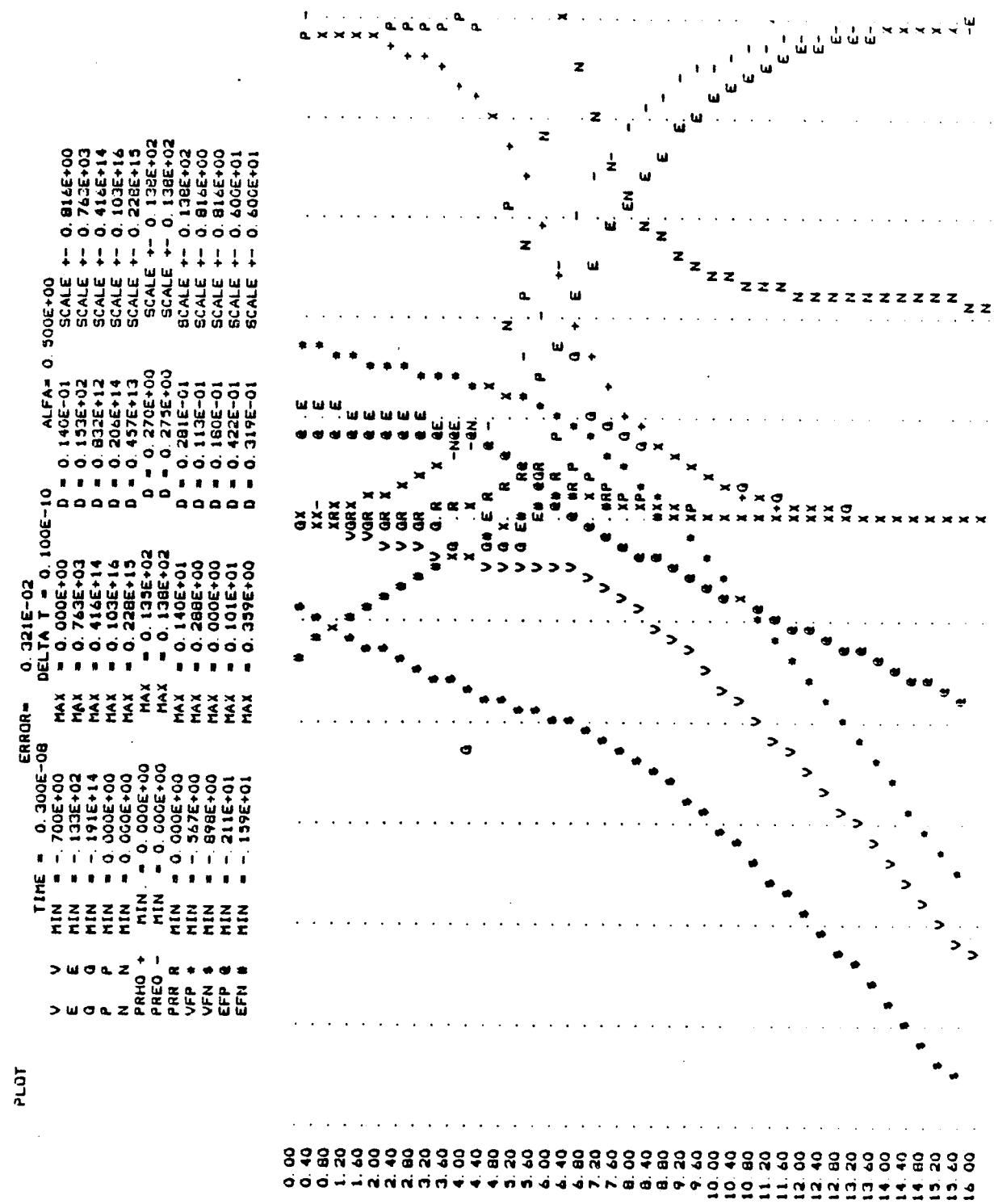


Fig. 3.2 Printout of GESIM1; for a forward biased P-N junction, (a).

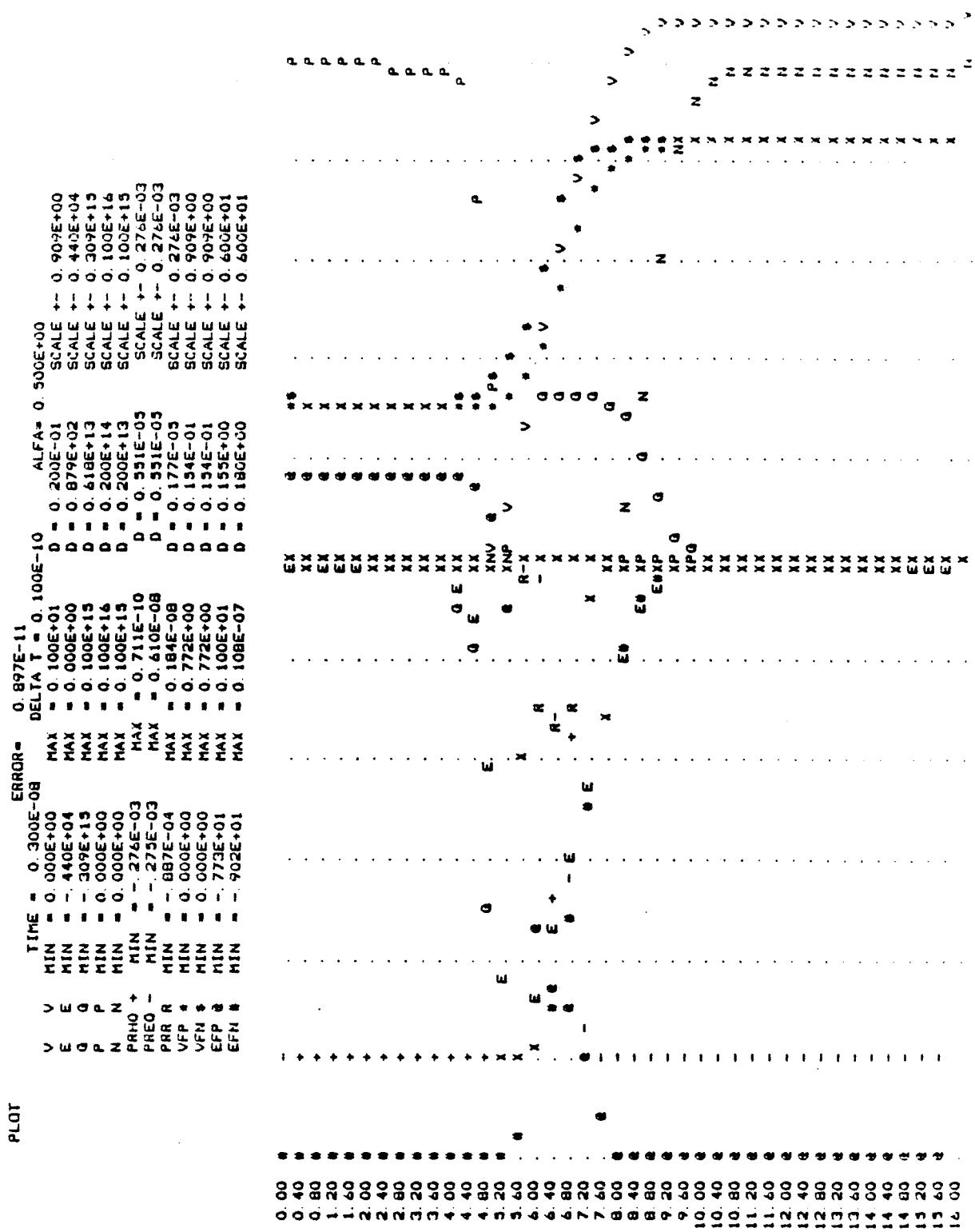


Fig. 3.2 (continued); for a reverse biased P-N junction, (b).

3.3 Bipolar transistor simulator program (BITRAS).

The program is both device and process simulation oriented using the processing parameters (temperatures, times and doses) as the input data. The simulation results are doping profiles and device electrical parameters which can be used as the input data for circuit simulation programs like SPICE2. BITRAS also allows for ploting of the resulting parameters and doping profiles. The program is relatively fast and can be used to perform the sensitivity analysis needed to optimize device design. It uses a combination of analytical and numerical procedures.

Figures 3.3 and 3.4 present simulation results for a quadruple diffused structure. First, a summary of input and output data (Figure 3.3) is presented for a structure fabricated according to a specific sequence: deep collector diffusion, shallow collector diffusion, deep base diffusion and emitter diffusion. Doping profiles after each of these steps are shown next, Figures 3.4(a), (b), (c), and the resulting doping profile of the quadruple structure are presented in Figure 3.4(d).

NUMBER OF IMPURITY DISTRIBUTIONS = 4
NUMBER OF JUNCTIONS = 3
NUMBER OF LAYERS = 4

TCHNOLOGICAL PROCESS PARAMETERS

NUMBER	TIME	TEMP	DOSE	XIMP	DYF	NSUR	LD	XQ	R/SQUARE	XJ
1	0.120E+04	0.113E+04	0.100E+14	0.000E+00	0.417E-12	0.299E+17	0.188E-03	0.000E+00	0.391E+03	0.648E-03
2	0.180E+03	0.113E+04	0.100E+14	0.000E+00	0.417E-12	0.760E+17	0.742E-04	0.000E+00	0.348E+03	0.687E-03
3	0.300E+02	0.110E+04	-0.200E+15	0.000E+00	0.306E-12	-0.270E+19	0.419E-04	0.000E+00	0.228E+03	0.103E-03
5	0.600E+02	0.110E+04	0.300E+16	0.000E+00	0.167E-12	0.688E+20	0.246E-04	0.000E+00	0.222E+02	0.112E-03

SUBSTRATE CONCENTRATION = -0.100E+16

LAYERS PARAMETERS

NUMBER	RSQ	DOSE	GUMMEL	BETATF	BETATR	TF	TR	XS	XE
1	0.220E+02	0.286E+16	0.135E+16	0.130E+05	0.496E+03	0.770E-09	0.201E-07	0.000E+00	0.112E-03
2	0.625E+04	-0.378E+13	-0.319E+12	0.537E+06	0.165E+06	0.186E-10	0.604E-10	0.112E-03	0.170E-03
3	0.112E+04	0.485E+13	0.443E+12	0.305E+04	0.307E+03	0.328E-08	0.326E-07	0.170E-03	0.695E-03
4	0.252E+04	-0.501E+13	-0.144E+12	0.264E+02	0.272E+02	0.378E-06	0.368E-06	0.695E-03	0.577E-02

OTHER PARAMETERS OF LAYERS - AVERAGE

NUMBER	UMAJ	UMIN	AVCON	TAUN	TAUP	SIGMA	RO	GUENGA
1	0.993E+02	0.109E+03	0.254E+20	0.101E-05	0.101E-05	0.404E+03	0.247E-02	0.217E+14
2	0.265E+03	0.552E+03	-0.639E+17	0.883E-05	0.883E-05	0.279E+01	0.358E+00	-0.319E+12
3	0.115E+04	0.449E+03	0.924E+16	0.989E-05	0.989E-05	0.170E+01	0.587E+00	0.423E+12
4	0.494E+03	0.134E+04	-0.987E+15	0.100E-04	0.100E-04	0.780E-01	0.128E+02	-0.144E+12

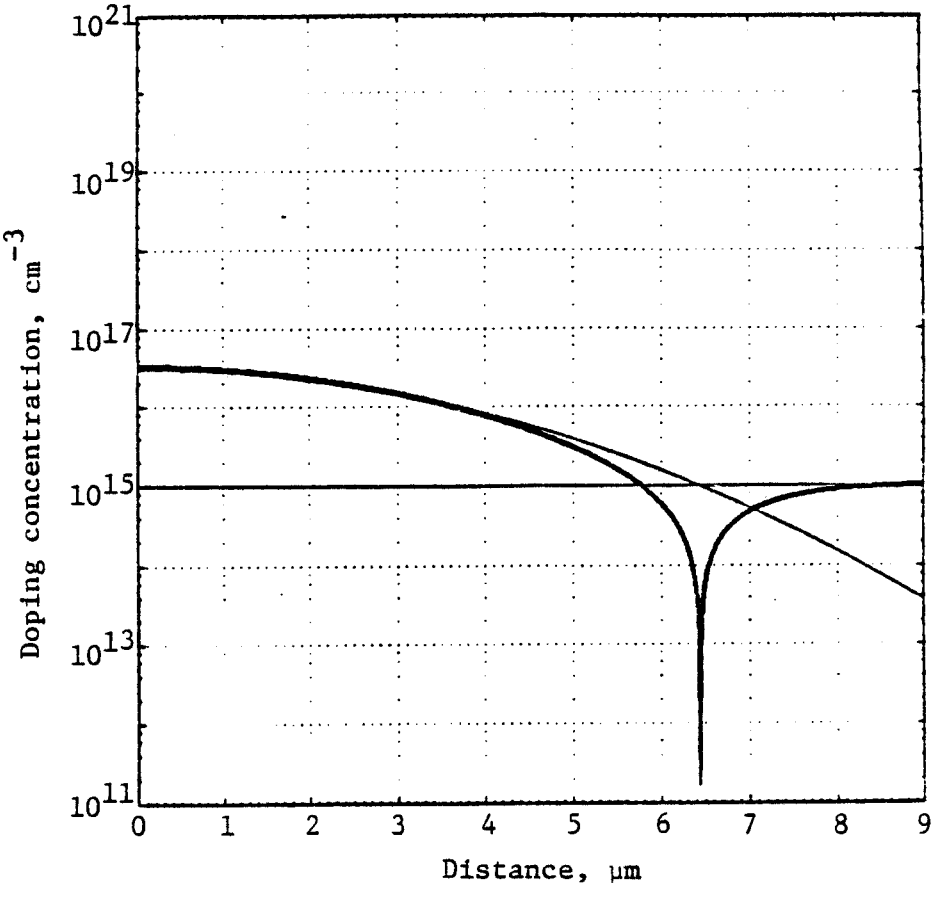
JUNCTION PARAMETERS

NUMBER	XJ	XJL	XJR	WJ	CJ	VFJ	JSATN	JSATP	BETAINJ	CONJ
1	0.112E-03	0.106E-03	0.121E-03	0.150E-04	0.702E-07	0.832E+00	0.155E-11	-0.105E-09	0.680E+02	0.447E+18
2	0.170E-03	0.155E-03	0.188E-03	0.331E-04	0.318E-07	0.744E+00	-0.105E-09	0.796E-10	0.756E+00	0.455E+17
3	0.695E-03	0.621E-03	0.788E-03	0.167E-03	0.630E-08	0.562E+00	0.796E-10	-0.233E-09	0.293E+01	0.100E+16

TRANSISTOR PARAMETERS

NUMBER	BETA	ISAT	TAU	CJ
1F	0.680E+02	0.107E-09	0.248E-10	0.702E-07
1R	0.132E+01	0.185E-09	0.129E-08	0.318E-07
2F	0.756E+00	0.185E-09	0.129E-08	0.318E-07
2R	0.341E+00	0.313E-09	0.140E-06	0.630E-08

Fig. 3.3 Summary of input and output data of BITRAS for a quadruple diffused bipolar transistor.



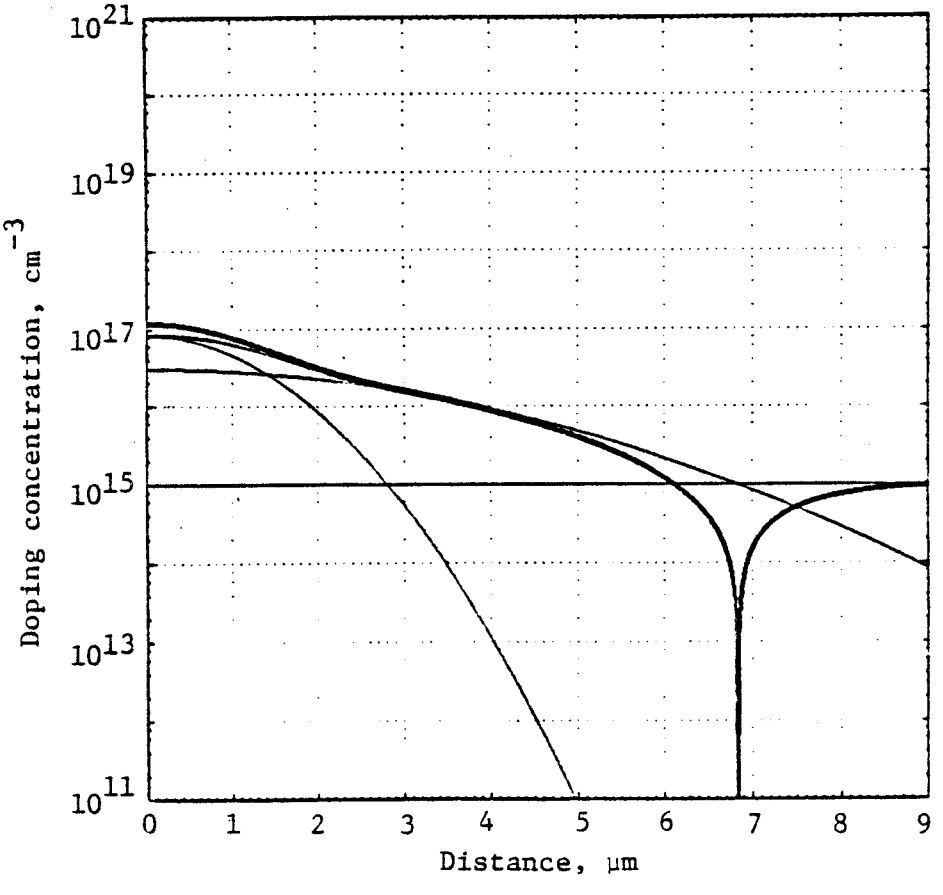
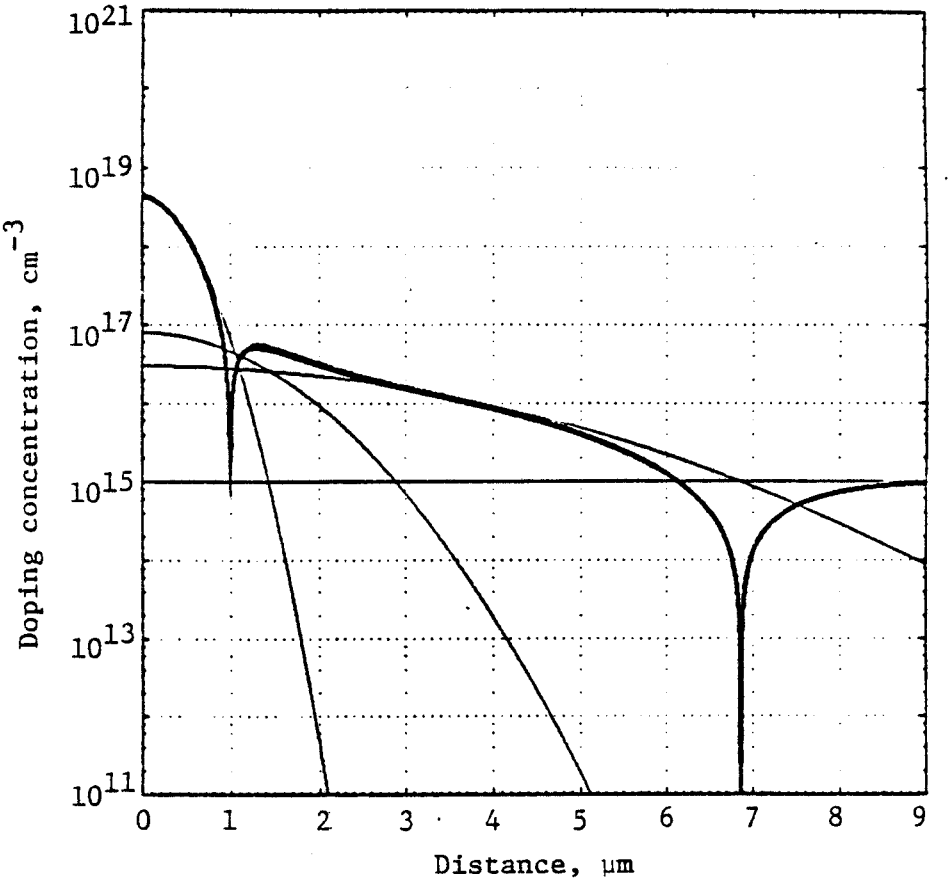
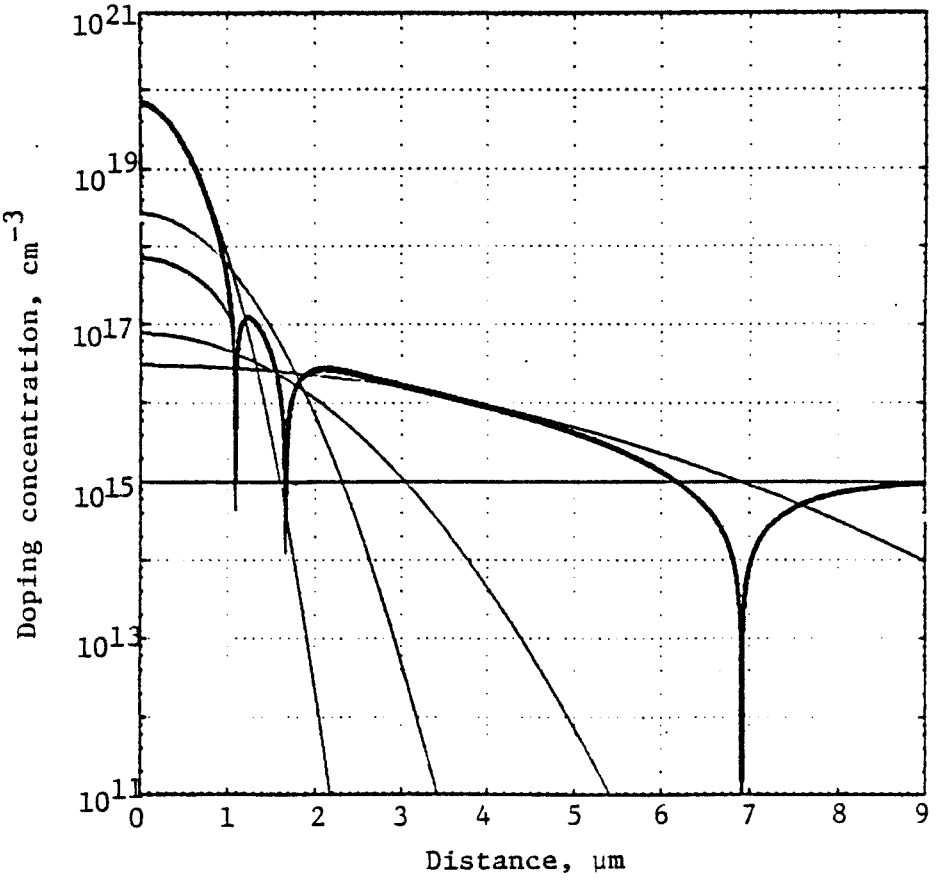


Fig. 3.4 Doping profiles after each fabrication step of the quadruple diffused structure; deep, (a), and shallow collector diffusion, (b).



(c)



(d)

Fig. 3.4 (continued); deep base, (c), and emitter diffusion, (d).

PART 2 - DEVICE FABRICATION

4. TECHNOLOGY/PROCESS DEVELOPMENT

4.1 Introduction

This section describes laboratory work done to realize techniques and devices applicable to VLSI technology. Fabrication in silicon of thin base bipolar transistors and space-charge limited loads has been completed. Reactive ion etching and local oxidation techniques for an isoplanar process have been developed. Fabrication of thin base bipolar transistors with Static Induction Transistor (SIT) protection against saturation using the isoplanar process is under development. Also, fabrication of SIT protected and PNP protected NPN transistors without LOCOS is in progress.

4.2 Development/modification of the Local Oxidation Technique

The development/modification of Local Oxidation Techniques has been successfully completed. The parameters, necessary to realize a self-aligning isoplanar process with 2.5 micron geometry, were established. Anisotropic reactive ion etching through 2000 angstroms of silicon nitride, approximately 250 angstroms of silicon dioxide, and 4500 angstroms of single crystal silicon has been demonstrated using a Perkin Elmer Randex Model 3140 Single-Target Sputtering system. Figure 4.1 is a Scanning Electron Microscope (SEM) display photo showing the reactive ion etched areas with widths of 2.6 microns.

Satisfactory dry etching was achieved with 65 watts of R.F. field power, 15 microns of Freon-14 pressure, and 20 minutes of etch time. Data for the Model 3140 indicates a single crystal silicon etch rate of 280 angstroms per minute. The etch rate for silicon nitride is 300 angstroms

per mimute, and the etch rate for KTI 747 negative photoresist is 250 angstroms per minute. These rates are valid for the process parameters given above including the 20 minute time interval (etching does not appear to be linear with time).

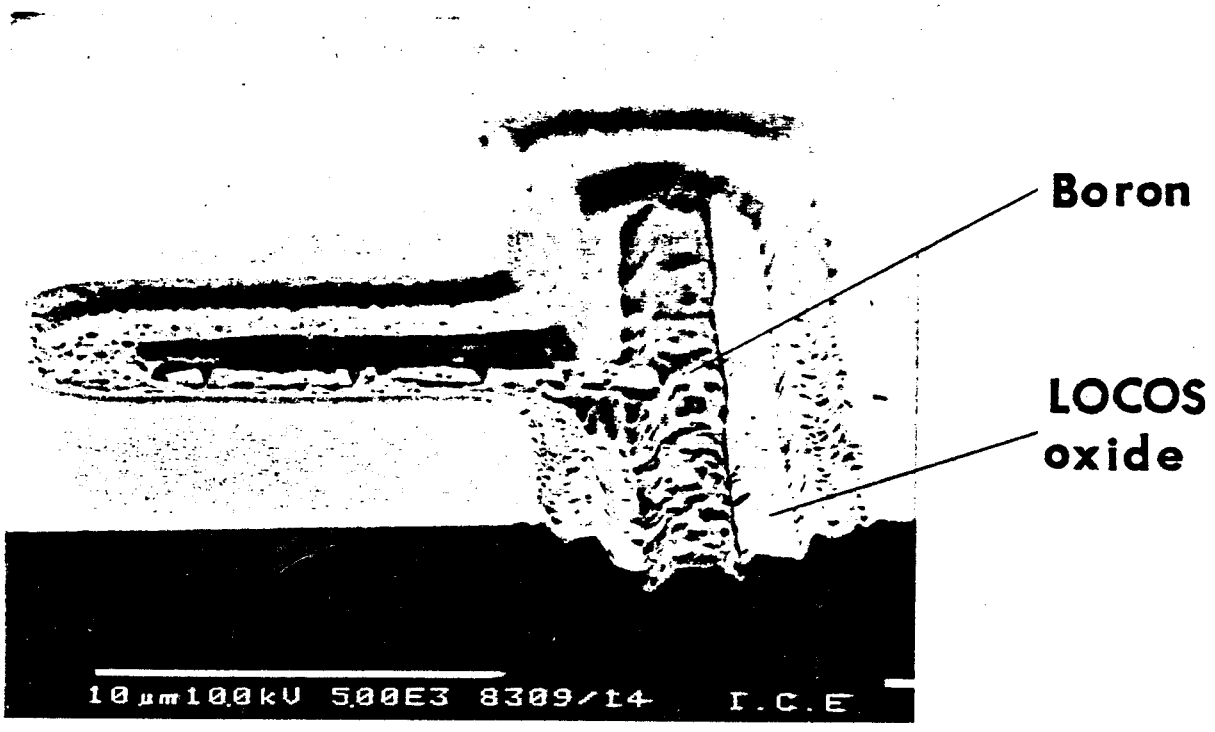
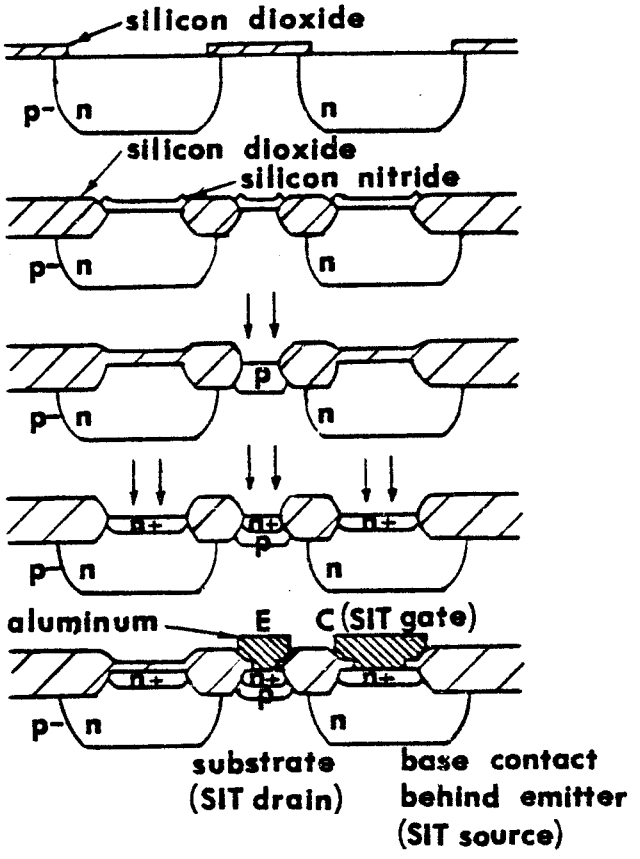


Fig. 4.1 SEM photo of reactive ion etched device with 2.6 micron geometry.

Because of the etch rates and photoresist thickness needed for realizing small geometries, a two step negative photoresist process was developed. KTI-747 (viscosity = 43 to 45) photoresist is spun on at 5500 rpm. After 7 minutes of the first step reactive ion etching, the photoresist is no longer an effective mask. The photoresist is then stripped. The same photolithography is repeated, and 8 to 12 minutes of second step reactive ion etching results in sufficient silicon etch to realize an isoplanar LOCOS. Of course, shallower oxide moats can be fabricated with a single step photoresist procedure.

Oxidation for the LOCOS process is standard. Wafers are subject to dry oxygen, wet oxygen, then dry oxygen at 950 degrees C for 5.5 hours. The problem of fissuring of thick oxides was overcome by furnace ramping. Ramping up and down of the furnace temperature was suggested by our S.R.C. mentors from Motorola [4.1], and has been adopted for all high temperature processing steps.

This LOCOS process has been adopted for the fabrication of the Static Induction Transistor (SIT) protected NPN bipolar transistors. The processing sequence for fabricating these structures utilizing composed masking and self aligning is shown in Figure 4.2. Devices fabricated with this process displayed emitter collector shorts. A complete discussion of this problem is included in section 4.3 of this report.



1. DEEP n-TYPE IMPLANT AND DRIVE.

2. SILICON NITRIDE DEPOSITION AND ETCHING, AND LOCOS OXIDATION.

3. BASE PHOTOLITHOGRAPHY AND DOUBLE BORON IMPLANT AND DRIVE.

4. EMITTER PHOTOLITHOGRAPHY AND PHOSPHORUS IMPLANT AND DRIVE.

5. FINISHED DEVICE.

Fig. 4.2 Processing sequence for SIT protected NPN bipolar transistors.

Improvement and recharacterization of the Model 3140 Sputtering system is continuing. The characterization (including etch rates) completed thus far shows good agreement with investigations of similar parallel plate machines [4.2]. New Static Induction Transistor designs and their layouts have been completed. These devices are fabricated both with and without the LOCOS technique. Therefore, fabrication of some SIT devices avoids the complexity of the LOCOS process. This isolates the problems related to the LOCOS process from problems related to either SIT or npn bipolar transistor operation.

4.3 Fabrication of thin base bipolar transistors

Thin base NPN bipolar transistors have been fabricated in deeply diffused n-type regions on p-type silicon substrates and directly on n-type silicon substrates. Typical base-collector junction depths are .9 microns. The fabrication of the base is by a double diffusion process [4.3]. A low dose implant is followed by a long (15 minutes at 1100 degrees C) drive-in to create a lightly doped active base with a depth of about .9 microns. A second higher dose (one order of magnitude higher) implant is followed by a lower temperature (950 degrees C) oxidation to create a shallow heavily doped extrinsic base for ohmic contact. Typical emitter-base junctions are .5 microns. Emitters are fabricated by a phosphorus implant. Therefore, the processing steps include three (for n-type substrates) or four (for p-type substrates) ion implants, and similarly three or four high temperature diffusion steps.

Although transistors fabricated on p-type substrates are actually quadruple diffused structures, the deep n-type diffusion may be seen as a process simplification. The 6 micron deep n-type diffusion is a simple alternative to epitaxy growth, and it can provide for isolation tubs through

standard photoresist procedures (or it can be combined with isolation oxide techniques).

Figure 4.3(a) shows typical transistor output characteristics for devices fabricated in n-type silicon substrates with no deep diffusion. These devices have typical base-collector breakdown voltages of 56 volts, base-emitter breakdown voltages of 6.2 volts, and forward betas of 50. Figure 4.3(b) shows typical transistor output characteristics for devices fabricated in deep n-type isolation regions on p-type silicon substrates. These devices have typical base-collector breakdown voltages of 12 volts, base-emitter breakdown voltages of 5 volts, low Early voltage, and forward betas of 5.

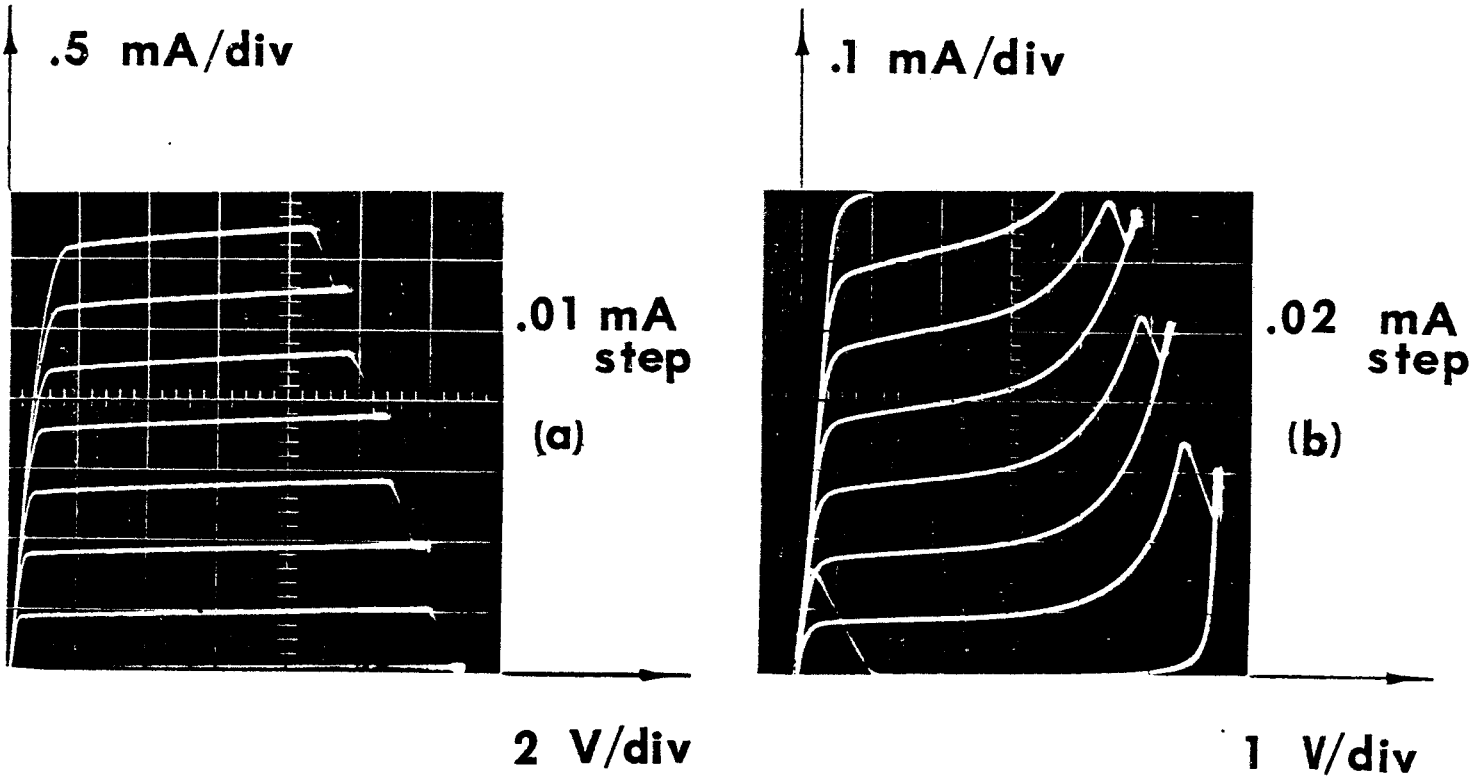


Fig. 4.3 Common emitter output characteristics: n-type substrate, (a), p-type substrate, (b).

Reliable data for very deep (6 micron) phosphorus implant and diffusion, and shallow boron implant and diffusion into the deep phosphorus diffusion were not available in standard references. To improve the quality of the quadruple diffused transistors, experimental data, including surface concentrations and diffusion lengths, was collected over a range of values. Appropriate concentration profiles have been established using this data in conjunction with the BITRAS simulation program. Also, from this data, Figures 4.4(a) and 4.4(b) were constructed to display implant dose as a function of sheet resistance/junction depth product for quadruple diffused transistors.

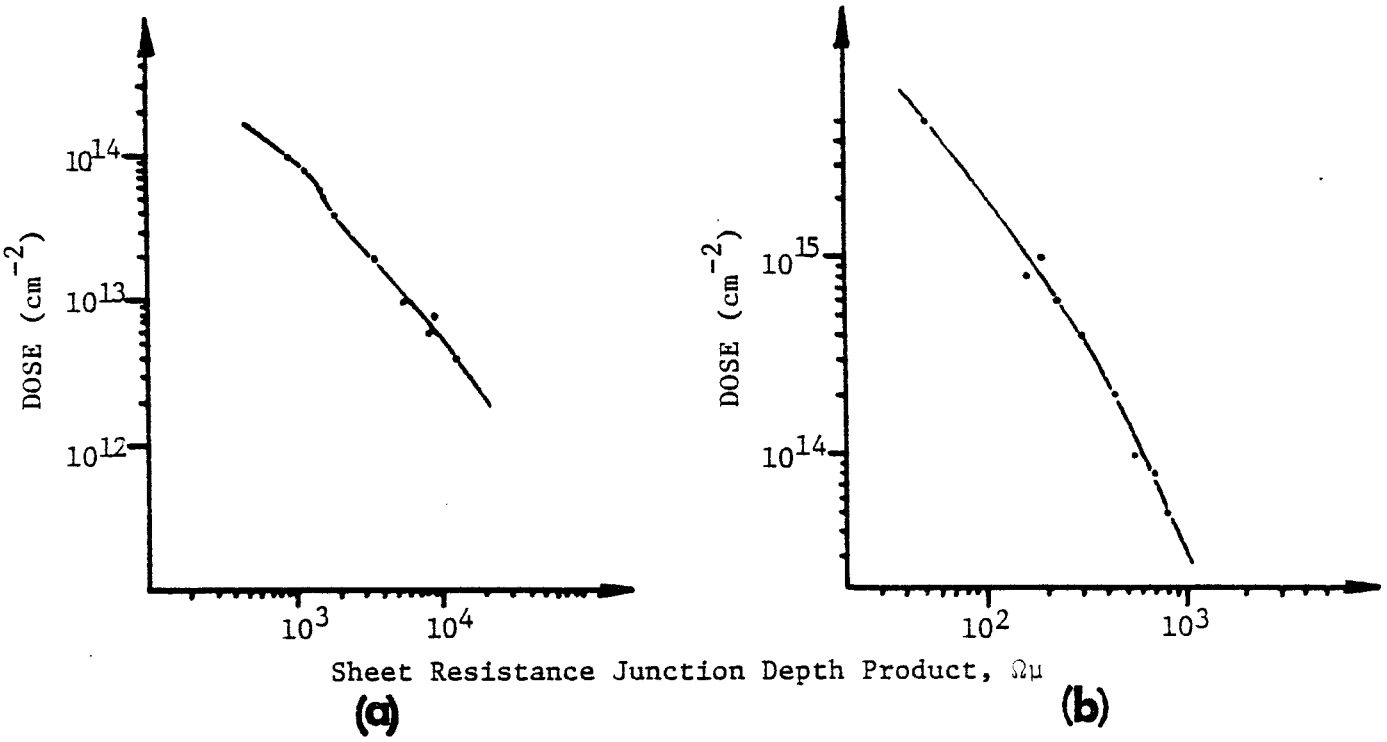
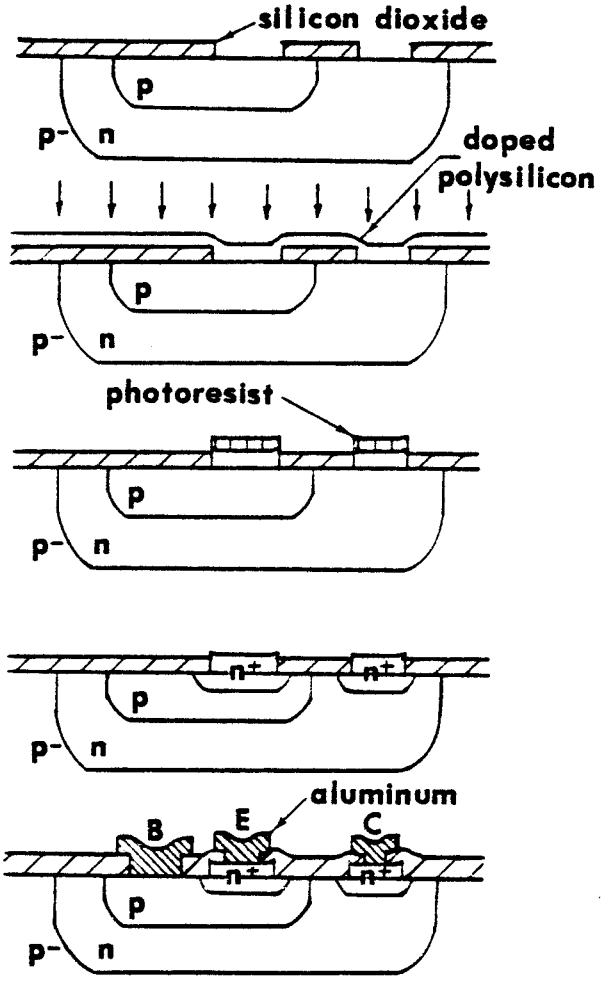


Fig. 4.4 Phosphorus implant dose into uniformly doped p-type silicon as a function of the sheet resistance/junction depth product, (a); boron implant dose into deep n-type diffusion as a funtion of sheet resistance/junction depth product, (b).

Initially, transistor quality improvement efforts concentrated on fabrication parameters which produced good results when simulated on the BITRAS program. Specificly, base width and concentration was reduced, thereby reducing the active base Gummel number, and the emitter doping and depth was increased, thereby increasing the emitter Gummel number.

These efforts to improve beta and decrease base width modulation resulted in emitter collector shorts. Consultation with S.R.C. mentors from Motorola resulted in the following process changes. First, aluminum sintering after metalization was reduced and, subsequently, not performed at all. The intent of this procedure was to eliminate aluminum spiking. Results show that avoiding the sintering step in many cases produced working devices which would have otherwise had emitter collector shorts. Also, to alleviate this problem, an aluminum sputter target with 2% silicon added has been purchased for use in the Perkin Elmer Randex Model 3140 Single-Target Sputtering system. Second, in order to improve beta (as well as helping the aluminum spiking problem) an additional mask has been made, and polysilicon emitter devices have been fabricated. Polysilicon deposited on emitters doped heavily with phosphorus will reduce the emitter hole gradient and, consequently, the base current. In initial fabrication runs, the polysilicon emitter areas were overetched. Subsequent ion implantation and drive-in resulted in overly deep phosphorus diffusion in the overetched regions. The process has been revised such that the polysilicon is first implanted with phosphorus and then the polysilicon over non-emitter areas is removed by reactive ion etching. The revised polysilicon emitter process beginning with emitter photolithography is shown in Figure 4.5.

Revised thin base bipolar transistor layouts of various geometries with and without polysilicon emitters have been made. The mask set has been made with the idea of simplifying the processing and increasing the number of working devices produced. A thin base bipolar inverter with a space charge limited load is included on the masks. Fabrication of these simplified devices is continuing.



1. Emitter photolithography.

2. Polysilicon deposition and phosphorus implant.

3. Reactive ion etching of doped polysilicon.

4. Photoresist removal and emitter drive-in.

5. Finished device after contact photolithography and metalization.

Fig. 4.5 Polysilicon emitter process.

4.4 Fabrication of punch-through space-charge-limited loads

Space-charge-limited loads of the configuration shown in Figure 4.6 were fabricated and tested. Resistance values for a 6 micron separation space-charge limited load were as high as 67 kohm whereas a 10 square dogbone substrate resistor provided only 33 kohm on the same wafer. P-type substrate sheet resistance was 3.33 kohm/square. The device of Figure 4.6 was implanted with 5x10**14 atoms/cm**2 of phosphorus and driven-in to a junction depth of 1.4 microns. The resulting n^+ areas had a sheet resistance of 75 ohms/square. Resistance values for 3, 4, 5, and 6 micron spacings of the space-charge-limited load are summarized in Table 4.1.

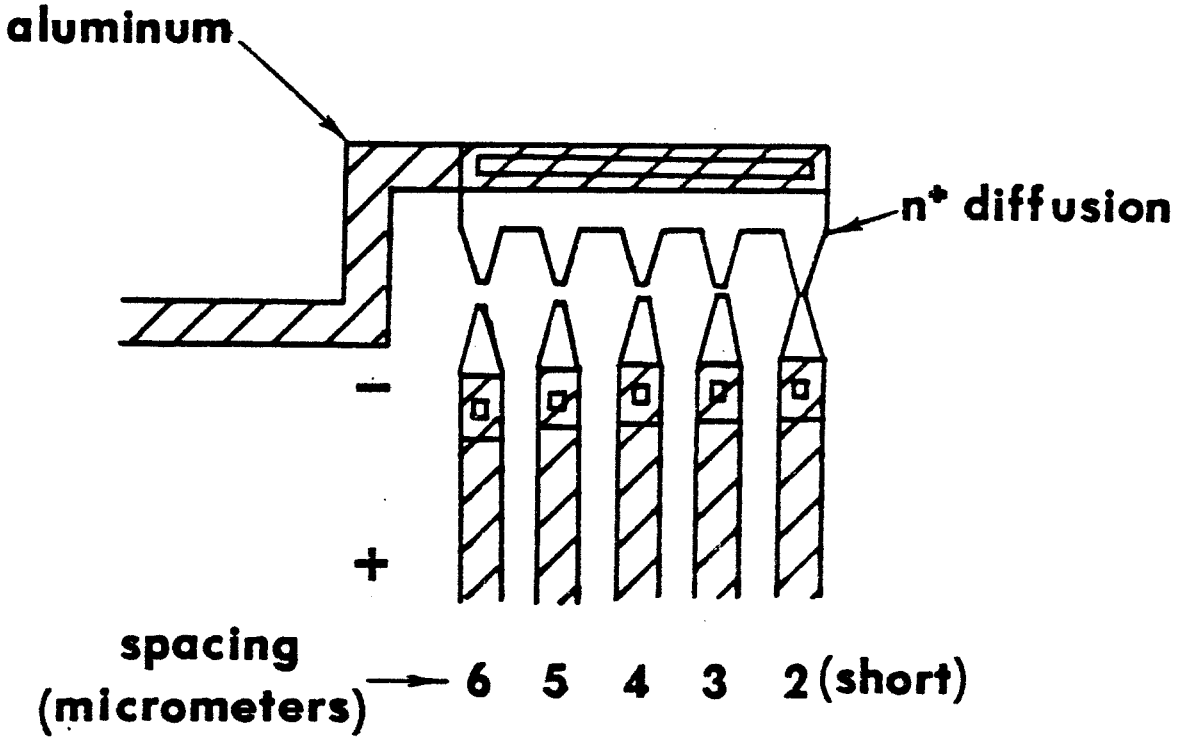


Fig. 4.6 Space-charge-limited load layout.

SPACE-CHARGE LIMITED LOAD SPACING (microns)	RESISTOR VALUE (kohms)
6	67.0
5	37.5
4	30.0
3	16.7

(Substrate sheet resistance: 3.33 kohms/square)

Table 4.1 Resistance for various space-charge-limited load spacing.

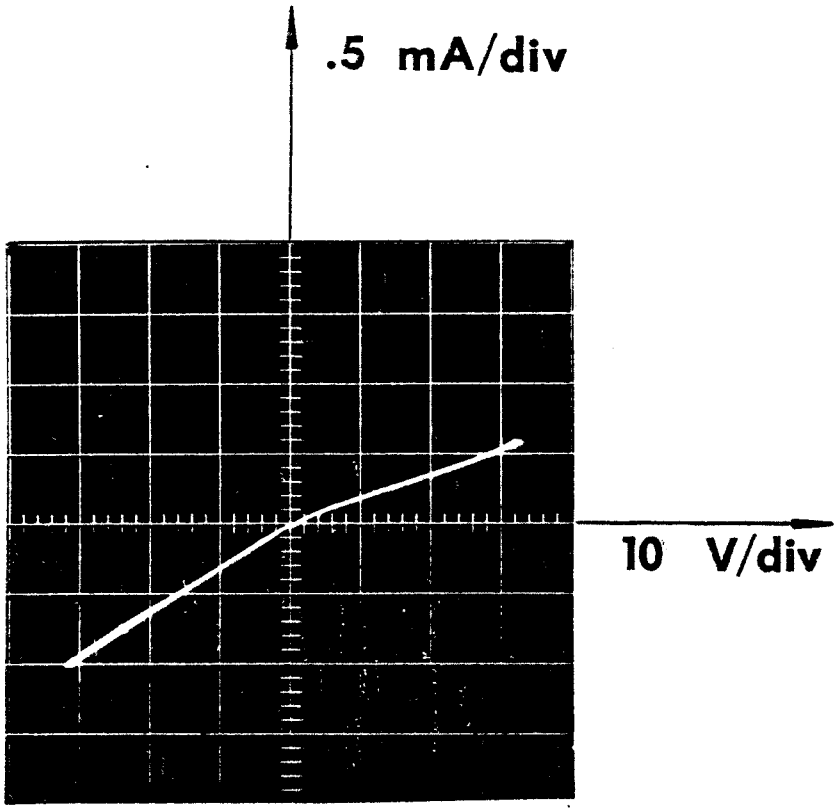


Fig. 4.7 I-V characteristics for space-charge-limited load.

Typical I-V curves for these devices are shown in Figure 4.7. Inspection of these characteristics shows that resistance is greater for the polarity shown as positive in Figure 4.6. Punch-through voltages could not be measured on a standard curve tracer at the wafer background concentrations of these devices [4.4]. The slight curvature of the I-V characteristics indicates increasing resistance with higher voltage. It is thought that these effects may be caused by interaction between the variously spaced loads. The spacing between the space-charge-limited loads was 10 microns.

A revised layout for space-charge-limited loads has been made to minimize interaction between loads with different spacings. Masks have been made with 50 micron spacing between the space-charge-limited loads. Also included on these masks is an inverter utilizing a space-charge-limited load.

4.5 Fabrication of Static Induction Transistors

Static Induction Transistors using LOCOS oxidation techniques and phosphorus sources were designed in the first quarter of this project (see Figure 4.2). Since then, many fabrication trials have been made. The major problems encountered have been source and channel (emitter and base) shorts, soft breakdowns, and aluminum penetration through the source deep into the channel.The SIT devices have been redesigned, and masks have been completed for structures both with and without LOCOS. To alleviate the major problems mentioned, n-channel devices will incorporate a polysilicon source. The polysilicon source will be phosphorus doped similar to the polysilicon emitters of the thin base transistors. Fabrication of these devices is now in progress.

4.6 Fabrication of triple/quadruple diffused polysilicon emitter transistors with protection

Polysilicon emitter transistors on both n and p-type substrates with both SIT and PNP Saturation Protection Transistors have been designed, and masks have been completed. In the initial fabrication runs, the polysilicon emitter areas were overetched and subsequent ion implantation and drive-in resulted in overly deep phosphorus diffusion in the overetched regions. The process has been revised to solve this problem (see Figure 4.5), and fabrication of these devices is now in progress.

PART 3 - PLANS FOR FURTHER STUDIES

5. SOFTWARE DEVELOPMENT FOR DEVICE AND CIRCUIT DESIGN

New structures, such as Space-Charge-Limited Loads, or SIT/PNP Saturation Protected Transistors require computer simulation tools that do not employ the various simplifications usually used. Such a general program for transient and static analysis of semiconductor devices has been initiated and its one-dimensional version developed. Some of the simulation results are included in the project annual report. However, there are still some convergency problems to be solved in GESIM1. They appear when very high impurity concentrations are present. To ensure convergency in such cases, very small time steps have to be used leading to prohibitively long CPU times. The program also requires various modifications to ensure easy handling of the input and output data. It is also our intension to expand the program to a second dimension, so that device structures employing complex geometries can be modeled and reliable results obtained.

In order to support technological efforts to fabricate triple/quadruple diffused structures, a program has been developed to simulate the fabrication sequence and to establish the proper processing parameters. Its present version, BITRAS, developed on a VAX 780 computer, has proved to be an essential tool in developing appropriate technological parameters for the desired device performance. The program still requires further work in expanding input/output data options and further modifications in matching simulation results to experiments.

Thus, the goals of the simulation oriented research are to:

1. continue the development of the GESIM1 program to simplyfy input requirements and the form of the output,

2. continue the development of the BITRAS program in a similar fashion as (1),
3. investigate the feasibility of expanding the GESIM1 program to include two-dimensional simulations.

6. FABRICATION

The fabrication efforts could lead to many high speed bipolar logic gates with switching speeds similar to ECL performance but much lower per gate heat dissipation requirements. This could allow denser packing of the circuits. In addition, the SIT or PNP saturation protected devices can be coupled with the space-charge-limited loads to reduce resistor dimensions, thereby increasing the device density. In order to realize such high speed, bipolar logic gate arrays, it is necessary to pursue research in an organized fashion.

The Space-Charge-Limited Load has been fabricated for use as a resistor, as described in the project annual report. A major problem associated with this device is the sensitivity of the desired parameter, resistance, to device geometries, especially spacing. The objective of the research is to identify the source of the variations and summmarize their impact. Based on previous experiences with the theory, simulation, and fabrication of such devices, success is expected in this aspect of the proposed research.

In order to fabricate the saturation protected NPN bipolar devices, it is necessary that either a quadruple diffused transistor process be developed or else a triple diffused process with a polysilicon emitter. Of the two approaches, the polysilicon emitter process appears to provide the best chance of success. The process should avoid the emitter metallization

generated punch-through problems encountered with this year°s work, as described in the annual report. Thus, the major effort in the fabrication area will be aimed at realizing the SIT and PNP saturation protected NPN bipolar devices. A final effort will be aimed at realizing the saturation protected devices on the same chip with space-charge-limited loads to realize a new family of high speed, low power, bipolar logic.

Thus, the goals of the fabrication effort are to:

1. continue the development of the Space-Charge-Limited Load (SCLL) to create large resistance values in small areas and study the sensitivity of such resistances to processing parameters,
2. develop a triple diffused structure process with a polysilicon emitter,and
3. fabricate NPN bipolar transistors with SIT and PNP clamps to verify simulated performance predictions.

REFERENCES

[1.1] P.M. Solomon, "A Comparison of Semiconductor Devices for High-speed Logic", Proc. IEEE, vol. 70, no. 5, pp. 489-509, May 1982.

[1.2] A. Reisman, "Device, Circuit, and Technology Scaling to Micron and Submicron Dimensions", Proc. IEEE, vol. 71, no. 5, pp. 550-565, May 1983.

[1.3] S. A. Evans et al, "A lum Bipolar VLSI Technology", IEEE Trans. Electron Devices, vol. ED-27, no. 7, pp. 1373-1379, July 1980.

[1.4] J. Lohstroh, R.M. Pluta, "Propagation Deley Times of ISL and STL", IEEE Journal of Solid-State Circuits, vol. SC-17, no. 4, pp. 687-695, August 1982.

[1.5] J. Nishizawa, T. Terasaki, J. Shibata, "Field-effect Transistors versus Analog Transistor (Static Induction Transistor)", IEEE Trans. Electron Devices, vol. ED-22. no. 4, pp. 185- 197, April 1975.

[1.6] B.M. Wilamowski, R.C. Jaeger, "The Lateral Punch-through Transistor", IEEE Electron Devices Letters, vol. EDL-3, no. 10, pp.271-280, October 1982.

[1.7] P. Plotka, B.M. Wilamowski, "Temperature Properties of a Static Induction Transistor", Solid State Electronics, vol.24, pp. 105-107, February 1981.

[1.8] L.W. Nagel, "SPICE2: A Computer Simulation Program to Simulate Semiconductor Circuits", University of California, Berkeley, Memo ERL-M520, May 1975.

[1.9] P. Plotka, B.M. Wilamowski, "Interpretation of Exponential Type Drain Characteristics of the Static Induction Transistor", Solid-State Electronics, vol. 23, no. 7, pp. 693-694, July 1980.

[1.10] J.M.C. Stork, J.D. Plummer, "Small Geometry Depletion Base Bipolar Transistors (BSIT) - VLSI Devices ?", IEEE Trans. Electron Devices, vol. ED-28, no.11, pp.1354-1363, November 1981.

[1.11] O. Ozawa, "Electrical Properties of a Triode-like Silicon Vertical-channel JFET", IEEE Trans. Electron Devices, vol.ED-27, pp. 2115-2123, November 1980.

[1.12] M. I. Elmasry, "Digital Bipolar Integrated Circuits", Wiley, NY, 1983.

[2.1] N. F. Mott, R. W. Gurney, "Electronic Process in Ionic Crystals", 2nd ed., Oxford: Clarendon Press, 1940.

[2.2] W. Shockley, U.S. Patent No. 2790037, March 14, 1952.

[2.3] S. Teszner, R. Gicquel, Proc. IEEE, vol. 52, pp. 1502- , 1964.

[2.4] P. Richman, "Modulation of space-charge limited current flow in insulated-gate field effect tetrode", IEEE Trans. Electron Devices, vol. ED-16, no. 9, pp. 759-766, September 1969.

[2.5] J. Nishizawa, T. Terasaki, J. Shibata, "Field-effect transistor versus analog transistor (static induction transistor)", IEEE Trans. Electron Devices, vol. ED-22, no. 4, pp. 1885-197, April 1975.

[2.6] T. Ohmi, "Punching through devices and its integration - static induction transistor", IEEE Trans. Electron Devices, vol. ED-27, no. 3, pp. 536-545, March 1980.

[2.7] B. M. Wilamowski, R. Jaeger, "The lateral punch-through transistor", Electron Device Letters, vol. EDL-3, no. 10, pp. 277-280, October 1982.

[2.8] Y. Mochida, J. Nishizawa, T. Ohmi, R. K. Gupta, "Characteristics of static induction transistors: effects of series resistance", IEEE Trans. Electron Devices, vol. ED-25, no. 7, pp. 761-767, July 1978.

[2.9] R. Ratnam, A. B. Battacharyya, "Accumulation punch-through mode of operation of buried-channel MOSFET°S", Electron Device Letters, vol. ED-3, no. 7, pp. 203-204, July 1982.

[2.10] C. Kim, E. S. Yans, "Carrier accumulation and space-charge limited current flow in field effect transistors", Solid State Electronics, vol. 13, pp. 1577-1589, 1970.

[3.1] W. L. Engl, H. K. Dirks, B. Meinerzhagen, "Device Modeling", Proc. of the IEEE, vol. 71, pp. 10-33, January 1983.

[3.2] S.R. Nassif, A.J. Strojwas, S.W. Director, "FABRICS II: A Statistically Based IC Fabrication Process Simulator", Research Report No. CMUCAD-83-16, Carnegie-Mellon University, October 1983.

[3.3] D.A. Antoniadis, S.E. Hansen, R.W. Dutton, "SUPREM II - A Program for IC Process Modeling and Simulation", Technical Report 5019-2, Stanford Electronics Laboratories, June 1978.

[3.4] S. M. Sze, "Physics of Semiconductor Devices", Wiley, NY, 1981.

[4.1] S. Mastroianni, Personal Communication.

[4.2] Lazaro Hong, "Evaluation of the Technics Planar Etch-II Plasma System", I.C.E. Corporation Report 11-789.

[4.3] S. M. Sze, "VLSI Technology", pp. 453-454, McGraw Hill, NY, 1983.

[4.4] B. M. Wilamowski, R. C. Jaeger, "The Lateral Punch-Through Transistor", IEEE Electron Device Letters, Vol. EDL-3, No. 10, October 1982.