The Lateral Punch-Through Transistor

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Abstract—**Operation of a diffused-gate, lateral punch through transistor has been demonstrated. Operation is similar to the static induction transistor, and the device can be used in planar integrated circuits. Current flow in this lateral device obeys the space charge limited conduction law over a wide range of currents, and the drain current exhibits a negative temperature coefficient.**

INTRODUCTION

SEMICONDUCTOR devices with either carrier injection over a potential barrier, or space charge limited current flow have unique properties. Carrier transit times are very small, and frequency of operation is high. These devices are very resistant to thermal breakdown because of negative temperature feedback at high current levels. The drain current can be controlled by both gate and drain voltage. One such device is the lateral punch-through transistor. Its operating mechanism is very similar to Nishizawa's SIT transistor [1] and its characteristics are similar to those obtained by Mochida et.al. for the vertical SIT [2]. They are also similar to those obtained by Richman in his MOS space charge controled devices on very high (40,000 ohm·cm) resistivity substrates [3]. The lateral construction described here has a much simpler fabrication process than any of the vertical structures [4]. The current in this lateral device obeys the space charge conduction law over a wide range of currents because of the relatively large spacing between source and drain.

DEVICE STRUCTURE

The device structure is shown in Fig. 1. The substrate is shorted to the gate. A positive voltage on the gate and negative voltage on the drain depletes all of the region surrounding the device. Therefore, the potential distribution in this region can be easily controlled by the applied terminal voltages. In order to obtain the same current with a higher gate voltage, the magnitude of the drain voltage has to be significantly higher. For very low current levels, carriers are injected from the source through a potential barrier, which is controlled by the gate and drain potentials. The mechanism and relationships are very similar to those described in [5] and [6]. For moderate to high current levels, the current flow becomes space charge limited. An increase in drain voltage causes larger current flow, and larger space charge, which neutralizes the effect of drain voltage on the potential barrier height.

Manuscript received April 16, 1982, revised July 28, 1982.

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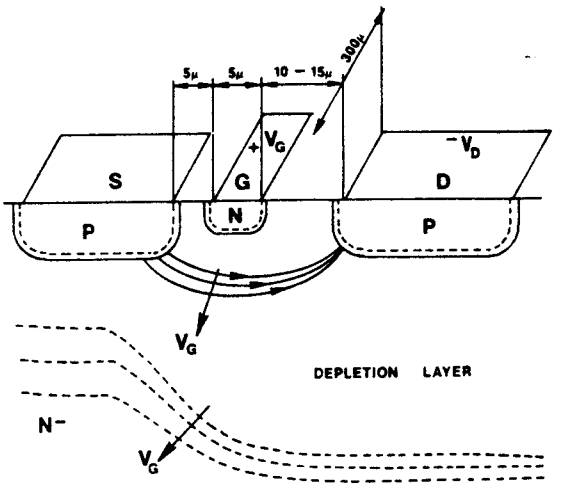

Fig. 1. Device structure.

SPACE CHARGE CONDUCTION LAW

The carriers injected from the source through the potential barrier drift toward the drain with limited velocity. These carriers create the space charge between the potential barrier and drain. Exact analysis of this two-dimensional structure is very difficult. However, some useful results can be obtained using an approximate one-dimensional approach along the carrier path. The analysis assumes that the carriers tend to flow in a potential trough from source to drain. In this trough, the transverse field is much smaller than the field in the direction of carrier motion—otherwise the carriers would disperse.

To calculate the voltage drop on the space charge, Poisson's equation must be solved along the current path:

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\epsilon\epsilon_0} \tag{1}$$

where the charge density $\rho(x)$ is:

$$\rho(x)\frac{Q}{\Delta x} = \frac{I_D\tau}{\Delta x} = \frac{J}{v(x)} \tag{2}$$

Carrier velocity $v(x)$ for small and moderate electrical fields is:

$$v(x) = \mu E(x) \tag{3}$$

For the case of large electrical fields, carrier velocity is constant and equal to v_s the saturation velocity.

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Solving (1) for small and moderate electrical fields (boundary conditions: $E = 0$, $V = 0$ at $x = 0$) yields:

$$I_D = \frac{9}{8} V_D^2 \mu \epsilon \epsilon_0 \frac{A}{L^3} \tag{4}$$

$$r_D = \frac{dV_D}{dI_D} = \frac{4}{9 V_D \mu \epsilon \epsilon_0} \frac{L^3}{A} = \frac{V_D}{2 I_D} \tag{5}$$

$$\tau = \frac{4}{3} \frac{L^2}{V_D \mu} \tag{6}$$

where V_D, I_D are the drain voltage and currents, A is the device cross-sectional area, τ is the transit time for carriers, and L is the spacing between the potential barrier and drain. In a similar way, for large electrical fields:

$$I_D = 2 V_D \epsilon \epsilon_0 v_s \frac{A}{L^2} \tag{7}$$

$$r_D = \frac{dV_D}{dI_D} = \frac{1}{2 \epsilon \epsilon_0 v_s} \frac{L^2}{A} = \frac{V_D}{I_D} \tag{8}$$

$$\tau = \frac{L}{v_s} \tag{9}$$

The detailed solutions yielding (4) and (7) are described in [7] and [8].

Experimental

Two devices with different geometries were fabricated using standard 5 μm process with spacing between source and drain equal to 20 and 25 μm. To obtain punch-through current between source and drain, high resistivity (600 ohm·cm), n-type substrates were chosen. The p-type diffused layer had a sheet resistance of approximately 100 ohm/□ and a junction depth of 4.5 μm. The n-type diffused layer had a sheet resistance of 6 ohms/□ and a depth of 1.8 μm.

The current-voltage (I-V) characteristics drawn for two different temperatures are shown in Fig. 2. The transistor characteristics are presented in Fig. 3 for a wide range of currents using a semi-log scale. In Fig. 4, the same characteristics are drawn with a log-log scale. The I-V drain characteristics follow the square law, and these measurements demonstrate that the space charge conduction law is valid for a very wide current range of 1 μA to 1 mA. The voltage amplification factor m as a function of gate voltage V_G is presented in Fig. 5.

Device Modeling

Introduction of the diffused gate electrode allows control of the space charge limited current flowing from source to drain. The voltage amplification factor m for the gate depends on the transistor geometry, and varies very slightly with the transistor biasing point. Therefore the drain current of the device for various gate biasing can be described by the following

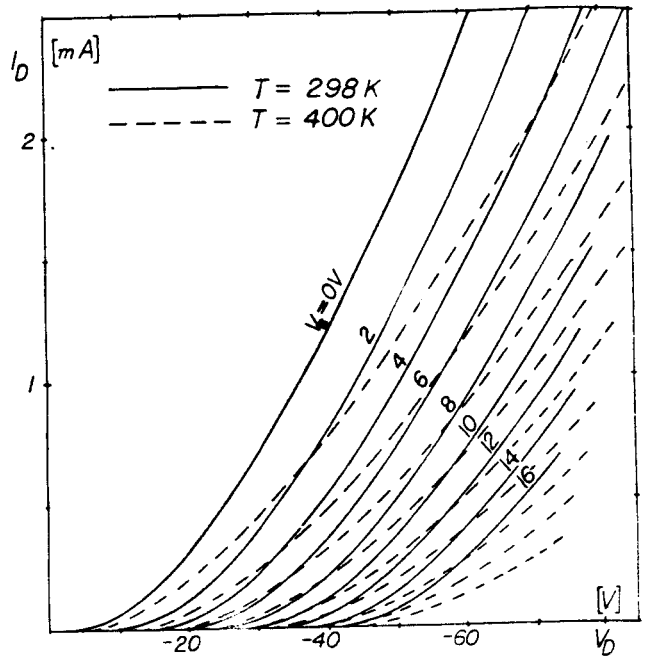

Fig. 2. Drain characteristics of device with 20 μm spacing between source and drain for two different temperatures.

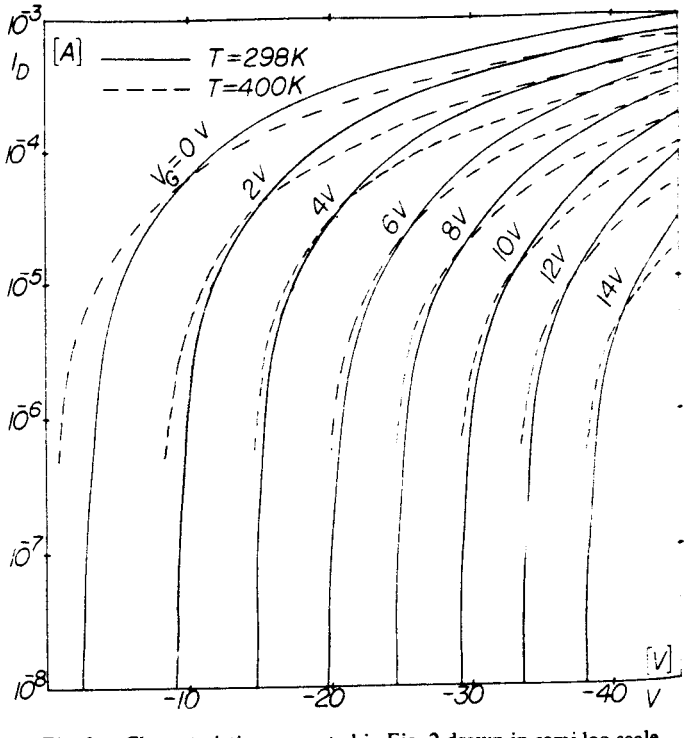

Fig. 3. Characteristics presented in Fig. 2 drawn in semi-log scale.

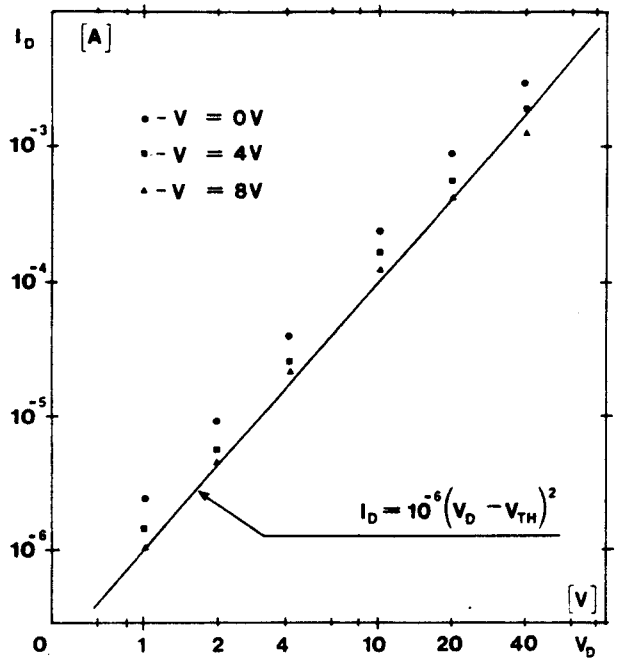

Fig. 4. Drain characteristics of device with 20 μm spacing between source and drain with a log-log scale.

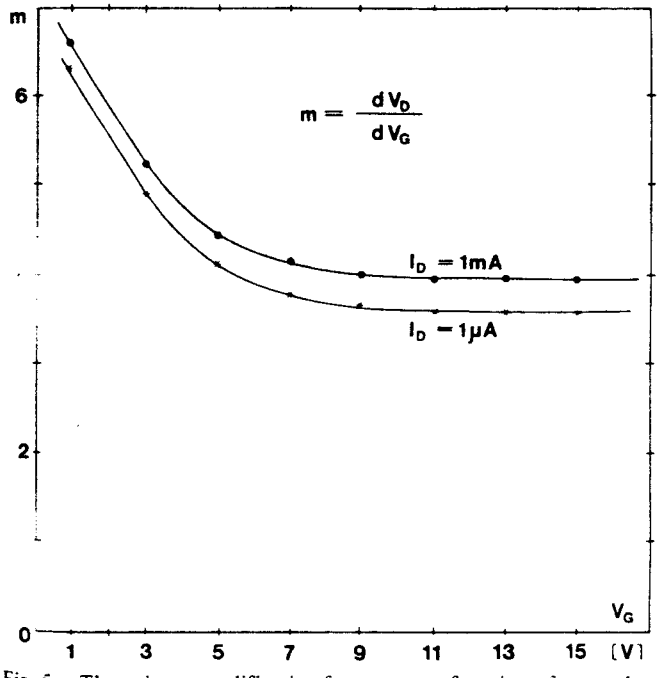

Fig. 5. The voltage amplification factor m as a function of gate voltage V_G for two values of drain currents.

phenomenological relationship:

$$I_D = \frac{9}{8}\mu\epsilon\epsilon_0 \frac{A}{L^3}(V_D - mV_G - V_0)^2 \tag{10}$$

where V_0 is the voltage required to achieve punch through. It can be estimated using a one-dimensional approximation:

$$V_0 = \frac{qNL^2}{2\epsilon\epsilon_0} - V_{bi} \tag{11}$$

where V_{bi} is the built-in drain-to-source potential. Using (10), g_m can be expressed by:

$$g_m = \frac{dI_G}{dV_G} = m\sqrt{\frac{9}{2}\mu\epsilon\epsilon_0 \frac{A}{L^3} I_D}$$

$$= \frac{2I_D}{(V_D - V_0)/m - V_G} \tag{12}$$

For a device with $L = 20$ μm and $A = 2000$ μm^2:

$$g_m = 0.003\sqrt{I_D}\ [A/V] \tag{13}$$

Also, using (6) the carrier transit time can be estimated to be 0.5 ns for $V_D = 20$ V. For other drain voltages:

$$\tau = \frac{10.66[\text{ns} \cdot \text{V}]}{V_D} \tag{14}$$

These are very small values if we remember that the source-drain spacing is of the order 20 μm. By scaling down dimensions, future improvement of transit time can be expected. However, the lower limit is given by (9). For the fabricated devices assuming constant $L = 20$ μm, and $V_0 = 2.25$ V, the effective areas of the device can be obtained: $A = 3350$, 2000, and 1350 μm^2 for V_G equal to 0, 4, and 8 V respectively. The influence of gate voltage on effective channel area can be qualitatively explained. A higher gate voltage forces the carrier path farther from the gate, and the path length L becomes longer (Fig. 1). At same time, the potential distribution becomes steeper and the carrier path is narrowed. These two-dimensional effects can be modeled by introducing $A/L^3 = F(V_G)$.

Conclusion

Lateral punch-through device operation has been demonstrated. The large spacing between source and drain, of the order of 20 μm, results in a relatively small electric field in the channel even for high drain voltages, and the device characteristics follow the space charge conduction square law over a very wide current range. This device may find application in fast analog circuits for multiplication, squaring and root calculation. Scaling will lead to smaller biasing voltages and higher speed. Since the region surrounding source, drain and gate is depleted of carriers, the parasitic capacitances are very small. This property is promising for future applications in fast digital circuits. However it will require special circuit design similar to that of GaAs logic due to the opposite biasing of gate and drain.

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