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Lateral base transistor logic for I^2L.

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Up to now the best τxP product in I^2L family has been obtained in SIT Logic technique. The published results using standard 5 μm photolitography process is 0.002 pJ /1/ /2/. The structure of SITL gate is presented in fig. 1. In this logic the carriers are injected through the potential barrier which is induced in the epi-layer between two p-regions by built-in field of the p-n junction. SITL gates can operate only if separation of the p - type region is below 3 μm and impurity doping level of the epi--layer is below $10^{14}cm^{-3}$. This paper shows that similar results can be obtained using the lateral base transistor /LBT/ /3/ logic fig 2. In this case high gain of the npn transistor is possible due to very low doping level in the lateral diffused base and because the built-in field in the base region, which hampers the carrier flow, practically does not exist. The LBT logic can operate both with low and high doping levels of epi-layer.

For preparation of the sample, standard bipolar technology was used. Only the doping level of the epi-layer was varried. In case of $N_{epi}=5\cdot10^{13}cm^{-3}$, th τxP product of 0.090 pJ for $I_D < 0.1$ μA was obtained and τ_{min} for $I_D=250$ μA was 25 ns. This logic could operate even if the doping level of the epi--layer was changed to the value of $8\cdot10^{15}cm^{-3}$. In this case τxP=0.15 pJ for $I_D < 1{,}0$ μA and $\tau_{min}=20$ ns. The results are presented in fig 3. In conlusion one can find that the results in LBT logic are almost as good as in SIT logic with the technological process relatively simple.

References

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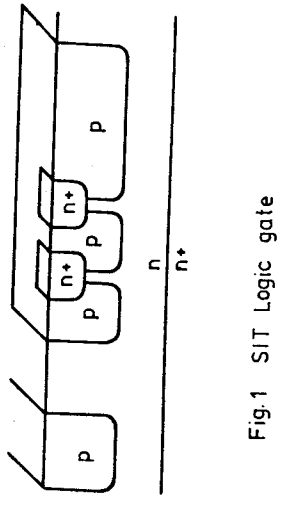

Fig.1 SIT Logic gate

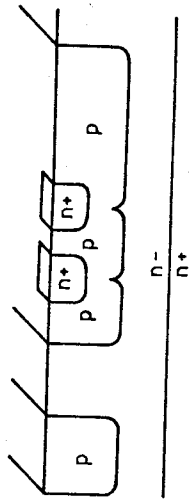

Fig.2 LBT Logic gate

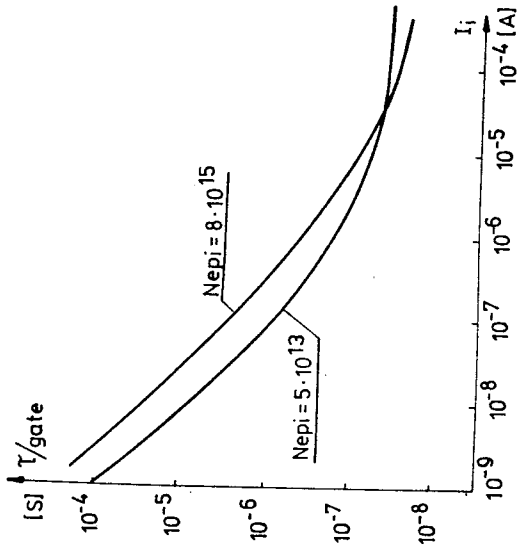

Fig.3 Delay time as a function of injector current