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ON THE DYNAMIC PROPERTIES OF SITL INVERTER

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SUMMARY

ANALYSIS of the dynamic behaviour of SITL (Static Induction Transistor Logic) circuit and a new I²L structure (I²LBL) is performed. Design details and measured data of fabricated structures are also given. The real parameters of the structures agree well with the proposed physical model. A simple method of manufacturing I²L structures is presented.

1. INTRODUCTION

THE FIELD EFFECT TRANSISTORS with triode-like characteristics shown in Fig. 1 are used in integrated injection logic (I²L) [1]. These transistors are characterized by fully depleted channel by means of build-in voltage of the gate-channel junction. Positive biasing of the gate with respect to the source decreases potential barrier and causes flow of the appriopriate *p-n-p* injector current to the ground. At this moment the holes are injected to the channel, drain and source.

Propagation delay of the SITL inverter definied as switch-off time of the junction FET was calculated from equation $\tau = Q/2I_0$, where Q is the sum of the excess holes charge and increase of the barrier layer charge and I_0 is the mean injector current. For the sake of determining the charge Q analysis of the charge distribution in the barrier layers of the junctions and quasi-neutral regions was carried out. Because of low doping density in the channel (10^{14} cm^{-3} and lower) analysis was done for high injection level.

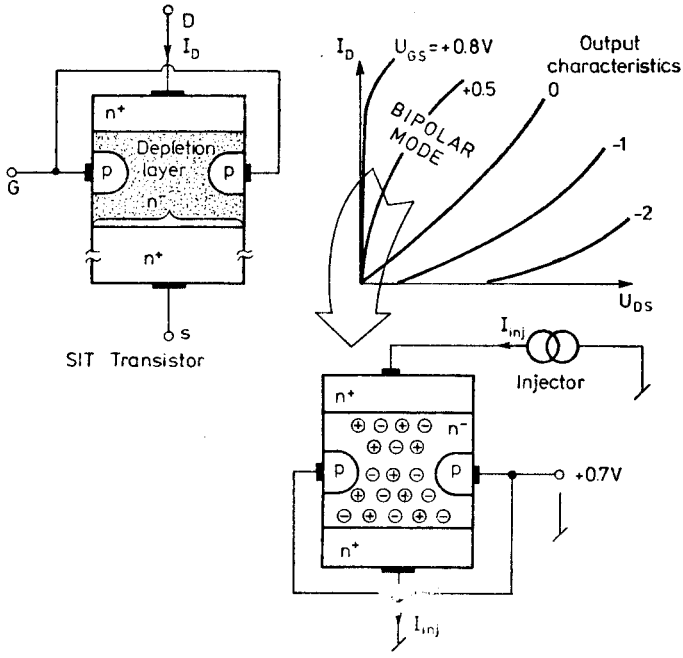

FIG. 1. Transistor SIT at bipolar mode.

2. ANALYSIS

Figure 2a shows circuit diagram of the SITL inverter. Integrated form of the inverter is shown in Fig. 2b and 2c. In the analysis of the SITL inverter, the structure is partitioned into two regions, shown in Fig. 3. The doping profile along section AA' (Fig. 3) is shown in Fig. 4.

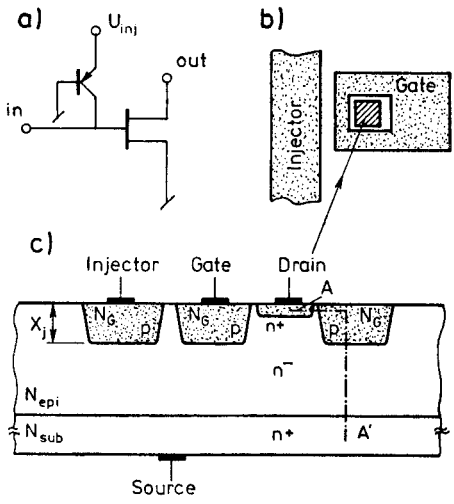

FIG. 2. SITL (I^2LBL) inverter: a) diagram, b) topology, c) design.

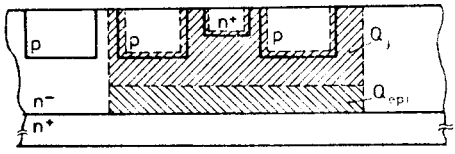

FIG. 3. Junction and epiregion charge.

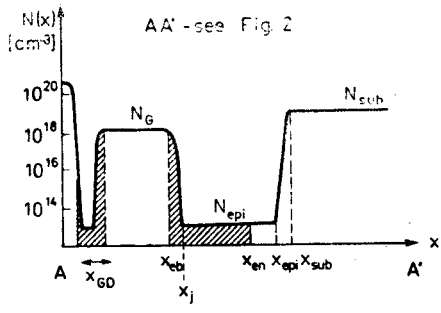

FIG. 4. Doping profile.

2.1. PROPAGATION DELAY OF THE INVERTER

The charge of the excess minority carriers in epiregion of the source is determined under assumption of one-dimensional current flow and quasi-charge neutrality in the epiregion. If the electron current is greater than the hole current the electric field in the epiregion can be described by relation

$$E = \frac{D_p \frac{dn}{dx}}{\mu_p n - N_{epi}}, \tag{1}$$

where D_p is holes diffusion coefficient, μ_p is holes mobility, n is electron concentration and N_{epi} is doping concentration in the epiregion.

One can determine electron distribution $n(x)$ from eq. (1) and from the expression for the electron current density J_n. Hence, the condition $J_n = \text{const}$ leads to electron profile in the epiregion [2]

$$2n(x) - n(x_{en}) + N_{epi} \ln \frac{n(x) - N_{epi}}{n(x_{en}) - N_{epi}} = J_n \frac{x - x_{en}}{q D_n}, \tag{2}$$

where N_{epi} is doping concentration in the epiregion, J_n is current density in the channel and

$$n(x_{en}) = N_{epi} + N_G \exp(-\psi/U_T)\,[1 - \exp(-2\psi/U_T)], \tag{3}$$

where N_G is average doping concentration in the gate region, $U_T = kT/q$ and

$$\psi = \frac{q}{\varepsilon\varepsilon_0} \int_{x_{eb}}^{x_{en}} x\, N(x) dx. \tag{4}$$

The hole doping profile is given by

$$p(x)=n(x)-N_{\mathrm{epi}}\cong n(x). \tag{5}$$

The terminal voltage V_{GS} is sum of the gate-source junction voltage U_{jGS}, voltage drop across the epilayer U_{EN} and voltage drop across the junction n-n^+ ($U_{nn}{}^+$)

$$U_{GS}=U_{jGS}+U_{EN}+U_{nn}{}^+. \tag{6}$$

The voltage applied to the depletion region of the junction U_{jGS} can be described by relation

$$U_{jGS}=U_T \ln \frac{N_G N_{\mathrm{epi}}}{n_i{}^2}-\psi. \tag{7}$$

Integrating relation (1) one can obtain the voltage drop across the epilayer

$$U_{EN}=U_T \ln\left[1+\frac{n(E_{\mathrm{epi}})-n(x_{en})}{n(x_{en})-N_{\mathrm{epi}}}\right]. \tag{8}$$

The voltage drop across the n-n^+ junction equals [4]

$$U_{nn}{}^+=U_T \ln \frac{N_{\mathrm{sub}}\, p(x)_{\mathrm{sub}}}{N_{\mathrm{epi}}\, p(x_{\mathrm{epi}})}, \tag{9}$$

where

$$p(x_{\mathrm{sub}})=p(x_{\mathrm{epi}})\left[1+\frac{p(x_{\mathrm{epi}})}{N_{\mathrm{epi}}}\right]\frac{N_{\mathrm{epi}}}{N_{\mathrm{sub}}}. \tag{10}$$

From above expressions one can determine the hole profile in the epiregion for a given U_{GS} and J_n. The change of the holes charge density in the epiregion during inverter switching is described by

$$\Delta Q_{\mathrm{epi}}=q\left(\int_{x_{en}}^{x_{\mathrm{epi}}} p(x)dx-\int_{x_{en}}^{x_{\mathrm{epi}}} p_0(x)dx\right)\cong q\int_{x_{en}}^{x_{\mathrm{epi}}} p(x)dx, \tag{11}$$

where $p(x)$ denotes holes density in transistor during conduction of current I_n (on-state) and $p_0(x)$ denotes holes density in cut-off transistor (off-state).

The second region of interest is depletion layer of the junction. The change of the charge density of jonized impurities during inverter switching is given by

$$\Delta Q_j=\left(\int_{V_{GS_1}}^{V_{GS_2}} C_{GS}\, dV_{GS}+\int_{V_{GD_1}}^{V_{GD_2}} C_{GD}\, dU_{GD}\right)U_{inj}, \tag{12}$$

where C_{GS} and C_{GD} are barrier capacitances of gate-source and gate--drain junctions respectively and U_{inj} is inverter supply voltage.

The capacitances per unit area of the junction are described by

$$C_{GS}=\frac{\varepsilon_0\,\varepsilon}{x_{\mathrm{epi}}-x_j}, \tag{13}$$

$$C_{GD}=\frac{\varepsilon_0\,\varepsilon}{x_{GD}}, \tag{14}$$

where x_{GD} is width of depletion layer of the gate-drain junction. Inverter delay was calculated from equation

$$\tau=\frac{\Delta Q_{\mathrm{epi}}+\Delta Q_j}{J_n}. \tag{15}$$

The charge in other regions was neglected for reasons presented later.

2.2. $P\cdot\tau$ PRODUCT

The speed-power product $P\tau$ of the SITL inverter for small current density is constant and given by relation

$$P\tau=\left(A_{GS}\int_{U_{GS_1}}^{U_{GS_2}} C_{GS}\,dU+A_{GD}\int_{U_{GD_1}}^{U_{GD_2}} C_{GD}\,dU\right)U_{inj}^2, \tag{16}$$

where A_{GS} is inverter gate area and A_{GD} is drain side area.

3. CALCULATION RESULTS AND EXPERIMENTAL DATA

In the experimental part of the work SITL inverters were fabricated. A ring oscillator has nine stages and a buffer was designed on a chip. The eight oscallator stages consist of single output inverters, the nineth is a dual output gate; buffer is made of additional I²L inevrter. A single test inverter is also located on the chip.

Topology of a single inverter of the ring oscillator is shown in Fig. 5. A *n-p-n* transistor area on a mask is 40×45 μm, drain area is 15×30 μm. A contact window area of the gate and drain is 5×20 μm. The gate of the SITL transistor is diffused into 40×45 μm area, except of 7.5×30 μm strip masked by oxide. The field effect transistor SIT channel is formed under this strip. The next step is drain diffusion in the place where gate diffussion does ont take place (only latteral diffusion); in the same time a shallow n^+ ring is diffused between gates of the SIT transistors.

Structures were fabricated on silicon water with epilayer of thickness $W_{\mathrm{epi}}=4-5$ μm and $N_{\mathrm{epi}}=10^{14}$ cm^{-3}; substrate doping concentration $N_{\mathrm{sub}}=3\cdot10^{18}$ cm^{-3}. The gate and drain diffusion were performed to the depth $x_j=2.5$ μm and $R_s=120$ Ω/sq, respectively.

It should be noted that by using mask with narrower strip masking channel of the SIT transistor (strip width 5 μm instead of 7.5 μm) during

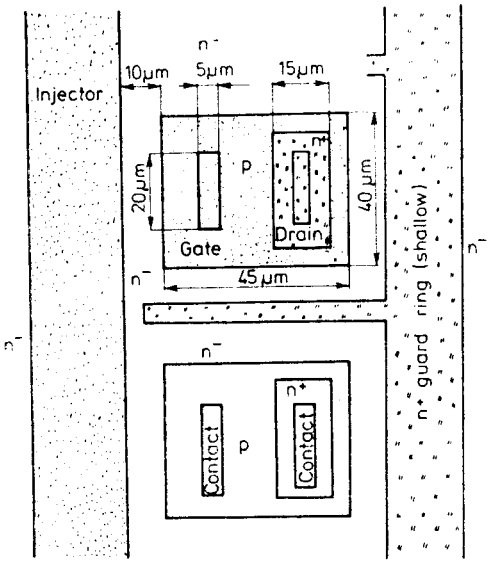

FIG. 5. Topology of single inverter in the ring oscillator.

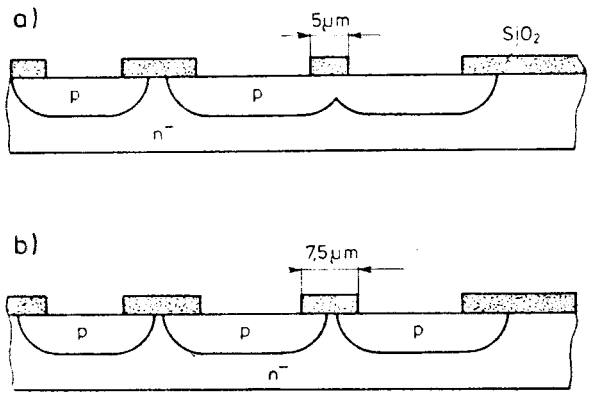

FIG. 6. Differences between SITL and I²BL: a) — base of the *n-p-n* transistor, b — gate and channel of the SIT transistor. Notice: both diffused regions were obtained in the same process.

gate diffusion, one can obtain simple *n-p-n* bipolar transistor, Fig. 6 (known as Base Lateral) and a new type of I²L device (called I²BL by the authors). Operation theory of the SITL gate described above applies to the I²LBL as well.

Fig. 7 shows propagation delay of the inverter versus drain current I_D (measured values).

Propagation delay depends mainly on the barrier capacitances of the junctions for the small current densities like in the case of simple I²L inverters. For the high current density propagation delay is inde-

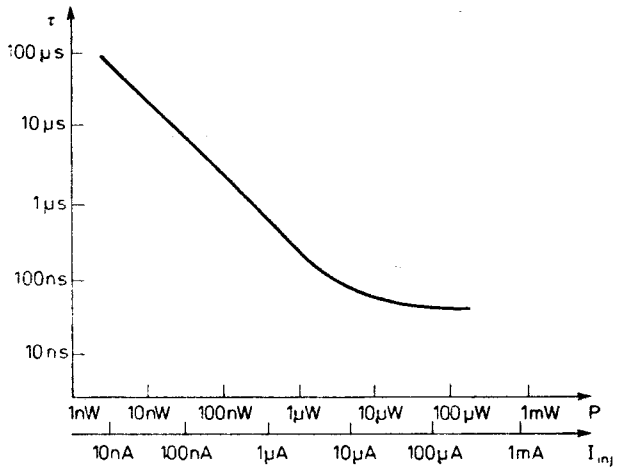

FIG. 7. Propagation delay τ of the inverter versus dissipated power P, and injector current I_{inj}.

pendent on barrier capacitance but relates to charge of holes accumulated in the epilayer. The measured value of the SITL inverter minimum propagation delay is

$$\tau_{\min}=45\ \mu\text{s} \quad \text{for} \quad I_D=100\ \mu\text{A}.$$

Value calculated from equation (15) is

$$\tau_{\min}=50\ \mu\text{s}.$$

Fig. 7 shows dependence of the $P\tau$ product on drain current I_D. The measured minimum value of the product $P\tau$ is

$$P\tau_{\min} \leqslant 0.15\ \text{pJ} \quad \text{for} \quad I_D < 0.1\ \mu\text{A}.$$

Value calculated from relation (16)

$$P\tau_{\min}=0.1\ \text{pJ}.$$

Very small value of the $P\tau$ product in the SITL inverter is caused by small doping density N_{epi} in the epiregion. The calculated values agree well with measured ones and confirm neglecting the holes accumulated in the remaining regions of the inverter during analysis. This result is typical for the common I^2L circuits [5].

4. CONCLUSIONS

Detailed charge analysis of the SITL inverter during switching was carried out. The propagation delay and minimum value of $P\tau$ was determined. Accumulation of the minority carriers in the gate, substrate, base of the n-p-n transistor and especially in the junction field effect

transistor channel has no influence on the analysis is investigated inverter design. One can use results of the analysis in designing SITL circuits. A new idea of the I^2L circuits was also presented.

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STRESZCZENIE

WŁAŚCIWOŚCI DYNAMICZNE INWERTERA SITL

W pracy przedstawiono analizę dynamicznych właściwości układów SITL i nowej konstrukcji układów I^2L (I^2LBL.) Przedstawiono konstrukcję i dane doświadczalne wykonanych układów. Uzyskano dużą zgodość zaproponowanego modelu fizycznego z rzeczywistymi właściwościami układów. Wykazano możliwość prostego wykonania układów I^2L.

РЕЗЮМЕ

ДИНАМИЧЕСКИЕ СВОЙСТВА ИНВЕРТОРА SITL

В работе представлен анализ динамических свойств схем SITL и новой конструкции схем I^2L (I^2LBL). Представлены конструкция и экспериментальные данные сделанных схем. Получено большое согласие предложенной физической модели с реальными свойствами схем. Представлен тоже несложной способ построения схем I^2L.