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The bipolar nonsaturating logical gate with short propagation delay and high packing density

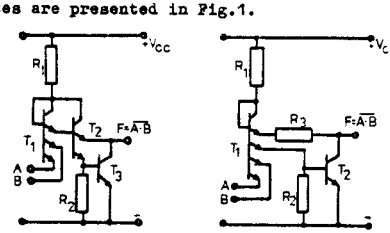
1. Introduction

The recent advances in the field of silicon IC's technology stimulates a very fast development of digital circuits. In the past decade some new bipolar logic families /I^2L Berger,H./1/, SITL Nishizawa,J./2/, CHL Lehning,H./3/ / were introduced and a number of the new versions of well known circuits /T^2L ECL,DTL/ were proposed. The potential properties of the new logics are usually demonstrated on simple logical gates. They are commonly described by following circuit-parameters: minimum propagation delay /$t_{pd\ min}$/,speed-power product /t_{pd}*P/,packing density,noise margins,fan-out,compatibility with other logic families and costs. From the viewpoint of the system flexibility the possibility of manufacturing of analog and digital circuits on the same chip /by means of the same technological process/ is required.

Taking into account the parameters of the existing gates one can conclude that each gate offers some satisfactory properties but suffers from the deficiency of another ones. For example: I^2L perfectly satisfies the requirements of high packing density and very low power dissipation but it is lacking in speed. On the contrary ECL is excellent candidate for fast systems but it consumes much more power. From the above brief considerations it is seen the evident need to develope a gate that would present some compromise between most essential parameters of logical gates. It is the purpose of this paper to propose one of the possible approaches to this problem.

2. The bipolar nonsaturating logic concept

The circuit diagrams of the developed gates are presented in Fig.1.



a/ b/

Fig.1

In order to ensure the possibility of the simultaneous realization of analog and digital circuits and low costs,the well-established standard silicon IC technology without gold doping and without Schottky contacts was adopted. In the case of the non-gold doped digital circuits it is necessary to prevent all transistors of the gate from entering the saturation region because of two undesirable effects: 1.the storage time during turn-off transient of transistors arises and strongly affects the total propagation delay and 2.the parasitic substrate pnp transistors become active. Assuming non-gold process one has to avcid also the use of conventional multiemitter transistor input circuit. For that reason another arrangement of multiemitter transistor was applied.

26. Intern.Wiss.Koll. TH Ilmenau 1981
Vortragsreihe
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In order to protect the output transistor from saturation in the low state two possible solutions were considered. In the gate in Fig.1 a/ two-emitter transistor clamping technique was adopted. The collector-emitter voltage of T_3 cannot be lower than V_{BE} on approximately. In the case shown in Fig.1 b/ the resistor R_3 controlls the degree of saturation of T_2 and the output voltage is normally held at about 300mV.

It was assumed that by protecting all transistors from saturation and by decreasing the area occupied by the gate the high speed, high packing density and low cost logic can be obtained.

3. The experimental results

In order to verify the foregoing assumptions the hybrid five-stages ring oscillator composed of the integrated transistors array UL 1111 /Fairchild-CA 3046/ and the discrete resistors was investigated. At first, the very important characteristic i.e. propagation delay versus power dissipation of the gate shown in Fig.1 a/ was measured. The supply voltage was kept at 5 V. The resistors R_1 were replaced by the controlled current mirrors built of discrete pnp transistors and the resistors R_2 were omitted. The results obtained are presented in Fig.2 and one can determine minimum propagation delay $t_{pd\ min}$= 15 ns and speed-power product $t_{pd} \cdot \bar{P}$ =37 pJ.

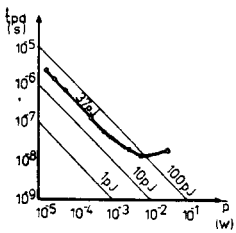

Fig.2

The next step was the optimization of the construction in order to improve the speed of the gate. In this case both resistors R_1 and R_2 were replaced by the controlled current mirrors and minimum propagation delay $t_{pd\ min}$=6 ns at $\bar{P}$=9 mW was achieved. Finally the optimal resistor values R_1=1.6 k and R_2=2.3 k were found.

In order to evaluate the packing density attainable in the fully integrated version it is necessary to inspect the topological layout of the gate drawn in Fig.3. Assuming typical dimensions indicated in this figure one can calculate the actual area of the gate A=1.9 $10^4\ \mu m^2$. It is seen that the packing density greater than 50 gates per mm^2 can be easily obtained.

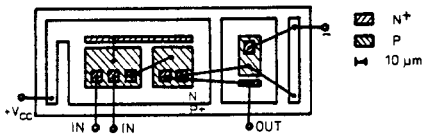

Fig.3

4. The computer simulations results

The results presented above promise to achieve the desirable properties in the integrated version. To verify this conclusion the sequence of the computer simulations was performed. The transient analysis of transistor circuits program TRAN for computer ODRA 1305 was used. The Ebers-Moll model of transistor including diffusion capacitances and junction capacitances and spread-base resistance was adopted. The parameters of the model were identified from the simple measurment procedure.

The chain of gates excited by the voltage step function was stimulated. The idealized waveforms obtained are shown in Fig.4. The average propagation delay contributed by each gate was then determined.

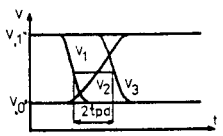

Fig.4

In the case of the simulation of hybrid version the computed and measured results were insatisfactory agreement. Subsequently the influence of various transistor parameters on propagation delay of the gate was investigated. It appeared that the junction capacitances, especially parasitic collector-substrate capacitance, are the speed-limiting factors of the gate. However, it is expected that these capacitances should be significantly decreased in the integrated version. It is mainly due to use of the common isolation island for T_1 and T_2, further reduction of dimensions within the standard technology and also the elimination of the large parasitics resulted

from the hybrid construction of the circuit. The simulation of the integrated gate including most essential parasitics confirmed that the propagation delay t_{pd} = 1.8 ns is feasible.

5.The summary

The high speed,high packing density,facility of manufacturing analog circuits on the same chip and low costs are the main advantages offered by the bipolar NAND gate presented here. The rather low logic swing /about 1 V/,low noise-margins are the apparent drawbacks resulted from relatively high value of the output voltage in the „0"state /about 0.7/ It is expected that these inconveniences can be overcome in the circuit shown in Fig.1 b/, that will be further investigated.

Taking into account the results reported in this paper it was concluded that the work on this topic should be continued. The development of various modifications of the basic circuit and the integration procedure is under way.

6.References

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