SESSION XVIII: ADVANCED TECHNOLOGY

FAM 18.3: Integrated Logic – Static Induction Transistor Logic

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SOLID-STATE CIRCUITS are designed to minimize both delay time and operational power. The product of these is thought to be constant, represented by a specific figure for each type of integrated circuit. The I^2L structure has been shown to operate with the lowest switching energy[1]. The power efficiency of the Vertical Injection Logic (VIL) structure shows a further improvement, by a factor of two. However, its fabrication requires the use of 7-8 masks[2]. A new logic circuit structure is proposed – Static Induction Transistor Logic (SITL) – utilizing the static induction transistor (SIT)[3]. This logic circuit permits a further reduction in the power-delay time product (theoretically 6×10^{-3} and experimentally, one order of magnitude). In the case of I^2L, it is made by a 3 or 4-mask technology. The packing density can be as high as 1000 gates/cm^2.

In this logic structure, the SITs are used as the output transistors and the lateral bipolar PNP transistor is used as the injector, as usual, as shown in Figure 1. The SIT consists of N^+ drains on the top surface of the N^- epitaxial layer, a P^+ gate configured on both sides of the drain on the same surface and the space charge layer formed surrounding the drain regions, N^- channels penetrating the gate region below the drains and the N^+ source substrate. The channels are about 2~3 μm in diameter and are formed by lateral P-type diffusion.

The fabrication process in this case is as follows. The N^- epitaxial layer is grown on the N^+ substrate, having a carrier concentration of $2\sim3 \times 10^{13}$ cm^{-3} and a thickness of 4~5 μm. After oxidation and photolithography, B-diffused layers were formed as the gate regions of the SIT and the emitter of the injector (the lateral transistor), followed by the second oxidation. Then, the N^+ -diffusion layers are formed as drain regions, followed by the opening of contact holes in the SiO_2 film, using the third photolithography. After Al evaporation, the Al film is selectively etched, and the ring oscillator formed, as shown in Figure 2.

The SIT has triode-like characteristics, that is, the drain current increases exponentially with the drain voltage and does not show saturation. The usual operation of the SIT is as follows: backward bias is supplied between the gate and the source, and an increase of this negative bias causes a decrease of the drain current. In this logic-structure, however, the SIT operates *off* without a gate forward bias, due to a high potential barrier in the channel, formed by the built-in field of the P^+N^- junction. It is *on* with a positive gate bias, which causes the injection of holes into the gate from the injector. This is slight because of the high doping of the gate. The conductive channel results from a reduction of the depletion layer thickness and of potential, as shown in Figure 6. The SIT structure can also be represented as a structure similar to that of the bipolar transistor, because the base region is formed as a result of lateral diffusion of gate impurities. In this structure, a thin P-type layer of low conductivity is formed across the channel, being similar to the usual bipolar transistor. It forms a potential barrier of electrons from the source, which is controlled electrostatically by the gate and the drain potential. In this case, lowering of the injection ratio can be prevented by the high doping level of the gate region which can be thought of as an ohmic contact to the base. Both types of the SIT structure have been fabricated. Figure 3 gives the I_{SD}–V_{SD} characteristics of the earlier type of SIT, where positive gate bias is supplied. In the gate bias region below about 0.5 V, where holes are not injected into the channel, the drain current increases nearly exponentially with increasing drain voltage, with a high drain resistance. However, in the gate bias region above which hole injection occurs, the drain resistance abruptly decreases to below 10 kΩ. Figure 4 gives the I_{SD}–V_{SD} characteristics of the same SIT, where the parameter is an injection current from the gate into the channel. In Figure 5, the gate voltage dependencies on the capacitances between gate and source and between the gate and the drain are shown, for a structure containing bonding pads and two drain fanouts. The total capacitance C_t is less than 0.5 pF. The delay time-power product (τP) is expressed, approximately, as $V_b{}^2C_t$, where V_b is the supply voltage. If V_b is 0.7 V, τP is nearly 0.25 pJ in this particular device. In Figure 6, the I_{CE}–V_{CE} characteristics of the $P^+N^-P^+$ lateral transistor are shown, where the current amplification factor, β, is about 5/gate. Although the fabricated logic has not yet sufficient gain and speed, these will be improved by proper design. The proposed SIT logic (SITL) has a number of advantages promised by the structure. The small capacitances result from the $P^+N^-N^+$ structure and the high purity of the N^- channel region with carrier concentrations of $\sim10^{13}$ cm^{-3}, 2~3 orders less than that of bipolar transistors, permitting logic speeds one-order faster than those of bipolar logic configurations. Further, the

[See page 255 for Figures 4, 5 and 6]

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[3] Nishizawa, J., Terasaki, T. and Shibata, J., "Field Effect Transistor Versus Analog Transistor (Static Induction Transistor)", *IEEE Trans. Electron Devices*, ED-22, p. 185; 1975.

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SIT has an extremely small negative feed-back channel resistance, which is one of the factors leading to high logic speed, helped by the small capacitance. According to our estimates, the product of the delay time and the operational power, τP, is nearly equal to $V_b{}^2 C_t$, because there is scarcely any series resistances: V_b is the supply voltage, (0.5 V), and C_t is the total gate capacitance, $C_{gs} + 2\,C_{gd}$. When the gate area is 30 μ x 30 μ in the SIT structure of Figure 1 *(b)*, C_{gs}, C_{gd} and C_m are estimated to be 0.09 pF, 0.017 pF and 0.02 pF, respectively. (C_m is the capacitance due to the metalization of 7 μ width). The total capacitance is very small, being about 0.15 pF for a fanout of 2. As a result, the τP product is about 0.037 pJ/gate and 10 times better than that of I^2L. Further theoretical estimation gives the smallest τP product.

In the SIT, drain current, I_D, is proportional to $\exp(-\frac{qV_D}{\eta kT})$, where η is a coefficient value, less than, but close to unity. When a small signal voltage $\tilde{V}_D$ is superimposed on V_D, the signal current $\tilde{I}_D$, is approximated as $I_D \frac{q}{\eta kT} \tilde{V}_D$. Then, the τP product is approximated by $I_D V_D R C_t = I_D V_D \frac{1}{I_o} \cdot \frac{\eta kT}{q} C_t = \frac{\eta kT}{q} V_D C_t$, where R is the resistance, $\tilde{V}_D/\tilde{I}_D$.

If the drain is several μm^2, C_t is about 0.1 pF, from which τP is about 0.006 pJ, or 10^3 times smaller than that of I^2L! Other advantages of SITL are that 4-mask technology can be used and that a high packing density is available. When the self-alignment technique is introduced, using doped oxide or Si_3N_4, a 3-mask process is also expected to be possible. In I^2L, a deeply diffused N-type layer is necessary for isolation between each gate, which prevents an increase in packing density. In SITL with the high current gain of the SIT structure, the required gate current is so small that the lateral carrier diffusion does not affect the circuit operation. This fact permits very high packing densities of up to 1000 gates/mm^2. In the modified structure, where the injector is vertical, packing densities of up to 2000 gates/mm^2 are expected.

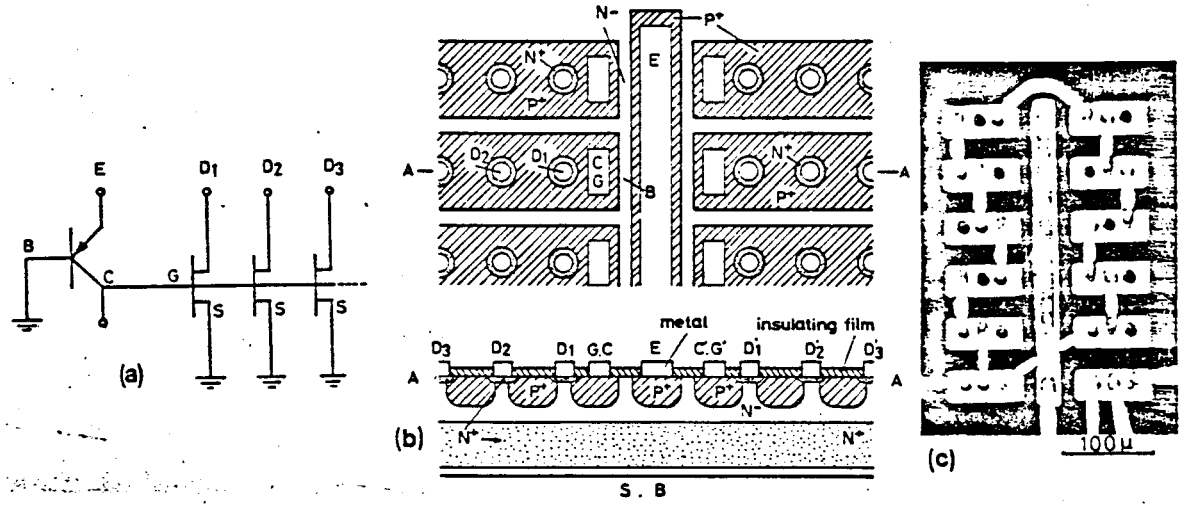

FIGURE 1 – SITL – equivalent circuit *(a)*; SITL structure using 4-mask technology *(b)*; photograph of manufactured SITL *(c)*.

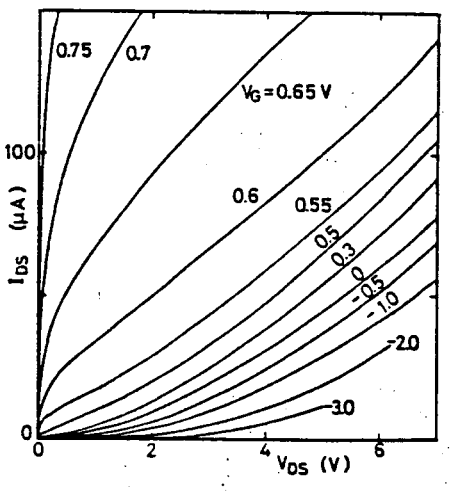

FIGURE 2 – I-V characteristics of SIT under positive gate bias.

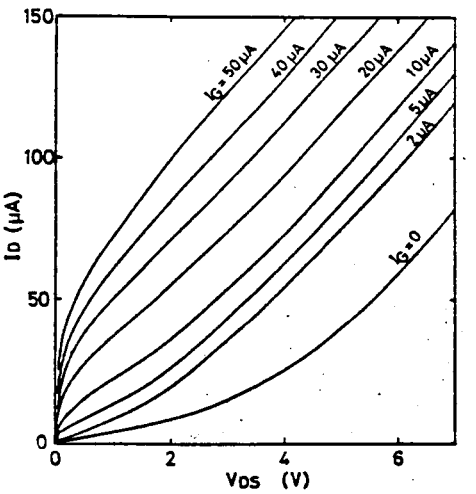

FIGURE 3 – I-V characteristics of SIT under gate current injection.

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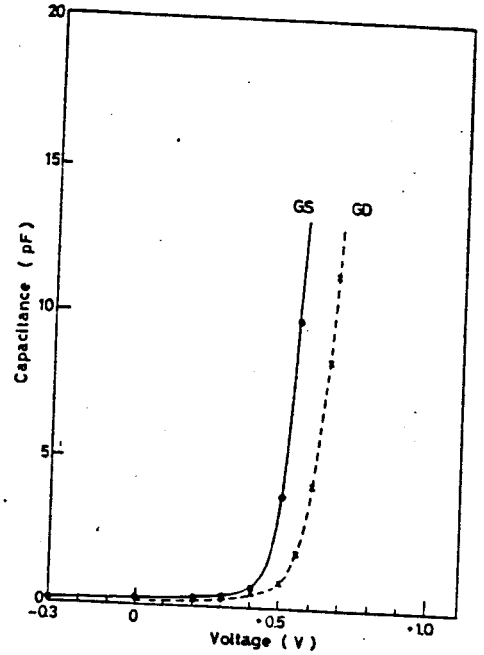

FIGURE 4 – C-V plots between gate and the source and between the gate and drain.

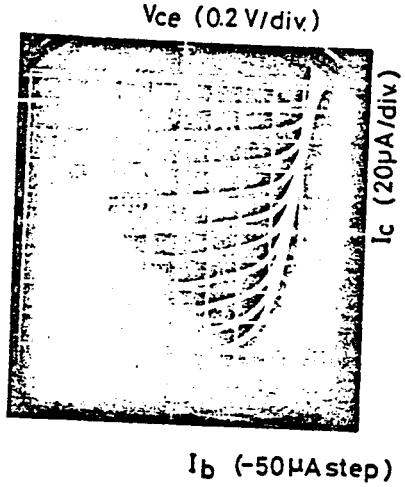

FIGURE 5 – I-V characteristics of PNP lateral bipolar transistor.

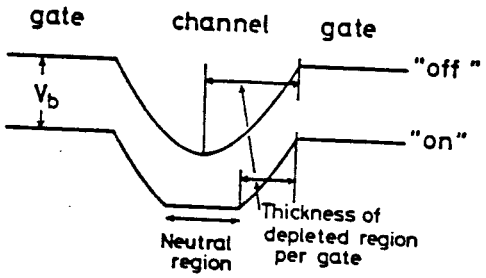

FIGURE 6 – Schematic of potential distribution across channel of SIT at forward operation.