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A New Transistor Structure and Its Application to Microenergy Logic

by

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Summary. The new transistor structure fabricated by lateral diffusion of the gate is introduced. Experimental characteristics of this transistor are presented. The logic circuit containing a new transistor is described. This bipolar integrated logic can be made using only 3 or 4 masking steps. It is characterized by a low power-delay product of the order of 0.1 pJ and a very high packing density of more than 1000 gates per sq. mm.

1. Introduction. The current trend in integrated logic circuit design is towards the reduction of both the delay time and the supply power. At present, the I^2L structure [1, 2] offers the lowest switching energy. Further reduction of this energy can be achieved in the VIL structure [3], in which the supply power efficiency has been increased, due to the increased injector current gain. However, the VIL structure requires eight masking steps. On the other hand, the Substrate-Fed-Logic [4] provides higher packing densities. The new transistor-type introduced here allows further reduction in the power-delay product.

2. Low delay-power product. For I^2L Logic family in micropower region of operation, the power-delay product can be expressed by the term

$$\tau \times P = \frac{V_{sw} V_b}{\alpha_i} C_t, \tag{1}$$

where:

V_b — supply voltage, which is determined by junction build-in field. By decreasing of impurity level one can lower this voltage.

V_{sw} — voltage swing between two logical levels. Decreasing of V_{sw} leads to lowering logic noise impurity.

— ratio of the injector current to the supply current. It also means *pnp* lateral injector efficiency. In the case of VIL structure, by vertical injection the α_i factor was improved ca. two times.

C_t — total capacitance

$$C_t = C_{sg} + n \cdot 2 \cdot C_{dg}, \tag{2}$$

n — number of outputs connected to one input.

Factor 2 is caused by Miller's effect. This capacitance can be decreased by minimizing the circuit size. However, if circuit dimensions are limited, then the second way is to decrease the impurity concentration.

If the oxide thickness is higher than 1 μm ($C=3.3$ nF/cm^2), the capacitance between metallization and silicon can be neglected. In case of source-gate capacitance C_{sg}, the depletion layer thickness can be assumed as 0.5 μm, which corresponds to $C_{sg}=10$ nF/cm^2. The gate-drain capacitance C_{gd} should be calculated in two dimensions. It can be roughly calculated from the equation:

$$C_{sg}=2\eta\sqrt{N_g}\,10^{-4}\ [\text{nF/cm}^2], \tag{3}$$

where:

N_g — surface concentration of p-type gate.

η — coefficient lower than 1, which depend on lateral diffusion and shape of drain. Practically $\eta\approx 0.1$–0.5.

3. The new type of transistor. In the presented logic circuit, a new transistor structure was introduced. Let us consider two types of transistors.

In Fig. 1*a* the bipolar transistor made by lateral p-type diffusion is shown. The potential diagrams for this structure with various biasing voltages are presented in Fig. 2. It can be seen that collector voltage has an influence on the emitter current.

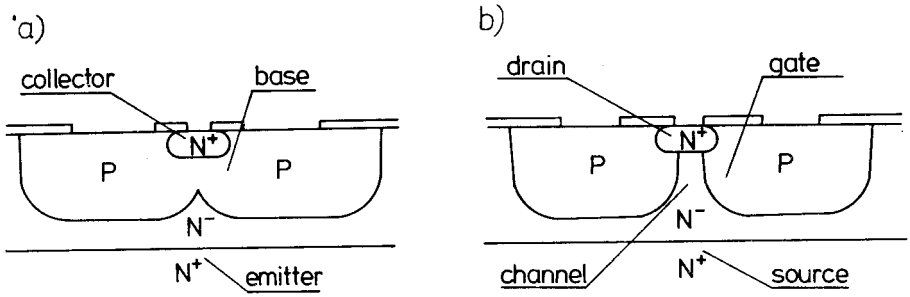

Fig. 1. Structure of the transistors made by lateral diffusion; *a*) bipolar, *b*) unipolar

In the case of the transistor structure presente din Fig. 1*b* the potential barrier for carrier injected from source is electrostatically induced by gate and drain potentials. This can be seen in Fig. 3. The height of this potential barrier V_{h2} (for the same voltage applied) is lower than V_{h1}. The structure presented in Fig. 1*b* can be operated then with lower supply voltages. This structure, however, will operate in logic circuits only when the drain potential influence on barrier height is weaker than the gate potential influence. This imposes the proper structure design. For negative and up to small positive gate potentials, the transistor presented in Fig. 1*b* operates as a Static Induction Transistor which was introduced by Nishizawa *et al.* [5]. At still higher positive gate potentials, both holes from the gate and electrons from the source are injected into the channel region. Because of the built-in field at the n^+ n^- interface only, the electrons can travel from the source to the drain, while the holes injected from the gate (for small drain voltages) create a static charge in the channel.

Fig. 4 shows the tested structure of Static Induction Transistor. The characteristics of this transistor is presented in Fig. 5 ($V_{DS}=0.5$ V/div; $I_d=10$ μA/div; $V_g=0.1$ V/step). The gate current is then caused mainly by this hole-electron recombination in the channel region. Direct injection of carrier both from the source to

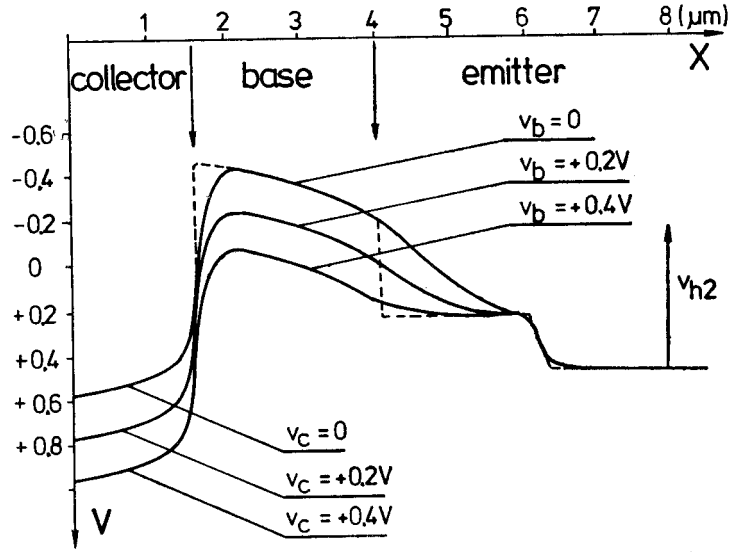

Fig. 2. Potential distribution for the transistor structure presented in Fig. 1*a*

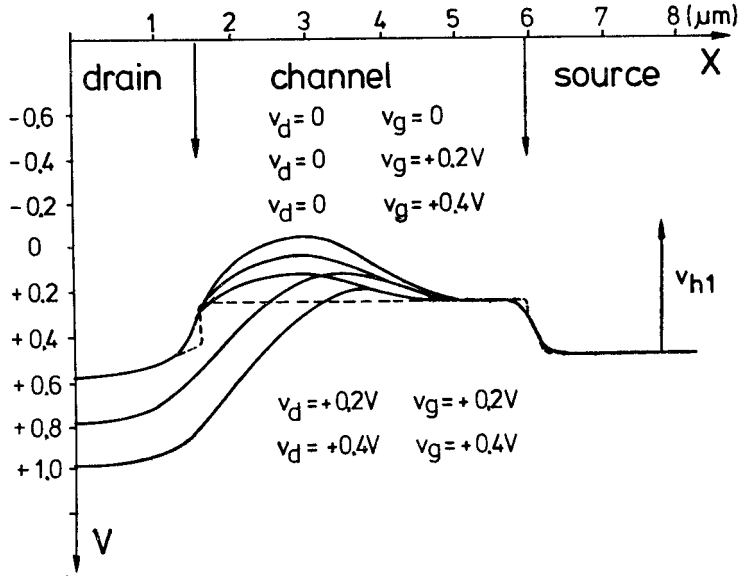

Fig. 3. Potential distribution for the transistor structure presented in Fig. 1*b*

the gate (electrons) and from the gate to the source (holes) is comparatively small, because of the presence of the built-in field. In a logic circuit this transistor operates in both the modes — the SIT mode for the high output-voltage level and the gate injection mode for the low output-voltage level.

Both transistor structures from Fig. 1 applied for logic circuit will improve the switching performance. In case of transistor from Fig. 1*a*, the delay-power product can be lowered by one order of magnitude, due to minimization of both the base-emitter capacitance originated from lower doped epitaxial layer and the collector-base capacitance caused by the specific impurity profile of the base region. Also the current gain for this *npn* transistor can be higher than in I^2L, due to non-existence of impurity gradient in the base.

The additional advantage of the transistor structure presented in Fig. 1*b* is that it can operate at smaller voltages, which gives a further decrease in the delay-power product.

Fig. 6 shows the experimental sample with ring oscillator for testing the logic delay time. After all the operation of this ring oscillator was not succeeded yet. In Fig. 7 the characteristics of *pnp* injector are presented ($V_{CE}=0.2$ V/div; $I_c=10$ μA/div; $I_g=100$ μA/step).

4. 3-Mask technology. As in usual cases the logic structure presented in Fig. 8 needs only four masking operations (*p*-diffusion, *n*-diffusion contact holes, metallization). However, because of this specific structure, wherein the entire wafer area consists of either *p*-type diffused or *n*-type diffused region only, it is possible to use

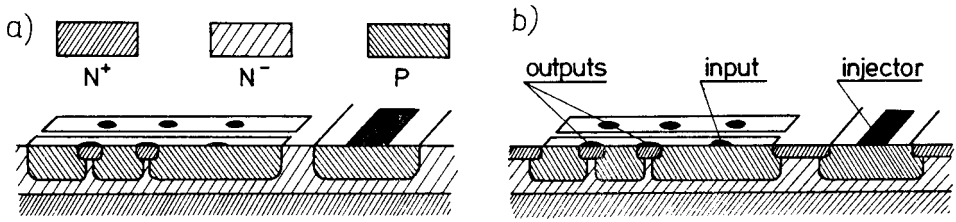

Fig. 8. Logic structures; *a*) made by 4-masking steps *b*) made by 3-masking steps

only one mask for both *p*-type and *n*-type diffusions (Fig. 8*b*). One of the known technological methods can be used for this purpose, e.g. boron doped SiO_2 or Si_3N_4 masking. This reduction in the number of masking operations required permits further miniaturization of the devices. When the Si_3N_4 is used, the self-alignment process can be applied. Therefore, in the case of minimum size of the mask windows equal to 5 μm both the n^+ drain diffusion and contacts to the drains can have sizes of the order of 2 μm and no alignment processes are necessary. The simple structure make the production process easier and the small number of masking processes can lead to the good yields comparable with MOS technology.

5. High packing density. In the I^2L structure all gates must be isolated by a deeply diffused *n*-layer to prevent lateral injection between gates. This is especially because in I^2L structure the *npn* transistor current gain is low (inversed mode operation) which results in a very low noise margin and also small fan-out. Thus, if we do not use *n*-type isolation diffusion in the I^2L, the circuit may not operate at all. In the case of the proposed structure (Fig. 1*b*), the lateral diffusion between gates

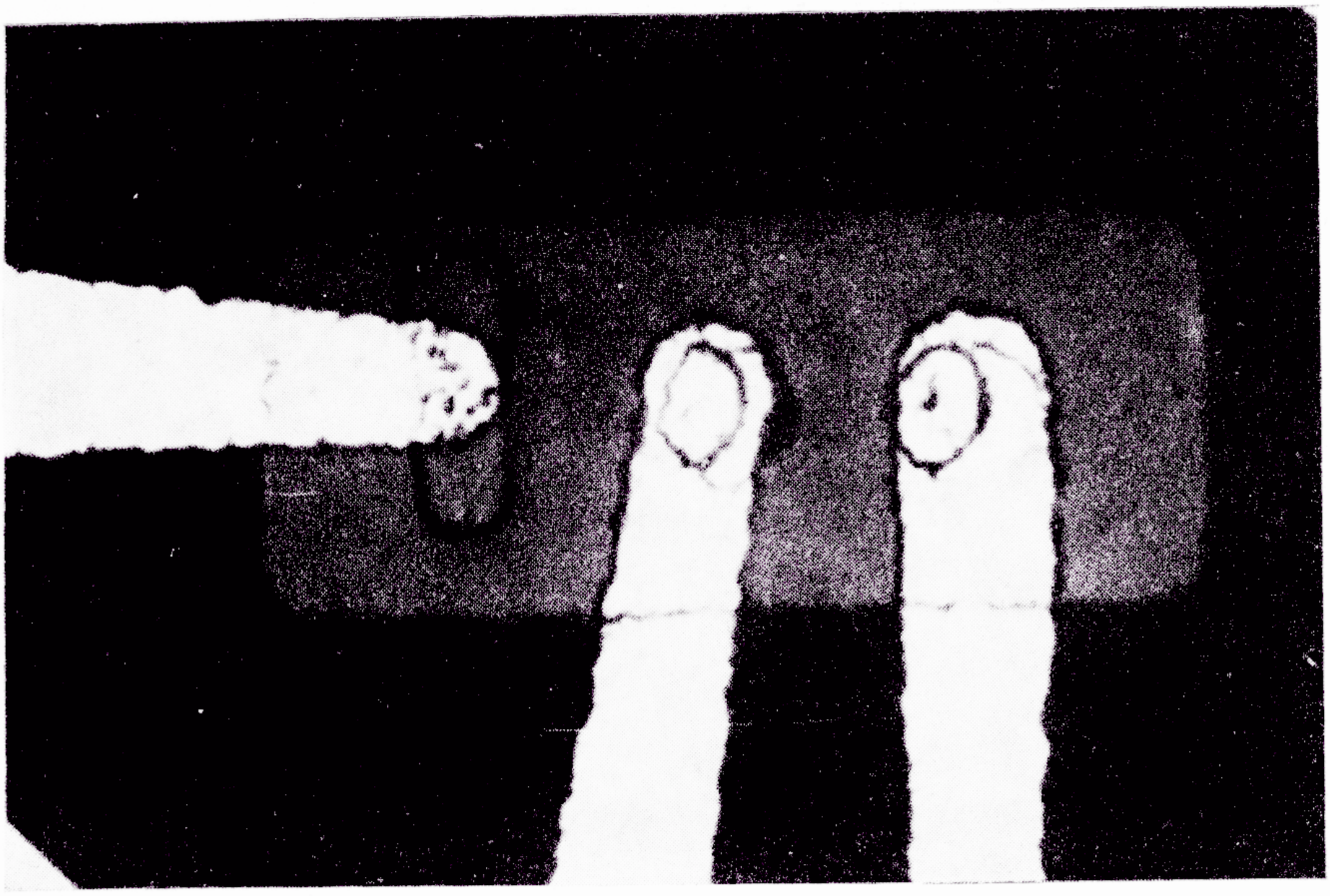

Fig. 4. The single gate

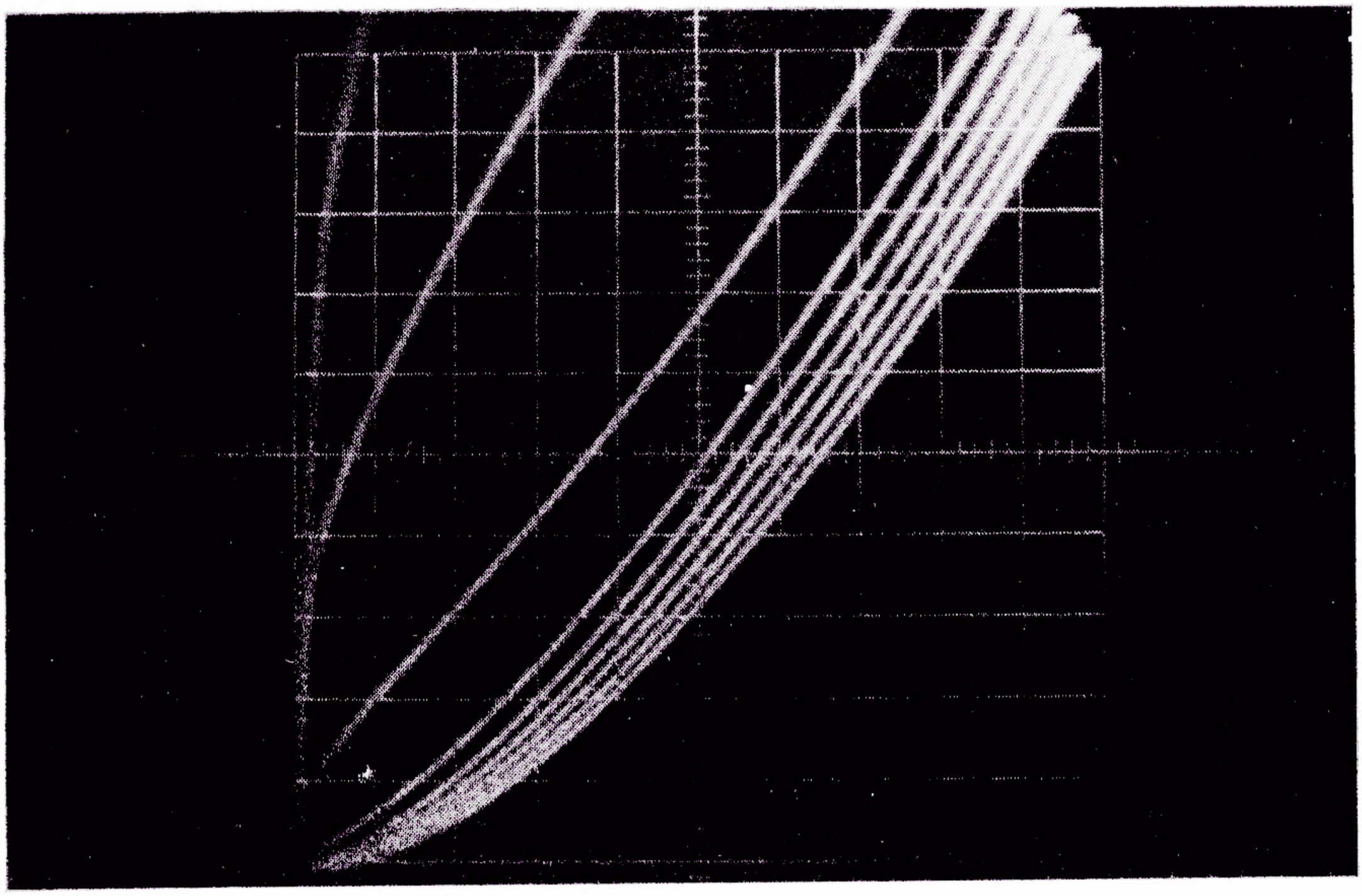

Fig. 5. Characteristics of the fabricated transistor;
(V_{ds}=0.5 V/div, I_d=10 μA/div, V_g=0.1 V/step)

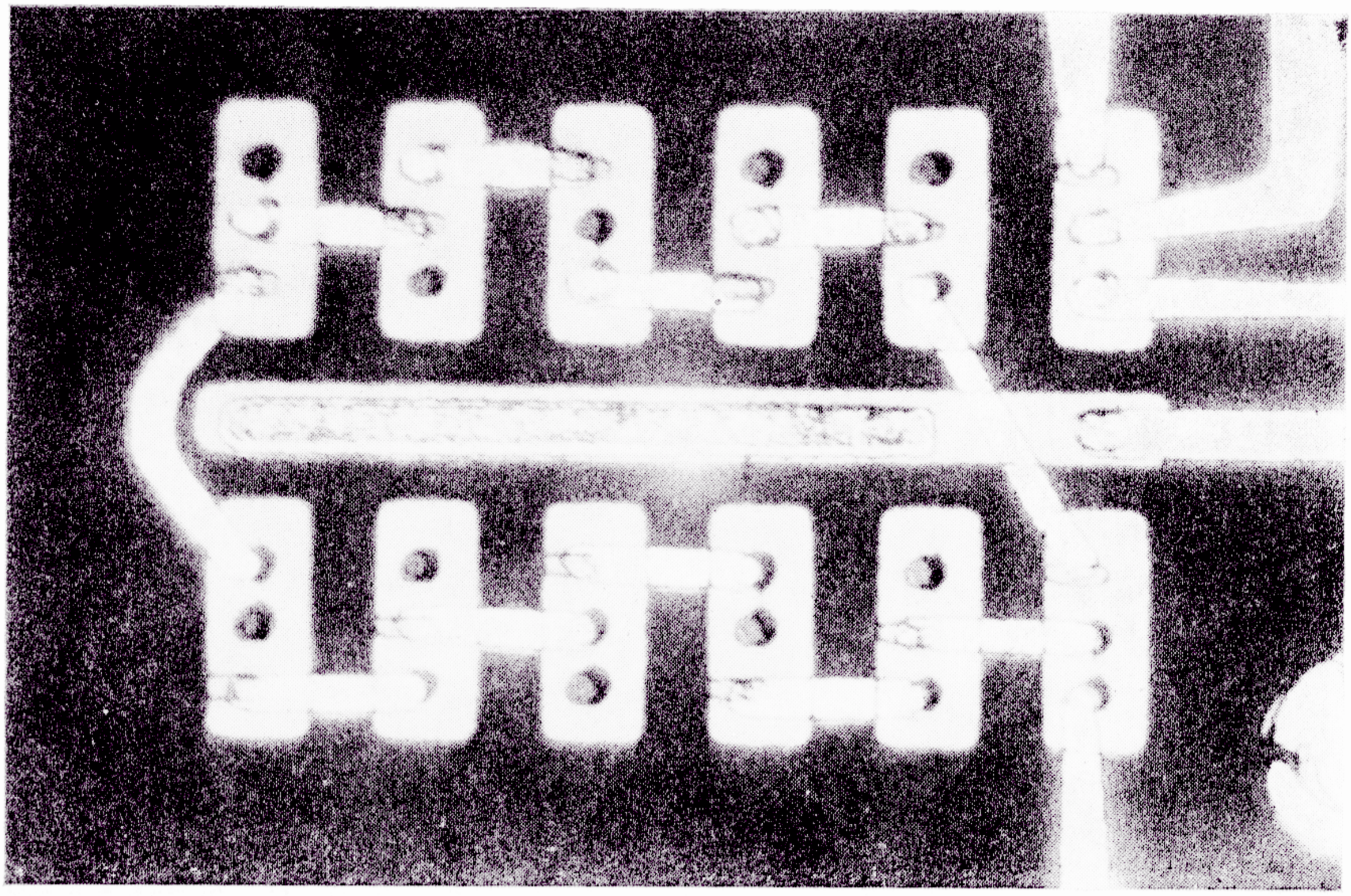

Fig. 6. Ring oscillator

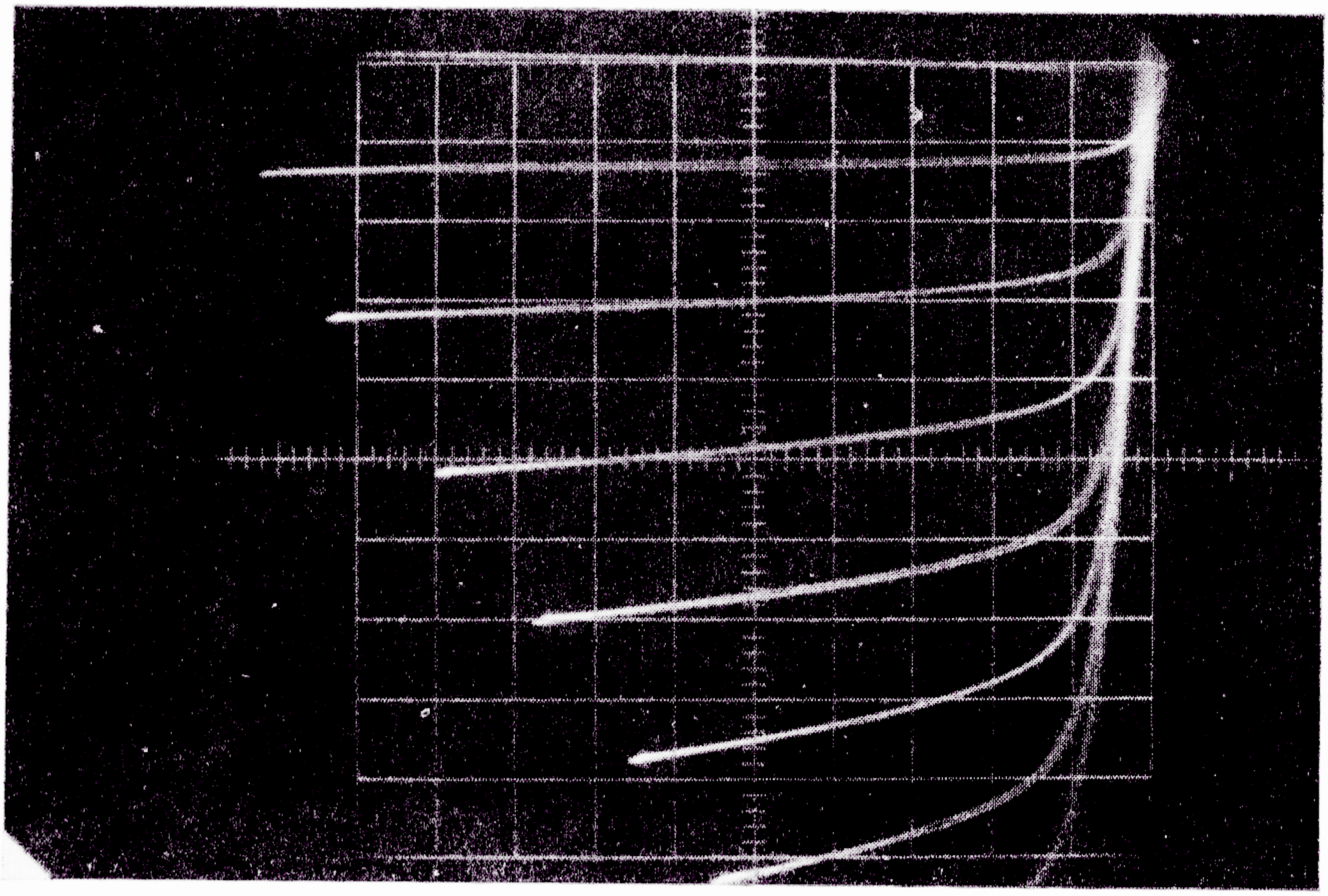

Fig. 7. Characteristics of the *pnp* injector
(V_c=0.2 V/div, I_c=10 μA/div, I_b=100 μA/step)

does not affect the circuit operation. On the contrary, this lateral injection between gates decreases the delay time, since the effective supply current is higher due to this effect. Accordingly, an *n*-type isolation diffusion layer is unnecessary. This permits very high packing densities up to 1000 double-output gates per mm^2.

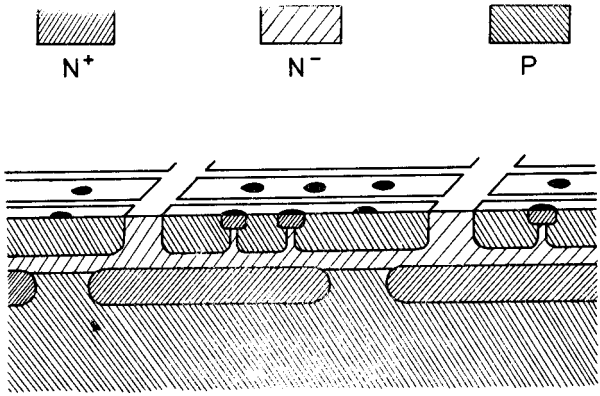

Fig. 9. Logic structure with the vertical injection

In Fig. 9, a structure with vertical injectors similar to SFL is shown. This modification allows a further increase in packing density up to about 2000 gates per mm^2. Therefore the packing density is limited only by the metal interconnection between gates.

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Б. Виламовски, **Новые структуры транзисторов и их применение для микроэнергетических логических схем**

Содержание. В работе представлена новая структура транзистора, полученная на основе затвора, использующего эффект боковой диффузии. Приведены экспериментальные характеристики этих транзисторов. Показана логическая схема, включающая новый транзистор. Эта биполярная логическая схема может быть реализована с использованием трех или четырех процессов маскировкп. Схема характеризуется низким уровнем произведения мощности и задерки (порядка 0,1 *p* и высокой плотностью упаковки, превышающей 1000 основных логических схем на 1 *мм*^{2}.