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A novel concept of neuristor logic†

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This paper describes a new method of neuristor logic construction without R junction but profiting from the threshold properties of the neuristor and annihilation collision phenomena. Neuristor diode, neuristor gate, functions ' and ', ' or ' and ' not ' are presented.

1. Introduction

H. Crane presented the neuristor concept in order to transfer the physico-chemical phenomena in the nervous network to the electronic logical networks. Crane (1960, 1962) proposed neuristor lines which have properties as follows :

1. Threshold.
2. Constant velocity of pulse transmission.
3. Shaping of pulses during its transmission.
4. Annihilation collision of two pulses.
5. Refractory period.

According to Crane the neuristor line can be connected using two kinds of junction : T trigger, in which pulses can be propagated in all directions and R refractory, in which pulses of one line will stop pulse propagation in the second one. Using these two junctions the logic network can be synthesized similarly to the real network.

Since that time many authors have presented various neuristor models : Cote (1961, 1965), Nagumo *et al.* (1962, 1965), Nishizawa *et al.* (1962, 1969, 1970), Scot (1963), Rosengreen (1963), Ambroziak (1964), Mattson (1964), Parmentier (1969) and others. But most of them reduce the problem to pulse propagation and pulse-shaping effect. The main difficulty and hindrance to the construction of a logic network are that it was possible to make practical realization of R junction only for two models (Cote 1961 and Wilamowski *et al.* 1970). But there are very complicated elements.

2. Basic principles

In this paper will be presented a new method of neuristor logic construction without R junction but profiting from the threshold properties of the neuristor and annihilation collision phenomena.

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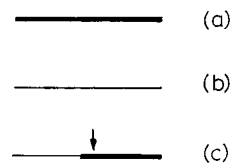
At first let us consider two kinds of neuristor lines :

1. With a normal threshold—the pulses are propagated (fig. 1 *a*).
2. With a very high threshold—the pulses are attenuated (fig. 1 *b*).

And also let us use in logic sections of neuristors with higher threshold, for example, twice as high as normal. These segments will be marked by an arrow (fig. 1 *c*).

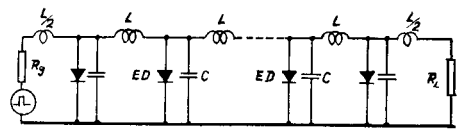
Fig. 1



Symbols of various type neuristor lines : (*a*) with normal threshold, (*b*) with very high threshold, (*c*) segment marked by an arrow with higher than normal threshold.

The above conditions are easy to perform for almost all of the published neuristor models. It is especially easy in the neuristor model with tunnel diodes (Nishizawa *et al.* 1969 and Wilamowski *et al.* 1970) presented in fig. 2. The attenuation line can be achieved using a ' shorted ' tunnel diode or resistances. The segments with higher threshold can be made using tunnel diodes with a higher ' peak current ' or simply two parallel diodes in one node.

Fig. 2

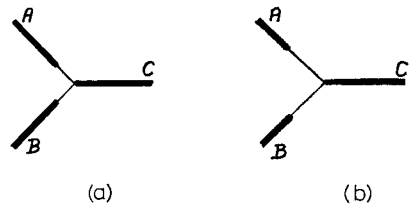


Model of the neuristor line.

3. ' Or ' and ' and ' functions

Using such lines the functions ' or ' (fig. 3 *a*) and ' and ' (fig. 3 *b*) can be constructed. In the element ' and ' the attenuation lines are longer. Only the superposition of pulses from A and B can pass the threshold in C.

Fig. 3



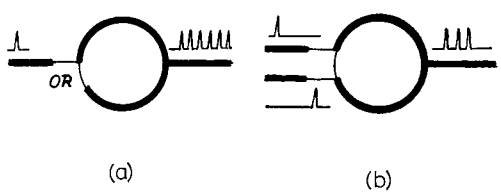
The neuristor connections : (*a*) ' or ', (*b*) ' and '.

In the element ' or ' each pulse from A or B can pass the threshold in C. Between A and B or B and A there is no pulse transmission. This element corresponds to the previously proposed T–R junction. The ' not ' realization is much more complicated and it will be described later.

4. Neuristor memory cell

A memory ring can be made using the ' or ' element. A pulse injected by the ' or ' element will circulate in the ring (fig. 4 *a*). On the output it will generate the sequence of pulses. To cancel the pulse it is necessary to inject a pulse by a similar element ' or ' in the opposite direction. The pulses after the collision will anihilate each other (fig. 4 *b*). The pair or voluntary sequence of pulses can be generated using the ' or ' element and various lengths of lines (fig. 5).

Fig. 4



Memory rings : (*a*) without cancel input, (*b*) with cancel input.

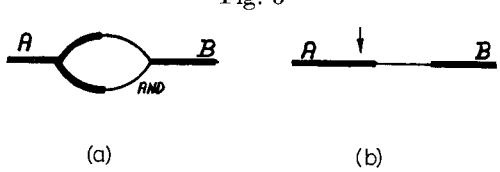
Fig. 5

The pair pulse generator.

5. Neuristor diode

One direction of pulse propagation can be achieved using ' and ' elements (fig. 6 *a*). Pulses will propagate from A to B only. This element can be treated as a neuristor diode. Such a diode can also be made simply by using part of the higher threshold line. The pulse from A to B (fig. 6 *b*) is attenuated and it cannot pass a raised threshold in A. In the opposite direction from A to B the attenuated pulses can pass normal threshold in B.

Fig. 6

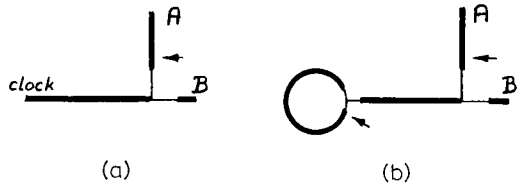


The neuristor diodes : (*a*) using and elements, (*b*) using segment with a raised threshold.

6. Neuristor ' not ' functions

The construction of this element is shown in fig. 7 (*a*). The clock pulses can achieve B if there are no pulses from A. Each pulse of A due to an ' or ' junction will go to the left direction and it will anihilate one clock pulse. The clock pulses can achieve B only if there are no pulses from A. On the output B there is a negation of A. In the point C the threshold must be raised in order to stop the clock pulse to the input A. The memory ring can be used as the clock (fig. 7 *b*). It is also possible to use one memory ring as the clock for the whole neuristor network.

Fig. 7

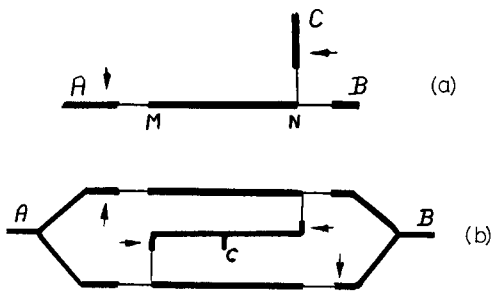


The ' not ' elements : (*a*) supplied by clock, (*b*) supplied by own memory ring.

7. Neuristor gate

It is interesting to note that in this way it is possible to construct a conventional Crane R junction which can be called the neuristor gate (fig. 8 *a*). Pulses from A to B can be propagated only if there are no pulses from C. In the opposite case pulses from C will anihilate pulses from A in the segment MN. The neuristor diode is used in order to stop pulses from C. A two-directional neuristor gate is shown in fig. 8 (*b*).

Fig. 8



The neuristor gate : (*a*) one-directional, (*b*) two-directional.

8. Conclusion

The new realization of neuristor logic using threshold phenomena and annihilation collision presented in this paper makes neuristor logic networks quite simple. This logic can be applied to most known neuristor models.

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