

Neuristor propagation in low impedance line†

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This paper describes the character of neuristor operation composed of a lumped parameter delay line with a negative resistance element parallel to the capacitance, as a function of the precise character of the negative resistance element. This model allows a neuristor pulse transmission in cases with very low characteristic impedance $Z_0 = \sqrt{L/C}$. The experiments cover a Z_0 value down to 11Ω . A lower characteristic impedance is possible. The model is analysed, applying Lienard's graphical method and linear approximations. As a result the criteria for characteristic parameters of negative resistance elements to operate as a neuristor are obtained. Based on the results, a neuristor with low inductance, small power, and high-speed operation can be designed. This circuit is convenient for neuristor logic, because, compared with the peculiar pulse width, it has a long delay time per section. The paper also describes neuristor logic without an R-type junction, using only the threshold property of the neuristor. A conventional Crane's R-junction is also presented. For this neuristor model a destructive collision phenomenon exists independent of the refractory period phenomena. The mechanisms of these phenomena are clarified.

List of symbols

NRE negative resistance element (fig. 2).

v voltage.

t time.

i current.

n number of stages.

p $s\sqrt{LC}$ normalized operator.

i_n current by NRE.

I_p peak current of NRE (fig. 3 a).

I_v valley current of NRE (fig. 3 a).

ΔI ($I_p - I_v$), see fig. 31.

V_b biased voltage of additional diode, see fig. 2.

V_{th} threshold voltage of neuristor line.

V_{sup} supply voltage.

$2V_0$ step amplitude of input pulse.

ΔV difference of voltages between high conductance region and negative impedance region, see fig. 18.

V_d drop voltage on additional parallel diode.

V_u lowest voltage of unstable region (fig. 22).

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- V_{in} input pulse voltage.
- V_{out} output pulse voltage.
- L unit inductance of neuristor line.
- L_s supply inductance (fig. 1).
- C unit capacitance of neuristor line.
- C_j junction capacitance.
- C_s stray capacitance.
- C_c coupling capacitance.
- R_s series resistance (fig. 2).
- R_c coupling resistance (fig. 20).
- R_g generator resistance.
- R_L load resistance.
- R_a resistance of approximation see, fig. 22.
- G_n non-linear conductance of NRE.
- r differential resistance of NRE.
- r_n dv/di negative resistance (fig. 31).
- r_a dv/di differential resistance in first region of NRE characteristic, see fig. 31.
- r_b dv/di differential resistance in high conductance region of NRE characteristic, see fig. 31.
- τ_c $1/\omega_c = \sqrt{LC}$ time constant for neuristor line.
- τ_r refractory period.
- τ_w width of pulse.
- τ_d delay time per one section.
- Z_0 $\sqrt{L/C}$ characteristic impedance of neuristor line.
- k $Z_0/r = G_n \sqrt{L/C}$.

1. Introduction

The neuristor is a digital logic device, it has been developed from the study of the operation of the nervous system neuron. It can be applied as a micro-logic element in computer realization. The wave shaping action and threshold property make it very useful in both the logic and highly reliable pulse transmission in pulse code communications.

Since Crane (1960, 1962) presented the theoretical model of the neuristor and neuristor logic realization various model circuits have been published by many authors. Cote (1961) made a neuristor using four layer diodes and R-C network. Nagumo *et al.* (1962) presented a neuristor model using tunnel diodes as monostable elements, and then as bistable elements (1965). The stability criterion for the latter was analysed by Parmentier (1968). Based on Crane's idea Rosengreen (1963) made a neuristor with four-layer diodes. The elements were made by the integrated circuit technique. A long refractory period compared with the delay time required the use of many single sections in order to achieve logic. In the storage ring, for example, 50 stages were necessary. Mattson (1964) proposed building a neuristor using the negative resistance of unijunction transistors. This model had a simple structure and was easily integrated but compared with the energy of the transmission signal an inordinately high supply current was necessary. This model had the same fault as Rosengreen's neuristor.

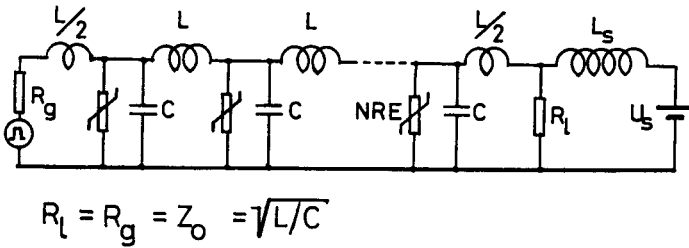
A neuristor using a delay line with tunnel diodes in nodes was proposed by Nishizawa (1961). Noguchi *et al.* (1963) studied this model using a computer. They found that destructive or non-destructive collision of pulses from opposite directions depended on the non-linear characteristic of the Esaki diode. Cote (1965) made a solid state form distributed tunnel diode, but only some properties of the neuristor were present. Scott (1964) showed the possibility of using a distributed superconducting tunnel junction to make a neuristor. Parmentier (1969) published theoretical calculations and experimental results using this Josephsen tunnel junction with the line at liquid helium temperatures. The properties of this line were strongly dependent on the temperature. The very small delay time (5 nsec) compared with the pulse width (1200 nsec) does not make it useful for logic.

Some theoretical explanation and experimental data on the neuristor using a lumped parameter delay line have been made by Nishizawa and Hayasaka (1969). The lowest limit for characteristic impedance $Z_0 = \sqrt{L/C}$, using a Ge Esaki diode with a peak current $I_p = 2$ mA, was found to be about 120 Ω . This paper gives further experimental data and a more precise theoretical analysis. The method is given of synthesis of the optimum non-linear characteristic of a negative resistance element for achieving a pulse propagation for an even lower impedance neuristor line.

2. Experiments

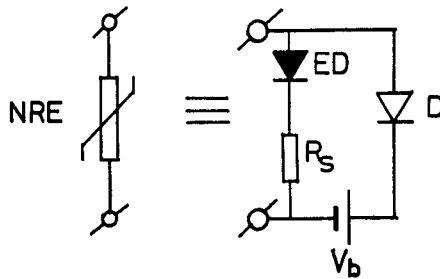
All experiments were made on the circuit presented in fig. 1. For investigation of the influence of the non-linear characteristics, the negative resistance element NRE was synthesized (fig. 2). The basic $I-V$ characteristics of NRE

Fig. 1



Experimental neuristor circuit.

Fig. 2



Negative resistance element (NRE).

could be changed using various R_s and V_b (figs. 3 c, 3 d). The biased voltage V_b was common for all NRE elements in the neuristor line.

For all experiments the following elements and instruments were used :

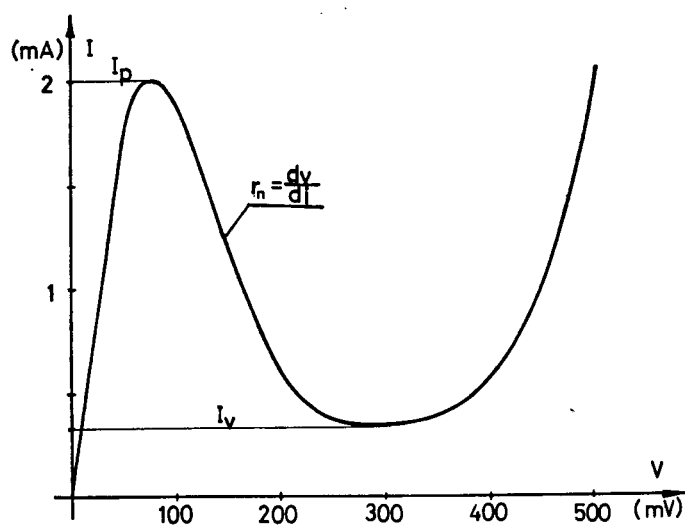
- (1) Tunnel diodes, 1T 1103 (Sony).

$$I_p = 2 \pm 0.1 \text{ mA}, C_j < 6 \text{ pF}, I_v < 0.3 \text{ mA.}$$

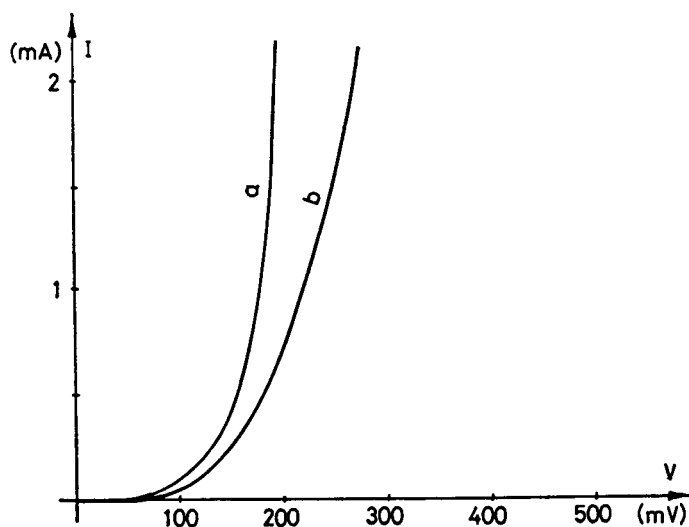
$$|r_n| = 60 \sim 80 \Omega \text{ (fig. 3 a).}$$

- (2) The germanium transistors with the base shorted to the collector in order to get as sharp $I-V$ characteristics as possible (fig. 3 b).
- (3) These germanium transistors were connected as a parallel diode in NRE.

Fig. 3

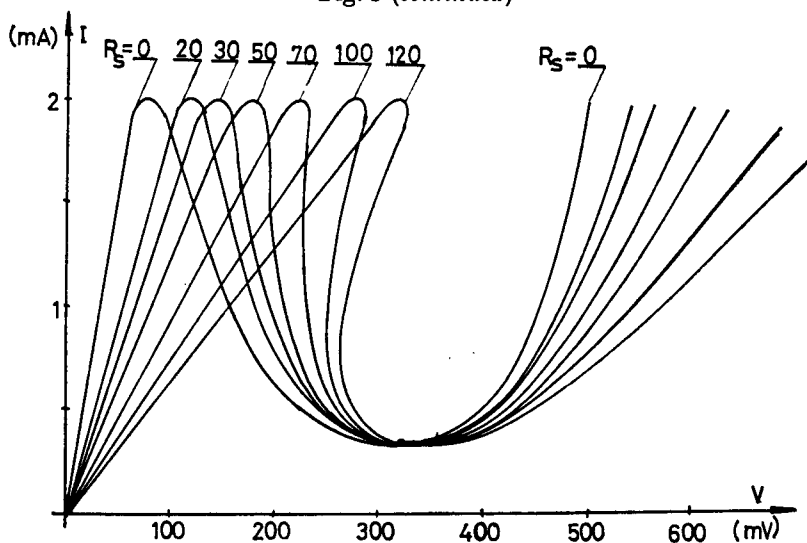


(a)

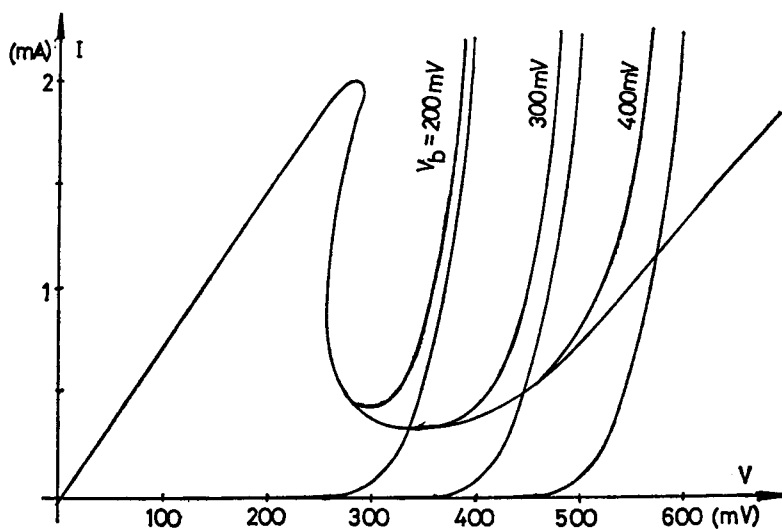


(b)

Fig. 3 (continued)



(c)



(d)

Typical characteristics. (a) Esaki diodes. (b) Transistors used as diodes. (a) emitter-collector characteristics base shorted to collector, (b) emitter-base characteristics. (c) Esaki diode and resistors in series. (d) NRE for various biased voltages. $R_s = 100 \Omega$.

- (4) Resistors and capacitors with tolerance less than $\pm 2\%$.
- (5) Home-made inductances with a tolerance of less than $\pm 10\%$ and loss resistance lower than 0.5Ω .
- (6) Oscilloscope : Textronix 545 A with probe input $10 \text{ m}\Omega$, 11 pf .
- (7) Pulse generator : General Radio 1391.

Experiments, trying many factors of the NRE characteristics, have been made using neuristor lines with various characteristic impedances $Z_0 = \sqrt{L/C}$

and various time constants $\tau_c = \sqrt{LC}$. Neuristor lines with $Z_0 = 200 \Omega$, 100Ω , 50Ω , 23Ω , 18Ω , 11Ω were investigated. The biased voltage was variable. $R_s = 0 \Omega$, 20Ω , 30Ω , 50Ω , 70Ω , 100Ω and 120Ω were used as series resistances.

For investigating the neuristor characteristic as a function of the value of Z_0 , only lines with a constant $\tau_c = 730$ nsec and with varying values of Z_0 such as 100Ω , 50Ω and 23Ω were used. In order to evaluate the influence of varying Z_0 , experiments on neuristor lines with a constant Z_0 and various τ_c was made. It was found that the results were the same, if we consider with the normalized time as: $t^* = t/\sqrt{LC}$.

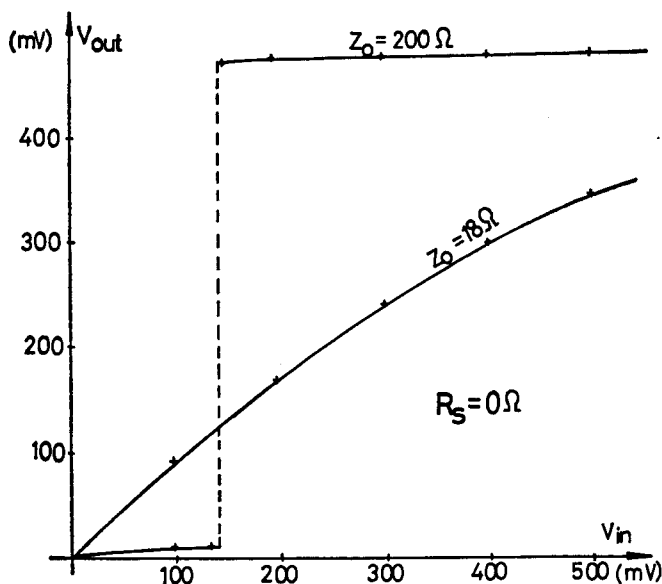
In later experiments the influence of various τ_c was neglected. The trigger pulse was applied from the pulse generator and a pulse transmission was observed in successive stages by an oscilloscope. Small 2Ω resistors for reading the sum current through capacitance and negative resistance element were put into the circuit. Thus I - V loops could be observed.

3. Results of the measurements

3.1. Threshold phenomena

This was investigated by measuring the pulse amplitude in the 6th section as a function of the input pulse voltage. In the case of $R_s = 0$ and high V_b , a nice sharp threshold characteristic was observed only when there was a high impedance neuristor line, with $Z_0 = 200 \Omega$. In lower impedance neuristor lines only pulse attenuation was present (fig. 4). The lowest limit of characteristic impedance for sharp threshold action was published previously by Nishizawa and Hayasaka (1969) as $Z_0 = 120 \Omega$. The present work achieved

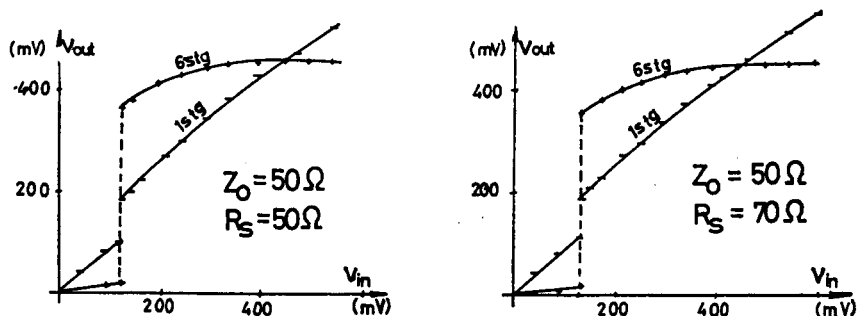
Fig. 4



Output-input amplitude characteristics of neuristor line measured on 6th stage.
 $I_{sup} = n \times 1.5$ mA, $Z_0 = 18 \Omega$ and 200Ω .

a sharp threshold property for lower characteristic impedances by using resistors and Esaki diodes in series (fig. 3 c). In the case of $R_s = 50 \Omega$ an exciting threshold, even for a line with $Z_0 = 50 \Omega$, was found to be present

Fig. 5



Output-input amplitude characteristics. $Z_0 = 50 \Omega$, $I_{sup} = n \times 1.5 \text{ mA}$.
(a) $R_s = 50 \Omega$; (b) $R_s = 70 \Omega$.

(fig. 5). In a low impedance neuristor line with $Z_0 = 18 \Omega$ and $Z_0 = 11 \Omega$ the exciting threshold was created with a series resistance higher than 70Ω (fig. 6).

$$R_s \geq 70 \Omega \quad (3.1)$$

is necessary to get a sharp threshold action in a low impedance neuristor line. It has been found that the threshold decreases with a decrease of Z_0 . However, the dependence of threshold on R_s can be neglected.

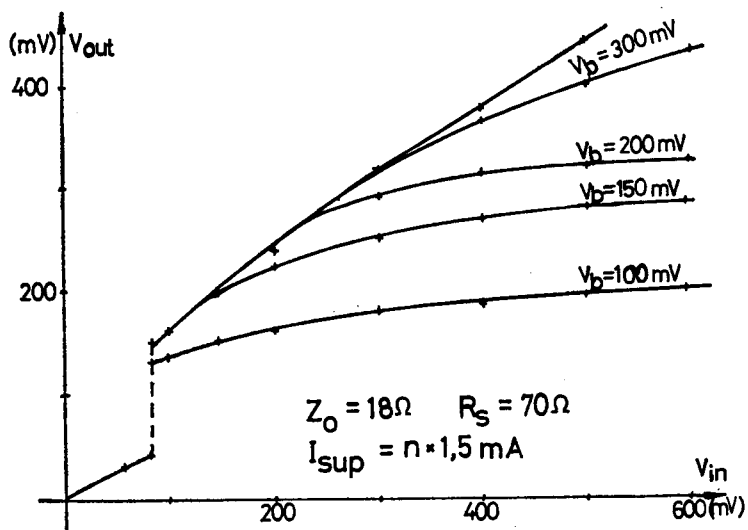
3.2. Shaping action

The effect of pulse shaping during pulse transmission has been observed. Shaping action for all types of neuristor lines was investigated. Normal, high, narrow and wide pulses have been applied to line input. The oscillograms on figs. 7, 8, 9, 10, 11, 12 and 13 show the shaping effect.

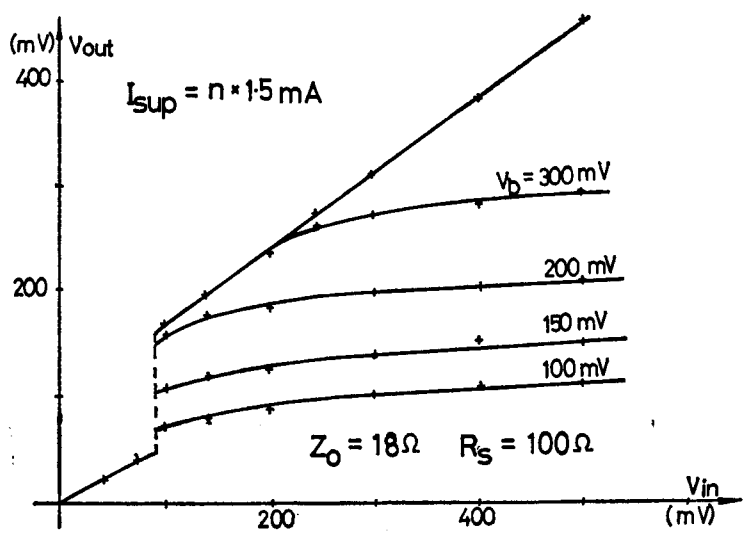
With high amplitude of input pulse and high R_s the pulse amplitude in later sections were strongly dependent on the V_b (fig. 14). This was noted because by a change of V_b , the high conductance region of the NRE characteristics can be moved (fig. 3 d).

One or two stages are always sufficient for shaping action in the case of the narrow pulse. See oscillograms (c) in figs. 7, 8, 9, 10, 11, 12 and 13. For wide pulse a very small shaping effect has been observed (oscillograms (d)). It is slightly better in neuristor with a higher Z_0 . Series resistance made it worse. Nice width shaping action can be achieved only in the cause of a small supply current (fig. 15 b). This small current was not sufficient for pulse transmission and the normal pulse was attenuate. In the case of the wide pulse with an amplitude slightly below threshold the shaping action occurred, thanks to the 'ringing'. In the case of the wide pulse with an amplitude above the threshold, the shaping action occurred as a result of both an increased risk time and the threshold phenomenon. With a higher amplitude and width the results were worse.

Fig. 6

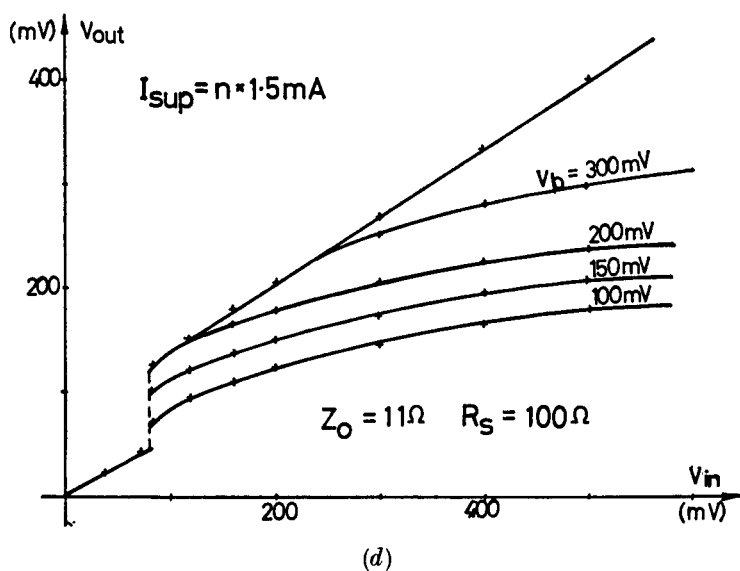
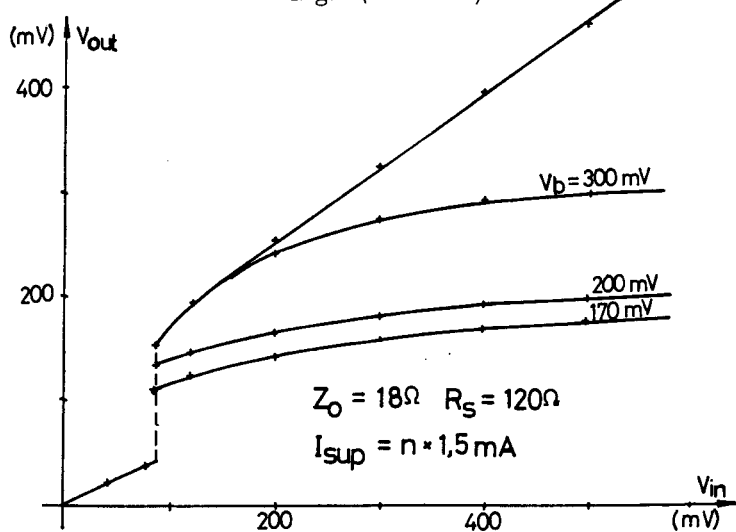


(a)



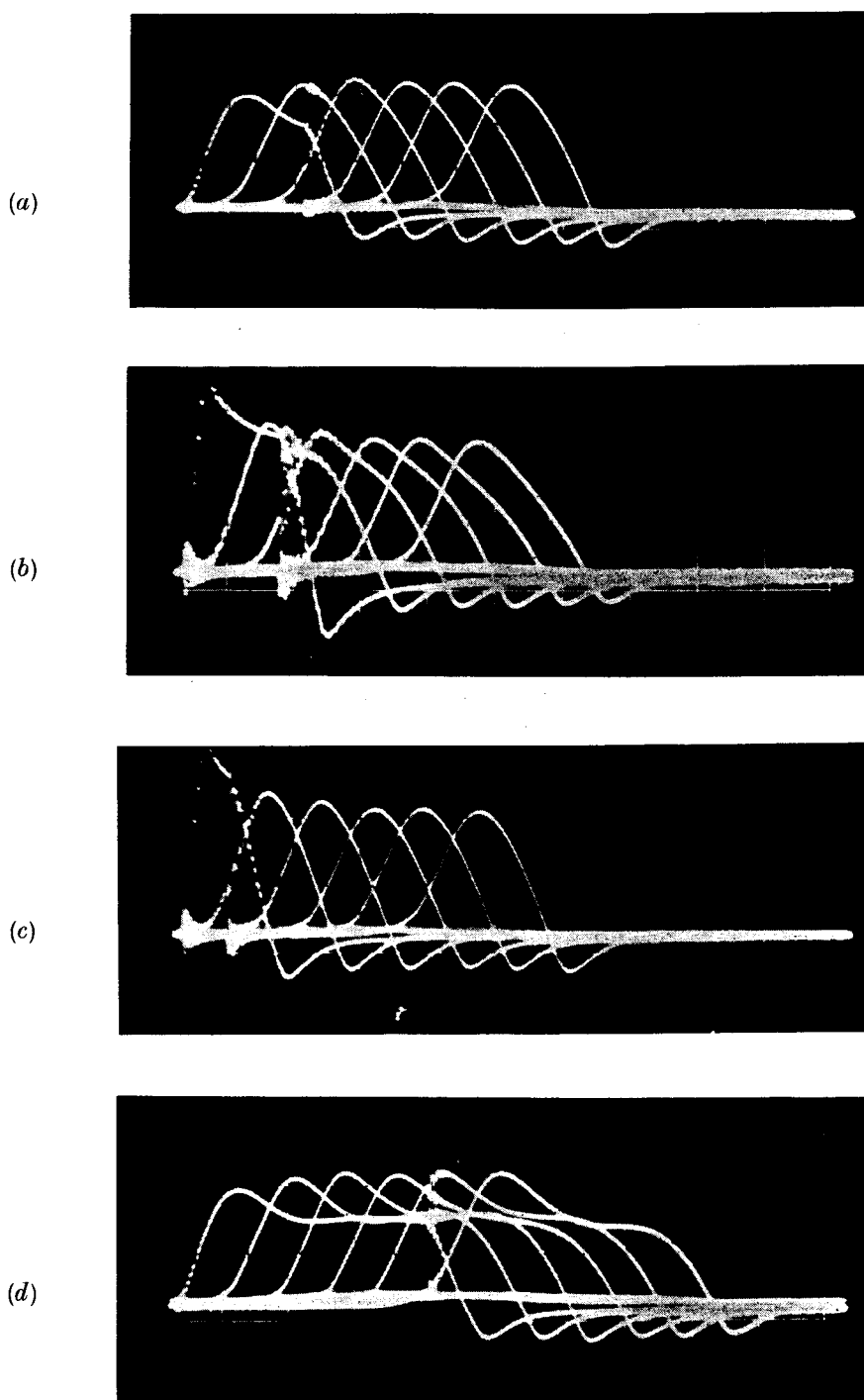
(b)

Fig. 6 (continued)



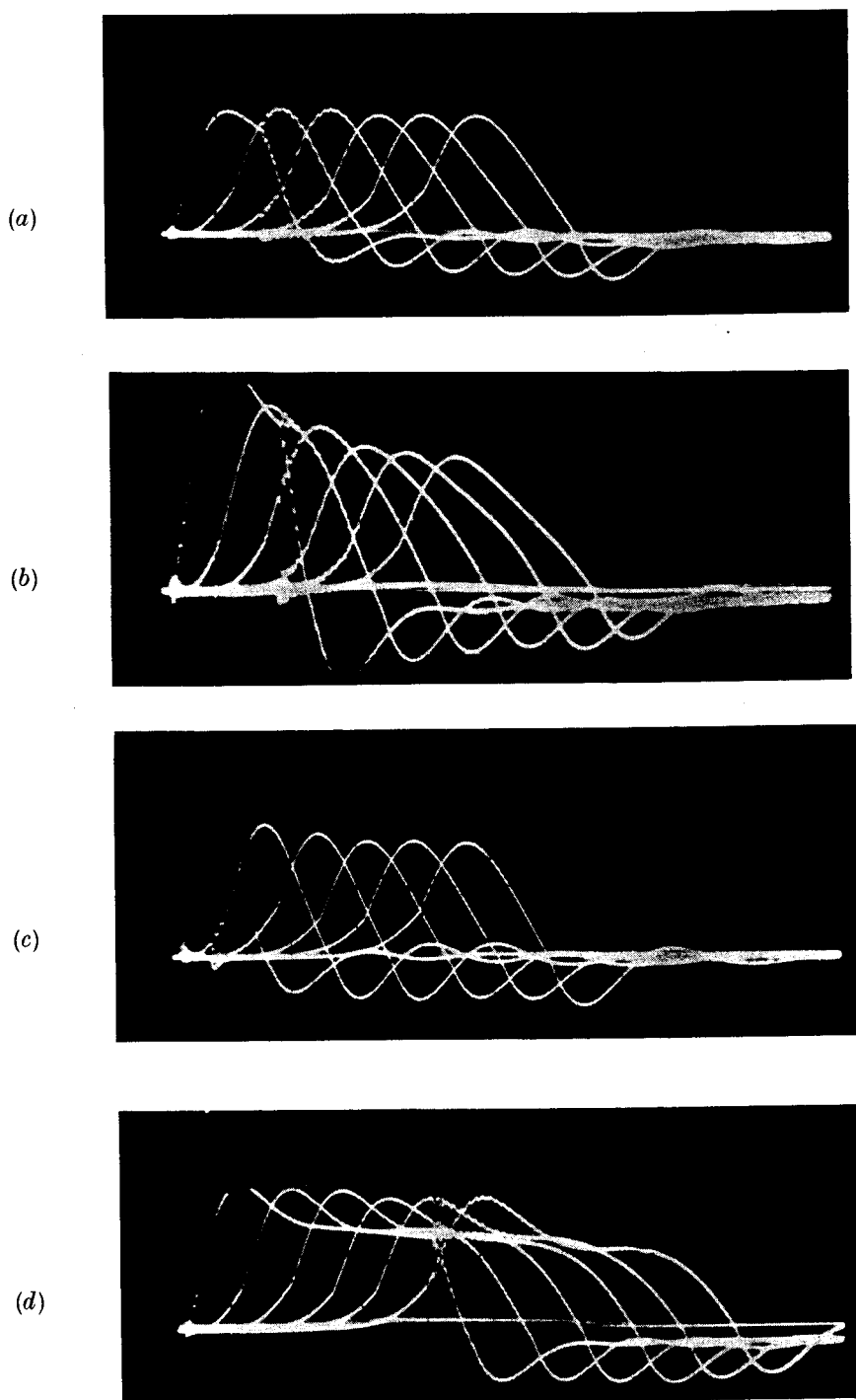
Output-input amplitude characteristics measured on 6th stage for a neuristor line with various biased voltages. $I_{sup} = n \times 1.5 \text{ mA}$. (a) $Z_0 = 18 \Omega$, $R_s = 70 \Omega$, (b) $Z_0 = 18 \Omega$, $R_s = 120 \Omega$, (c) $Z_0 = 18 \Omega$, $R_s = 100 \Omega$, (d) $Z_0 = 11 \Omega$, $R_s = 100 \Omega$.

Fig. 7



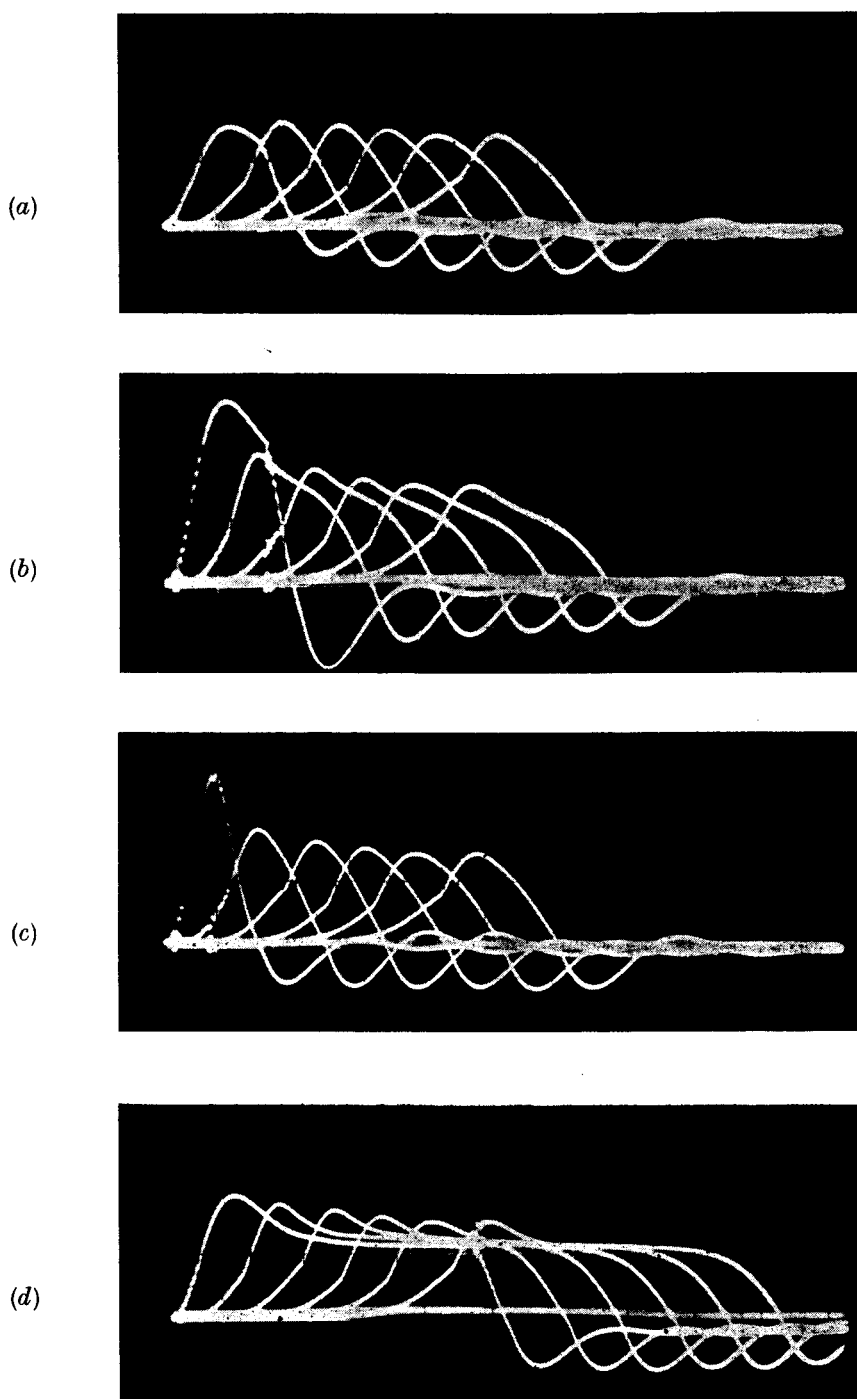
Pulse shaping action in neuristor line with $Z_0 = 100 \, \Omega$, $R_s = 0 \, \Omega$, $V_b = \text{high}$ for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $1 \, \mu\text{sec}/\text{div.}$, vertical $200 \, \text{mv}/\text{div.}$).

Fig. 8



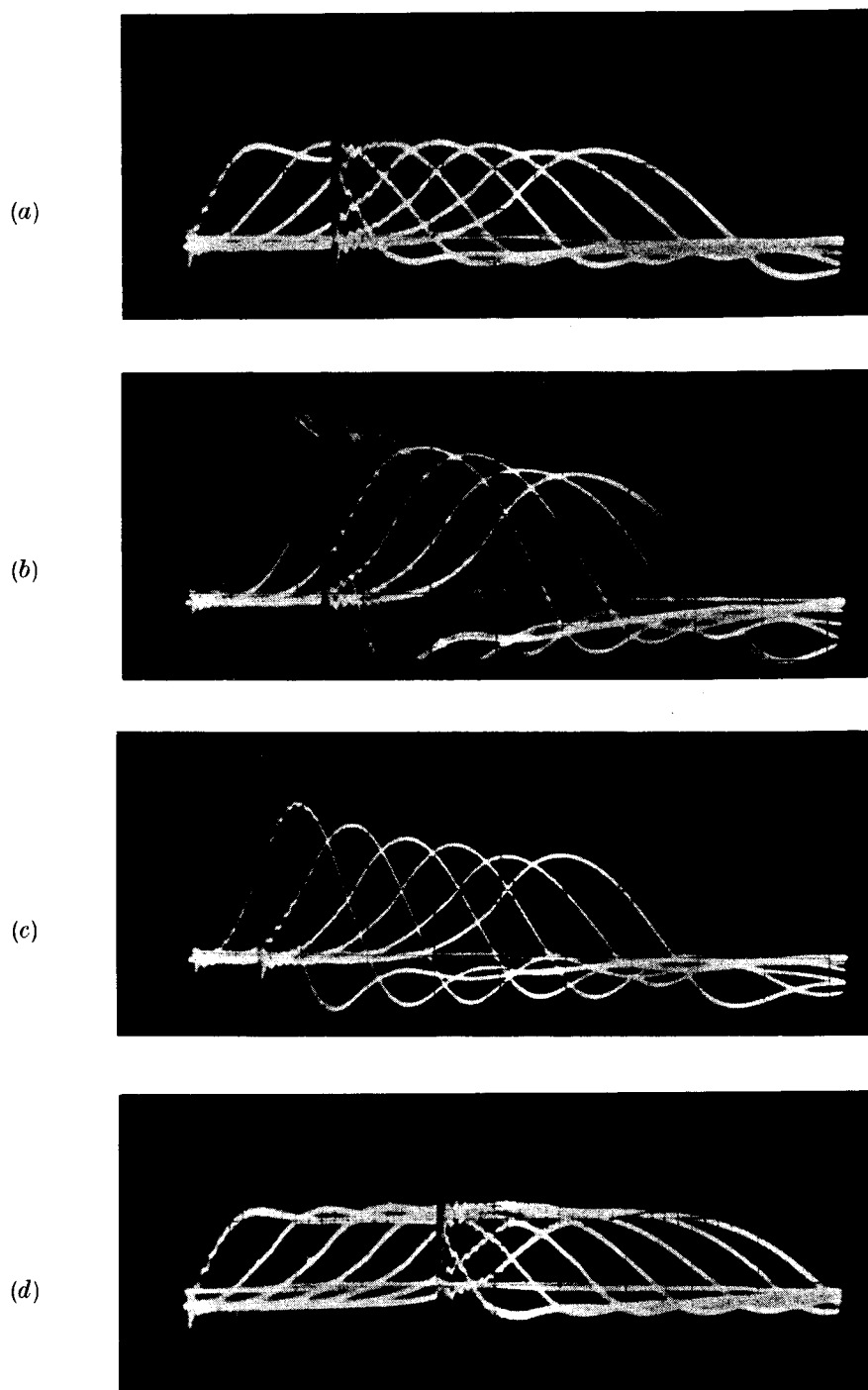
Pulse shaping action in neuristor line with $Z_0=100\ \Omega$, $R_s=120\ \Omega$, $V_b=\text{high}$, for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $1\ \mu\text{sec}/\text{div.}$, vertical $200\ \text{mv}/\text{div.}$).

Fig. 9



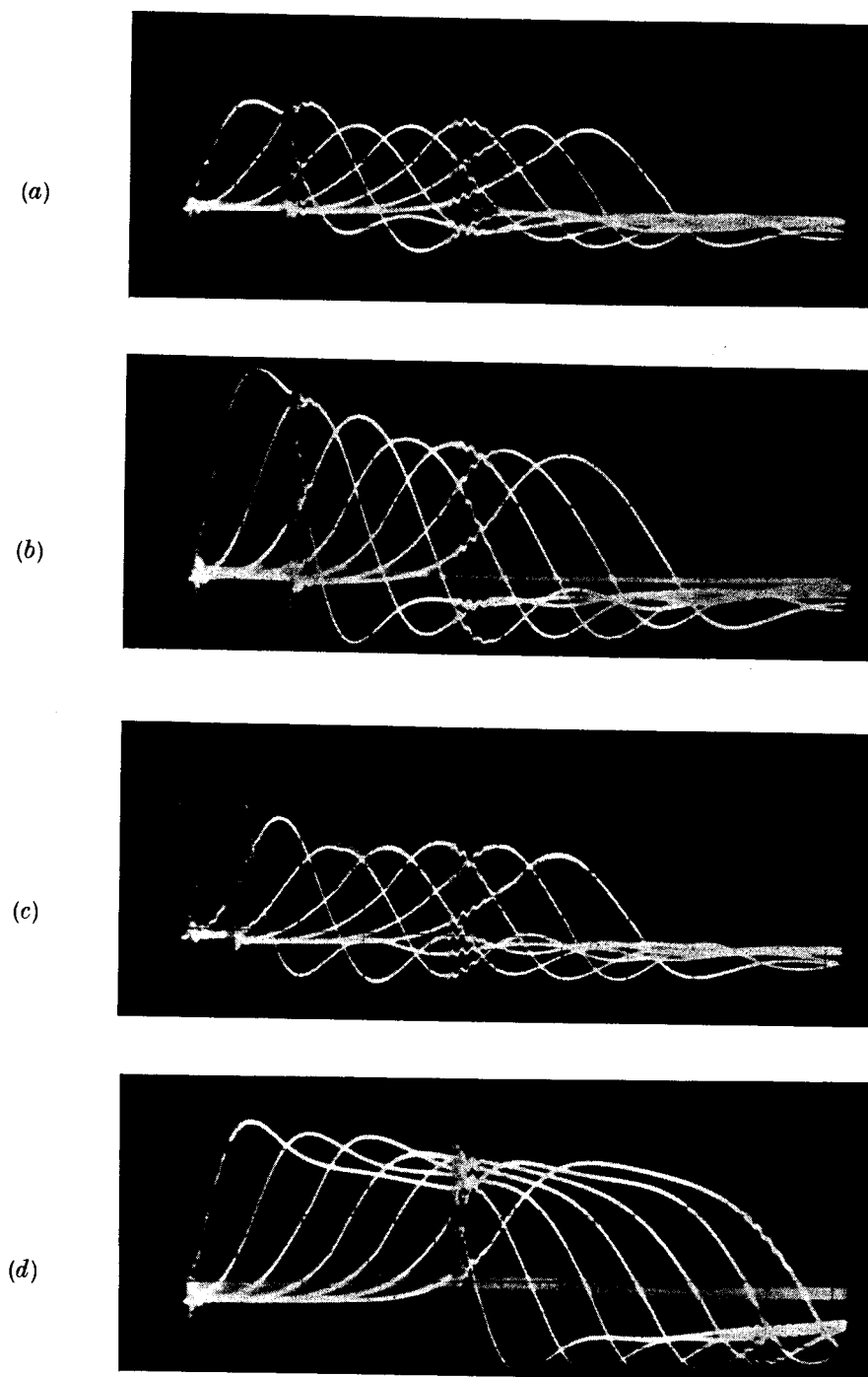
Pulse shaping action in neuristor line with $Z_0=100\ \Omega$, $R_s=120\ \Omega$, $V_b=300\text{ mv}$, for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $1\ \mu\text{sec/div.}$, vertical 200 mv/div.).

Fig. 11



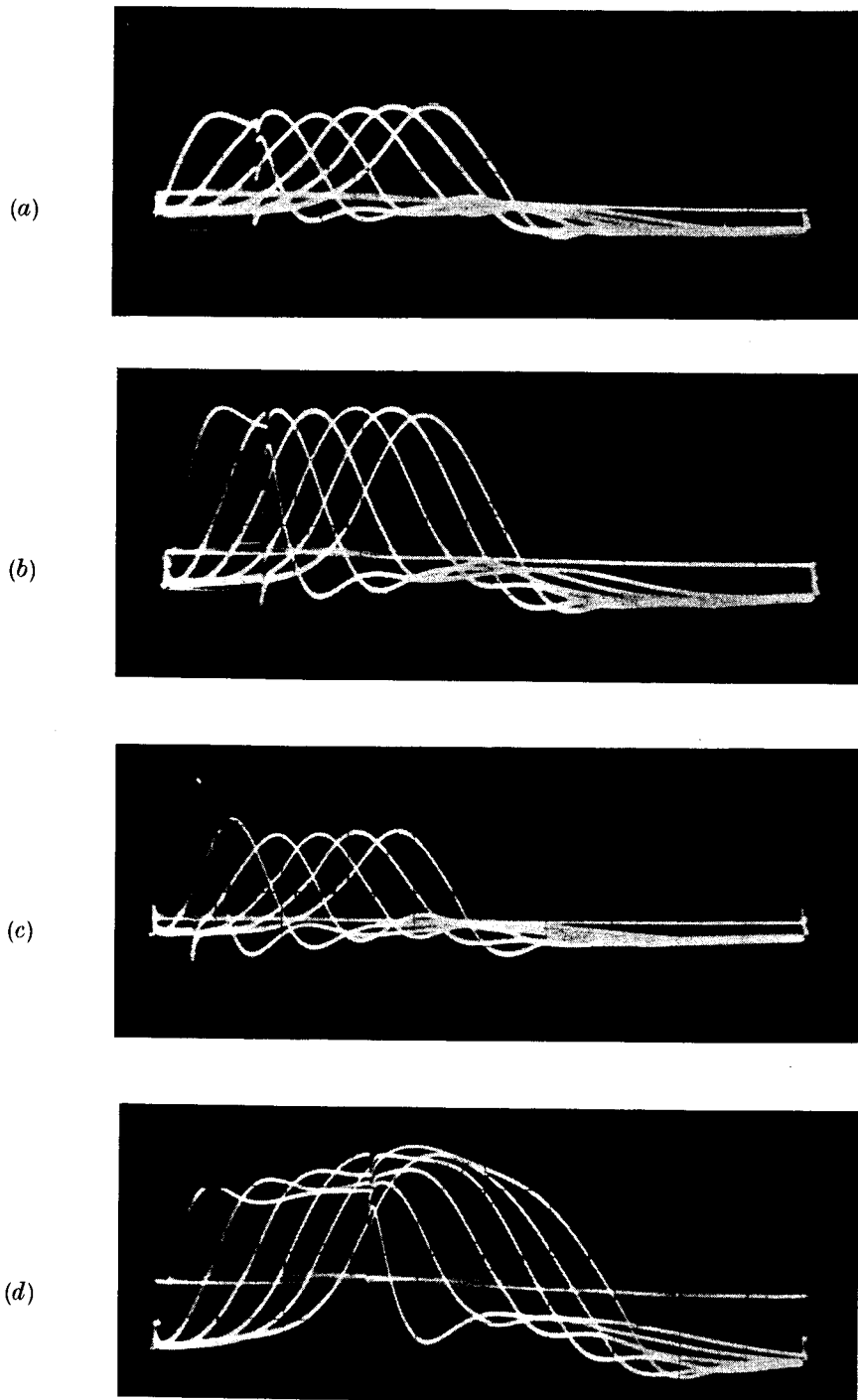
Pulse shaping action in neuristor line with $Z_0=18\ \Omega$, $R_s=120\ \Omega$, $V_b=170\text{ mv}$, for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $5\ \mu\text{sec/div.}$, vertical 50 mv/div.).

Fig. 10



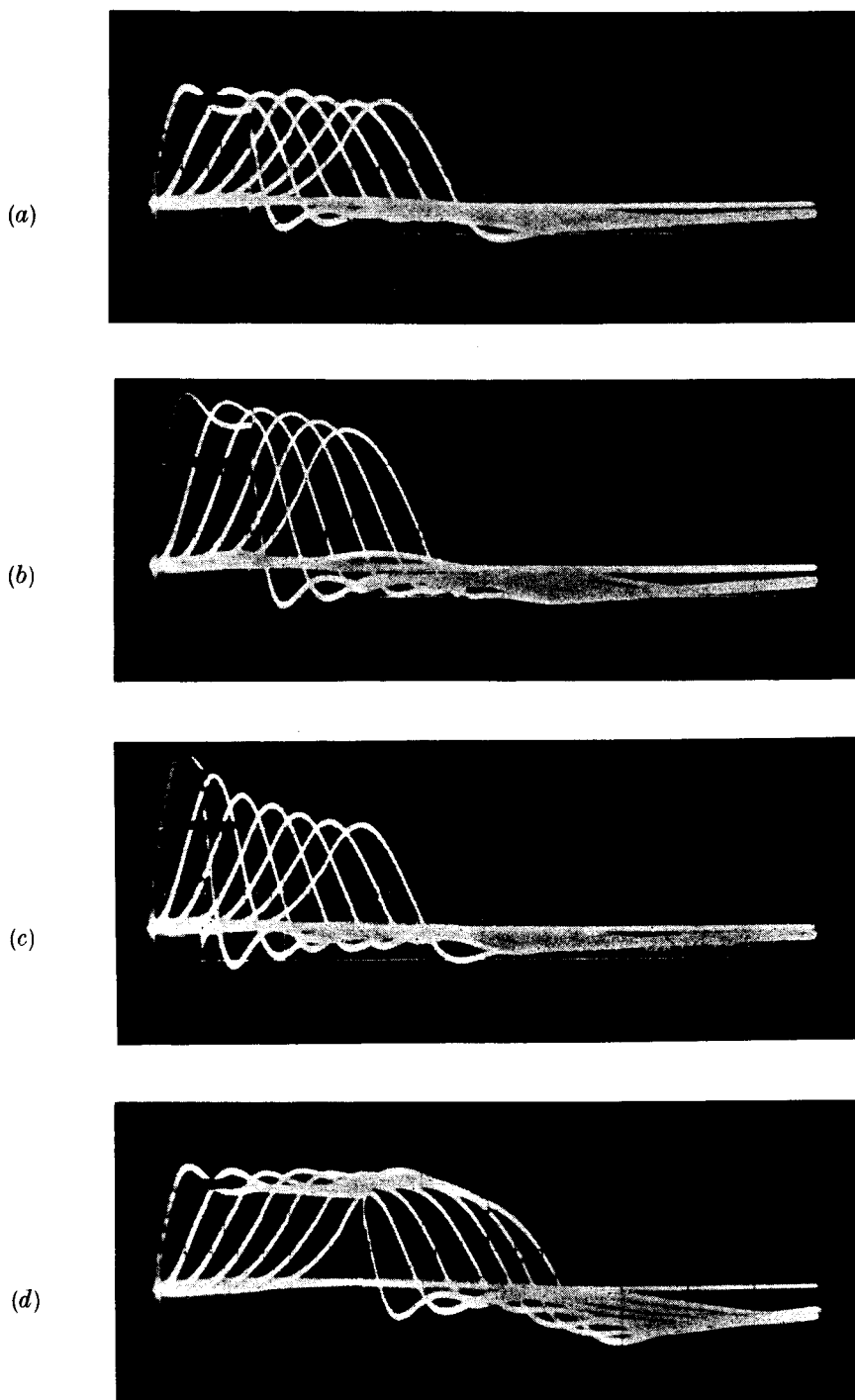
Pulse shaping action in neuristor line with $Z_0=18\ \Omega$, $R_s=120\ \Omega$, $V_b=200\text{ mv}$, for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $5\ \mu\text{sec/div.}$, vertical 50 mv/div.).

Fig. 12



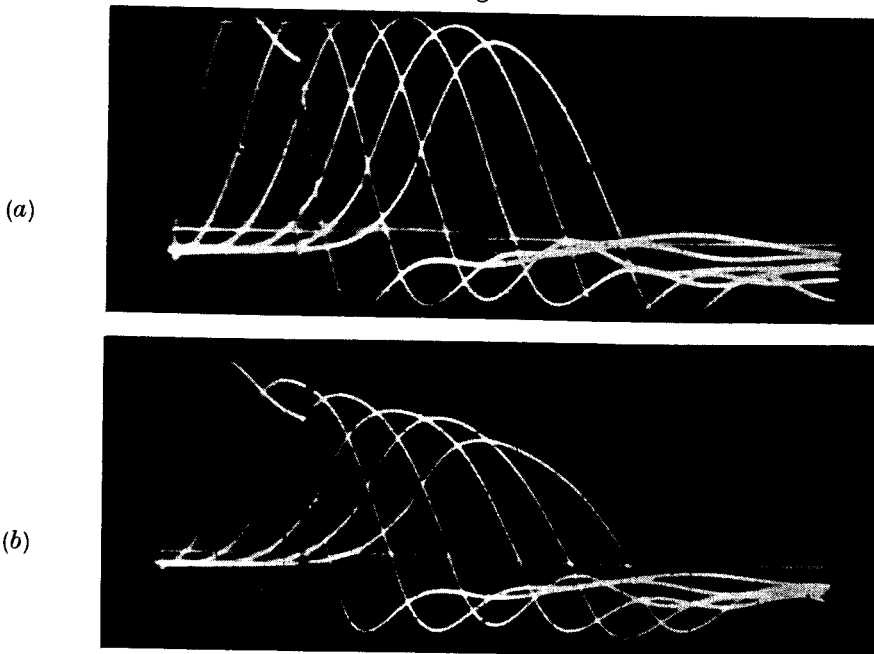
Pulse shaping action in neuristor line with $Z_0 = 11 \Omega$, $R_s = 100 \Omega$, $V_b = \text{high}$, for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $10 \mu\text{sec}/\text{div.}$, vertical $50 \text{ mV}/\text{div.}$).

Fig. 13



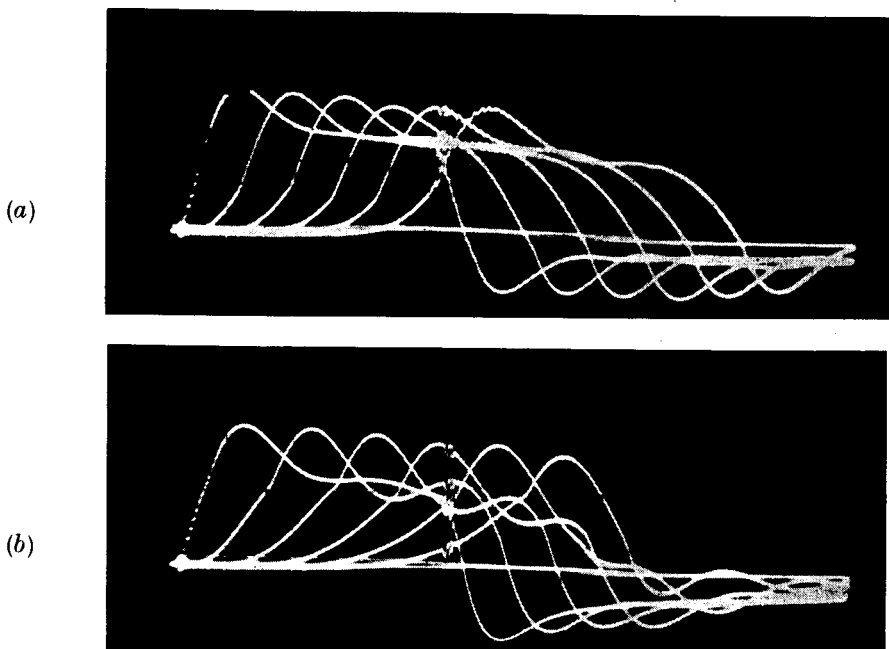
Pulse shaping action in neuristor line with $Z_0 = 11 \Omega$, $R_s = 100 \Omega$, $V_b = 200 \text{ mv}$, for various input pulses. (a) normal, (b) high, (c) narrow, (d) wide (horiz. $10 \mu\text{sec/div.}$, vertical 50 mv/div.).

Fig. 14



Pulse transmission in neuristor line with $Z_0 = 18 \Omega$, $R_s = 100 \Omega$, $I_{\text{sup}} = n \times 1.5 \text{ mA}$.
 (a) for $V_b = 200 \text{ mV}$, (b) for $V_b = 100 \text{ mV}$ (horiz. $5 \mu\text{sec/div.}$, vertical 50 mV/div.).

Fig. 15



Width shaping action in neuristor line with $Z_0 = 100 \Omega$, $R_s = 120 \Omega$, $V_b = \text{high}$ and various thresholds (various supply currents). (a) $I_{\text{sup}} = n \times 1.5 \text{ mA}$, (b) $I_{\text{sup}} = n \times 0.5 \text{ mA}$ (horiz. $1 \mu\text{sec/div.}$, vertical 200 mV/div.).

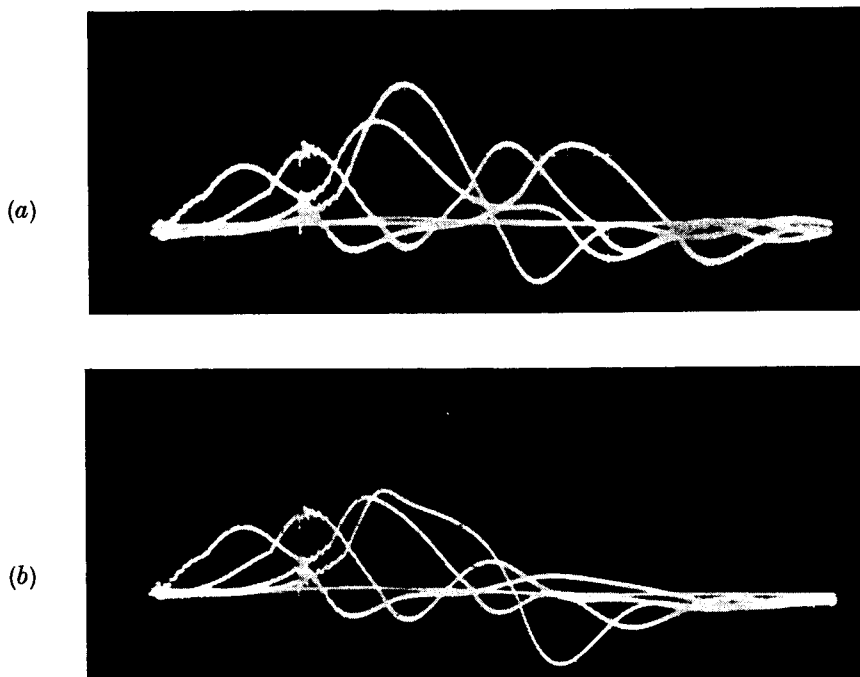
3.3. Refractory period

The refractory period phenomena defined by Crane (1962) and observed in this neuristor model by Hayasaka and Nishizawa (1965) and Nishizawa and Hayasaka (1969) was found to be a result of inductance in voltage supplying circuit L_s . Because the pulse amplitude is even ten times higher than supply voltage, the supply current rapidly decreased. Next follows the recovery period determined by L_s . The supply current increases slowly to the initial value. Yet, in this period the supply current remains lower and the threshold higher. A pulse could not be propagated. With high density of pulse transmission the total supply current decreases about 20%.

3.4. Collision

For all neuristor models in previous studies, the destructive collision phenomenon (Crane 1962) was a result of the refractory period. In this model the destructive collision can exist independent of the refractory period. When resistance R_s was added to the Esaki diode in series the $I-V$ characteristics became flatter in the higher voltage region (fig. 3 c). However, condition (3.1) must be satisfied for sharp threshold action. The pulse amplitude doubles during collision (fig. 16 a). Even with various supply currents the collision is always non-destructive at that instance.

Fig. 16



Pulse collision in neuristor line $Z_0 = 100 \Omega$, $R_s = 120 \Omega$, $I_{sup} = n \times 1.5 \text{ mA}$. (a) non-destructive with double pulse amplitude in collision stage for high V_b , (b) destructive for $V_b = 200 \text{ mV}$ (horiz. $1 \mu\text{sec/div.}$, vertical 200 mV/div.).

When an additional diode is included the power loss for high pulse becomes large (fig. 3 d). It causes a limitation of pulse amplitude. In the collision stage this superposed pulse is followed by remarkable attenuation. As a consequence the pulses, after collision, have a smaller amplitude. If these amplitudes were below the threshold, destructive collision phenomena occurred (fig. 16 b).

Destructive collision has been observed when the following conditions are presented ;

- (1) The threshold is high enough.
- (2) The biased voltage V_b is adequately small.
- (3) The differential conductivity of the parallel diode is adequately dissipating a loss high enough to lower the threshold for high pulse amplitude.

This last condition is especially important for a low impedance line.

As an experimental result, a non-critical condition for differential conductance of parallel diode can be approximately written as :

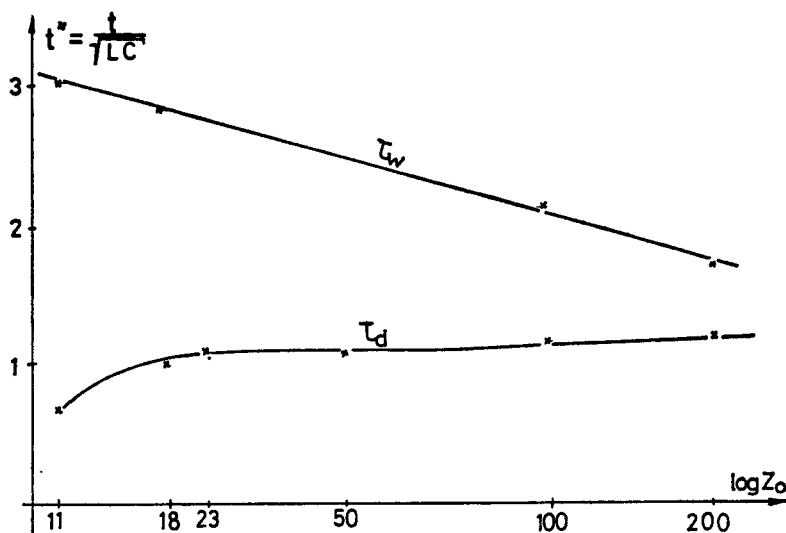
$$\frac{di}{dv} \gtrsim \sqrt{\frac{C}{L}} \quad (3.2)$$

The same formula can be applied for high amplitude pulse shaping action.

3.5. Pulse width

The pulse width, measured in half-maximum amplitude, increased with a decrease of characteristic impedance Z_0 (fig. 17). For $Z_0 = 200 \Omega$ the pulse width $\tau_w = 1.7\sqrt{LC}$ for $Z_0 = 11 \Omega$ is about $3\sqrt{LC}$. Pulses are wider for a low impedance line.

Fig. 17



Pulse width and delay time in respect to time constant $\tau_c = LC$ as a function of characteristic impedance.

3.6. Propagation

Pulse propagation velocity is defined as the number of sections a pulse can pass in a unit of time :

$$n = \frac{1}{\tau_d}, \quad (3.3)$$

where τ_d = delay time per section. The propagation velocity was independent of pulse amplitude, but increased a little with the raising of the threshold, i.e. decreasing supply current.

Delay time can be given by the equation :

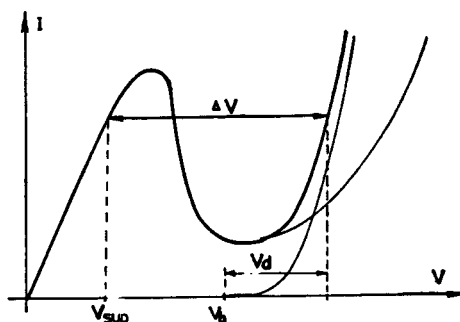
$$\tau_d = \sqrt{LC}; \quad (3.4)$$

however, being dependent it is a little shorter for a low impedance neuristor line (fig. 17). This model had a very high delay time compared with pulse width.

3.7. Pulse height

This was investigated by the measuring of the pulse voltage on the 6th section as a function of the input pulse voltage. The slope of transfer output-input characteristic for high input voltage (fig. 6) is independent both of R_s and V_b , but depends on Z_0 and on the conductivity of the parallel diode. Optimum V_b for various R_s can be easily understood by looking at the characteristics of the NRE (figs. 3 c, 3 d). The constant output amplitude is equal to the difference between the voltage of the high conductance region of the NRE and the supply voltage (fig. 18).

Fig. 18



Characteristic of synthesized negative resistance element (NRE).

Pulse amplitude for a circuit with a parallel diode can be described as ;

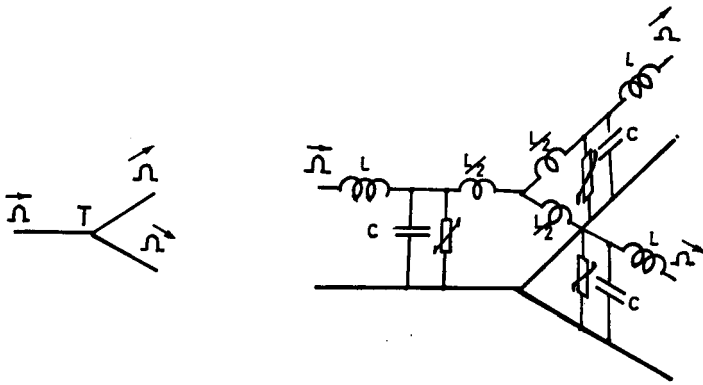
$$\Delta V = V_b + V_d - V_{\text{sup}}, \quad (3.5)$$

where V_b biased voltage,

V_d voltage drop of a parallel diode if in forward direction,

V_{sup} supply voltage.

Fig. 19



T-junction. (a) symbol, (b) circuit diagram.

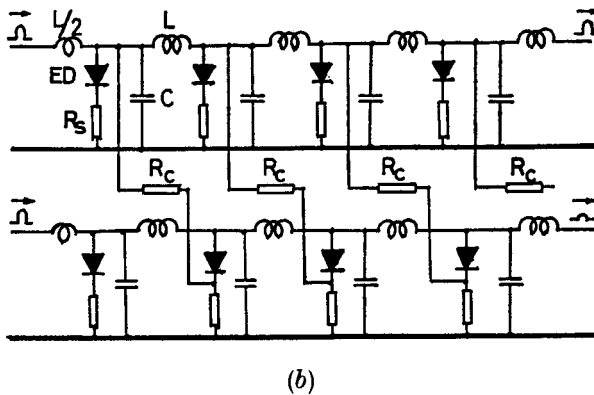
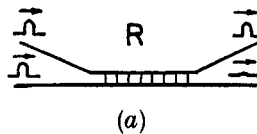
3.8. T-junction

The trigger junction was proposed by Crane (1962). The T-junction of this model is shown in fig. 19. The pulses can propagate in all directions. In the junction the pulse attenuates to about two-thirds of the input amplitude. It follows that, for pulse propagation, the threshold voltage must always be lower than two-thirds of the pulse amplitude.

3.9. R-junction

Refractory junctions (Crane 1960, 1962) are the most complicated elements for neuristor models. Many neuristor models have already been published but the R-junction was proposed only by Crane (1960, 1962) and Cote (1961).

Fig. 20



R-junction. (a) symbol, (b) circuit diagram.

Refractory junction for the model used in this study is shown in fig. 20. The R-junction was made for a low impedance neuristor line with $Z_0 = 11 \Omega$, $R_s = 100 \Omega$, $V_b = 200$ mv. When an equal pulse was applied to both lines the pulse attenuated in only one line (the second). The pulse voltage of the first line through the coupling resistors shifts the bias voltage on the tunnel diodes in the second line. In this way the threshold of the second line is raised. Coupling resistors $R_c = 120 \Omega$ were used but even with very weak coupling $R_c = 150 \Omega$ the threshold in the second line was higher. To observe whether or not the pulse goes above the threshold and also the difference between threshold and pulse height, an oscilloscope input probe was connected to R_s . With three coupling resistors the pulse attenuated to about 0.6 of the input amplitude. In this case the height of the threshold is critically close to the pulse amplitude. To make a good R-junction it is necessary to use many coupling stages or to use a neuristor line with higher loss, i.e. higher attenuation, than the model used in this study. Models with high Z_0 , and the same NRE, have higher attenuation.

4. Theoretical explanation

To understand the theory of this experiment a single section (fig. 27) is considered. The circuit in fig. 21 operates, according to the following equations :

$$\left. \begin{aligned} \frac{L}{2} \frac{di_1}{dt} + R_g i_1 + v - 2V_0 &= 0, \\ \frac{L}{2} \frac{di_2}{dt} + R_L i_2 - v &= 0, \\ C \frac{dv}{dt} + G_n \cdot v + i_2 - i_1 &= 0. \end{aligned} \right\} \quad (4.1)$$

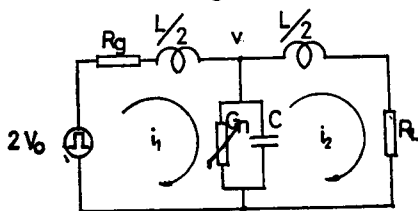
and

This circuit is circumscribed by the 3rd-order differential equation. However, if we put $R_g = R_L = Z_0$ and $i_1 - i_2 = i$ it can be rewritten as :

$$\left. \begin{aligned} 2v + \frac{L}{2} \frac{di}{dt} + Z_0 i &= 2V_0 \\ C \frac{dv}{dt} + G_n v - i &= 0. \end{aligned} \right\} \quad (4.2)$$

These equations can be solved by the graphical method ; either Lienard's or isocline.

Fig. 21



Single section of neuristor line. G_n is non-linear function of voltage.

4.1. Calculation for graphical solution

Introducing a non-linear function which describes the negative resistance element $i_n(v) = G(v)v$ eqns. (4.2) can be written :

$$\left. \begin{aligned} \frac{L}{2} \frac{di}{dt} + Z_0 i + 2(v - V_0) &= 0, \\ C \frac{dv}{dt} + (i - i_n) &= 0. \end{aligned} \right\} \quad (4.3)$$

The slope of trajectory is given as :

$$\frac{di}{dv} = \left(\frac{4C}{L} \right) \frac{V_0 - (Z_0/2) i - v}{i - i_n(v)}. \quad (4.4)$$

To apply Lienard's method it is convenient to put in a new variable :

$$\left. \begin{aligned} i^* &= \frac{Z_0}{2} i = \sqrt{\left(\frac{L}{4C} \right)} i, \\ i_n^* &= \frac{Z_0}{2} i_n = \sqrt{\left(\frac{L}{4C} \right)} i_n. \end{aligned} \right\} \quad (4.5)$$

and

Equation (4.4) can be rewritten as :

$$\frac{di^*}{dv} = \frac{V_0 - i^* - v}{i^* - i_n^*}. \quad (4.6)$$

The trajectories using Lienard's method were plotted on a modified $i^* - v$ plane with $i^* = 1/(2Z_0 i)$ and v as the axis.

4.2. Exciting threshold conditions

To achieve a sharp threshold effect an unstable region on the NRE characteristic must exist. By applying a small signal analysis and the linear theory, we find the condition of the system to be unstable. The circuit is stable, if its characteristic equation has no poles in the right-hand half of the s plane. It will be classified as unstable if it has poles either in the right-hand half of the s plane or on the imaginary axis (Brown and Nilsson 1962).

From eqns. (4.2) we can write the following characteristic equation as :

$$\frac{s^2 \tau_c^2}{2} + s \tau_c \left(1 + \frac{k}{2} \right) + k + 2 = 0, \quad (4.7)$$

where

$$\tau_c = \sqrt{LC}; \quad k = G_n \sqrt{\left(\frac{L}{C} \right)} = \frac{Z_0}{r_n}.$$

From Rout's criterion it can be said that the system will be unstable if

$$\left. \begin{aligned} 1 + \frac{k}{2} &\leq 0 \\ \text{or} \\ k + 2 &\leq 0 \end{aligned} \right\} \quad (4.8)$$

is fulfilled.

The above equation is valid when

$$-\frac{Z_0}{2} < r_n < 0. \quad (4.9)$$

A necessary condition for the exciting threshold is that the absolute value of the negative resistance must be lower than half of the characteristic impedance.

The negative resistance element which is considered must have values limited by :

$$-\frac{Z_0}{2} < r_{nt} + R_s < 0, \quad (4.10)$$

where R_s is the resistance connected in series with the tunnel diode and r_{nt} is the negative resistance of the tunnel diode.

This theoretical result agrees well with the experiments.

4.3. Threshold phenomena

Pulse generation can be achieved if the voltage v on the NRE (fig. 23) can increase enough to reach the unstable region on the NRE characteristic during a pulse transmission. In other words, the threshold will be passed if an instantaneous voltage in the node is higher than the lowest voltage in the unstable region. The region before the unstable region can be approximated by resistor $R_a = V_u/I_p$ (fig. 22) and for a voltage below the threshold the linear theory can be applied. The transfer function for the circuit presented in fig. 23 is given by :

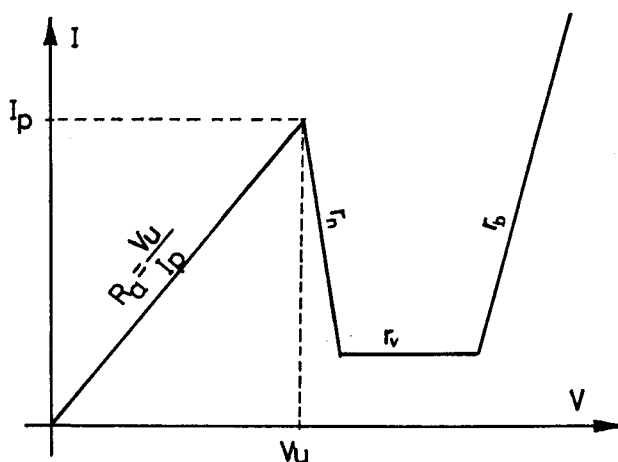
$$v(s) = v_a(s) \frac{\frac{s\tau_c}{2} + 1}{\frac{s^3\tau_c^3}{4} + \frac{s^2\tau_c^2}{2} \left(\frac{k_a}{2} + 1 \right) + s\tau_c \left(\frac{k_a}{2} + 1 \right) + 1}, \quad (4.11)$$

where

$$\tau_c = \sqrt{LC}, \quad k_a = \frac{1}{R_a} \sqrt{\left(\frac{L}{C} \right)} = \frac{Z_0}{R_a}.$$

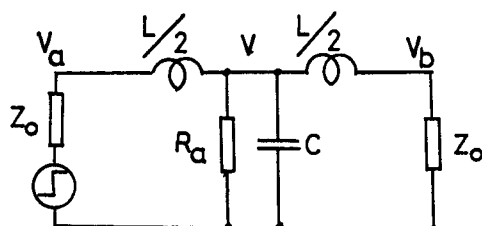
The time response depends on the shape of the input pulse. With step voltage there will be 'ringing' and therefore the threshold will be a little lower. To pass threshold by the pulse with high risk time the amplitude of this pulse must be higher. It should be possible to find an exact solution. In this paper, however, it will be calculated only briefly, seeking the response of a step exciting pulse by the graphical method (Iyer and Sahai 1965).

Fig. 22



Characteristic of NRE approximated by linear segments.

Fig. 23



Single section of neuristor line. NRE is approximated by a resistor.

The threshold voltage is shown in fig. 24 as a function of Z_0 and in fig. 25 as a function of supply current and in fig. 26 as a function of series resistance R_s . The value of the overshoot is equal to the difference in threshold voltage in the 1st and 2nd approximations. The 2nd approximation threshold is lower.

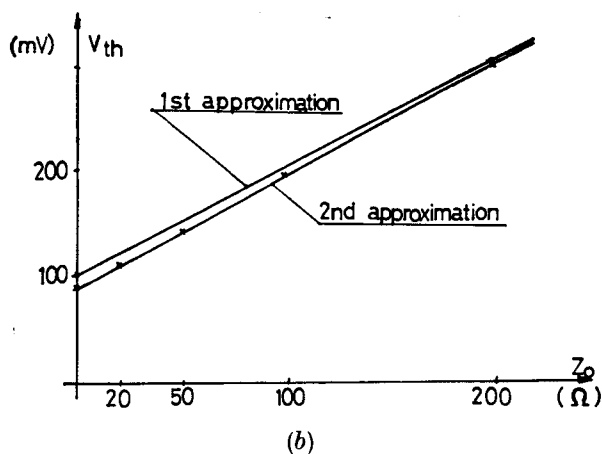
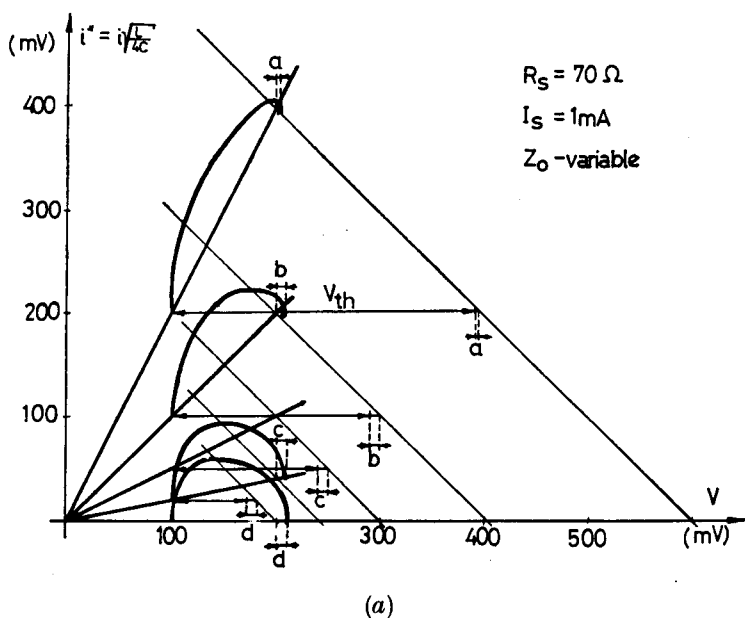
4.4. Shaped pulse height

The trajectories have been drawn graphically for various input step pulse voltages and the crossing point of trajectories and characteristics of NRE has been recorded as output amplitude (fig. 27 a). In this way the characteristic of the height shaping effect for one section was theoretically obtained. The characteristic for n sections was found by simple multiplication of graphical analysis. The result was in rather good agreement with the experiments (fig. 27 b).

4.5. Shaped pulse width

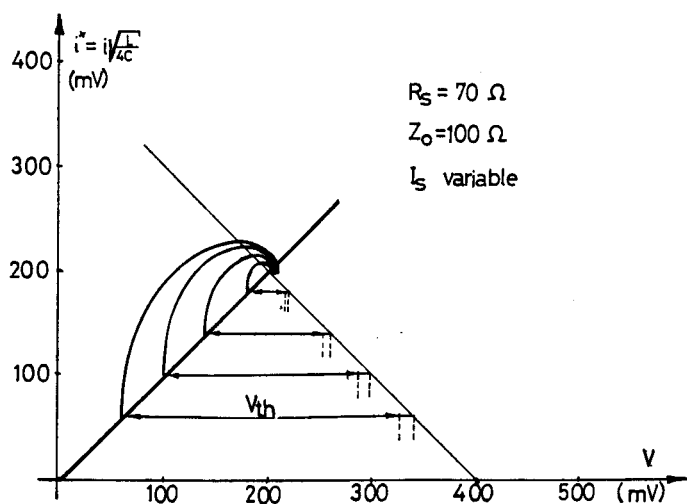
Rectangular pulses with various widths were used as input signals. The trajectory of normal, wide and very wide pulses in neuristor line with $Z_0 = 18 \Omega$

Fig. 24

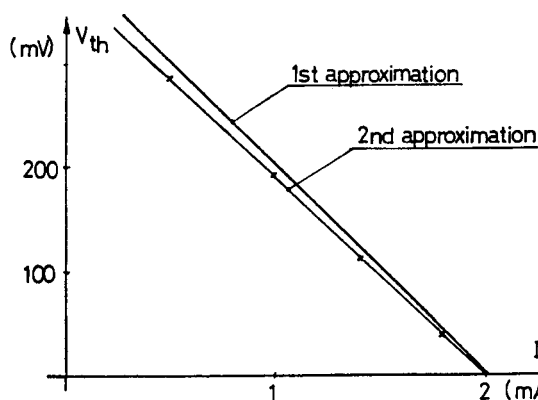


Threshold voltage as a function of Z_0 for step input pulse. (a) graphical representation of various characteristic impedances $Z_0 = 200 \Omega$, 100Ω , 50Ω , 20Ω . (b) graph.

Fig. 25



(a)



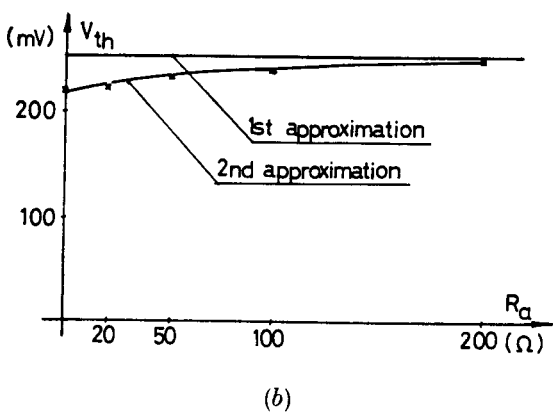
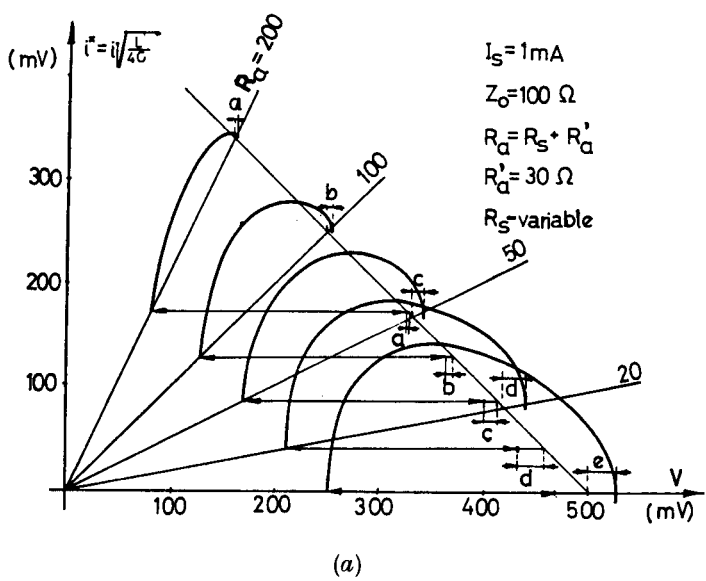
(b)

Threshold voltage as a function of Z_0 for step input pulses. (a) graphical representation for various supply current $I_{sup} = 0.6; 1.0; 1.4; 1.8$ mA, (b) graph.

and $R_s = 100 \Omega$ is shown in fig. 28. The oscillograms with $I-V$ loops for the same cases are presented in fig. 29.

The neuristor under consideration was developed from a lumped parameter delay line by putting some non-linear elements (NRE) in nodes. Resistance of this element is a function of voltage. Without such 'variable resistors' frequency response is like a K-type maximally flat low-pass filter, and shaping action for a wide pulse is impossible. Width shaping action as a result of an overshoot and threshold property can be obtained. For an overshoot there should be some band-pass characteristics.

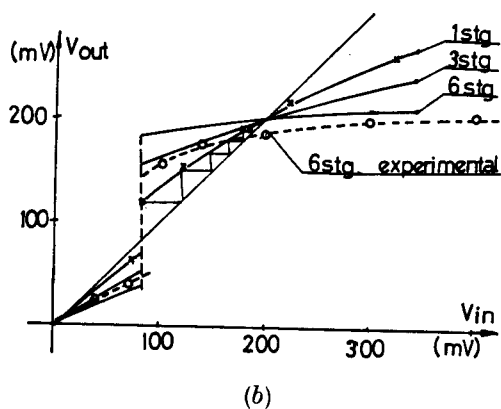
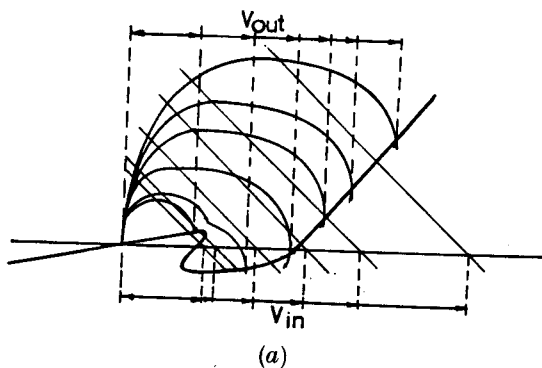
Fig. 26



Threshold voltage as a function of R_a for step input pulses. (a) graphical representation of various R_a , (b) graph.

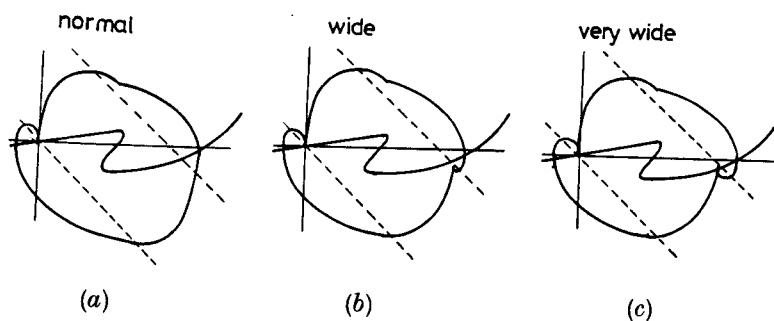
Fig. 27

$$V_b = 200 \text{ mV} \quad R_s = 100 \, \Omega \quad Z_0 = 18 \, \Omega$$



Output-input characteristics. (a) graphical constructions for various amplitude of step input pulse. One section $V_b = 200$ mV, $R_s = 100 \, \Omega$, $Z_0 = 18 \, \Omega$, (b) theoretical and experimental output-input characteristics.

Fig. 28



Graph of I - V loops for rectangular pulses with various widths. (a) normal, (b) wide, (c) very wide.

Fig. 29



(a) normal, (b) wide (1.5 of normal), (c) very wide (2.5 of normal).
Experimental $I-V$ loops for pulses with various widths.

Let us consider a frequency response for the single section loaded by Z_0 (fig. 23). The transfer function is :

$$\frac{V_b}{V_a} = \frac{1}{\frac{s^3 \tau_c^3}{4} + \frac{s^2 \tau_c^2}{2} \left(\frac{k}{2} + 1 \right) + s \tau_c \left(\frac{k}{2} + 1 \right) + 1}, \quad (4.12)$$

where $\tau_c = \sqrt{LC}$ and $k = Z_0/r$.

Absolute value of the transfer function for $s = j\omega$ is :

$$\left| \frac{V_b}{V_a} \right| = \frac{1}{\sqrt{(a_6 \omega^6 + a_4 \omega^4 + a_2 \omega^2 + 1)}}, \quad (4.13)$$

where

$$\left. \begin{aligned} a_6 &= \frac{1}{\sqrt[6]{16}}, \\ a_4 &= \frac{1}{4} \left(\frac{k}{2} + 1 \right) \left(\frac{k}{2} - 1 \right), \\ a_2 &= \left(\frac{k}{2} + 1 \right) \frac{k}{2}. \end{aligned} \right\} \quad (4.14)$$

and

If $a_4 = 0$ and $a_2 = 0$ the Butterford-Wagner condition for maximally flat frequency response is satisfied. It is a low pass filter with modified cut-off angular frequency $\omega_c = \sqrt[6]{16} = 1.59$.

The frequency characteristics are like low band-pass filter, if expression :

$$a_4 \omega^4 + a_2 \omega^2 < 0 \quad (4.15)$$

for any angular frequency $\omega < \omega_c$. The above equation is valid when the condition

$$-2 < k < \frac{2\omega^2}{\omega^2 + 4} \quad (4.16)$$

is fulfilled. This condition makes a width shaping action for a wide pulse possible. From eqn. (4.8) the condition for the existence of an exciting threshold can be written as :

$$k \leq -2. \quad (4.17)$$

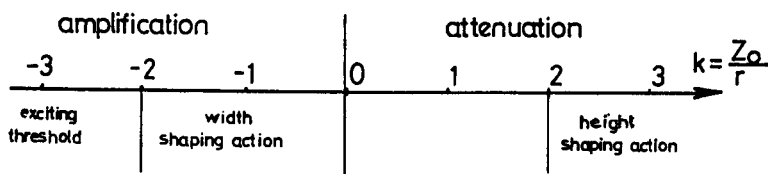
The influence of the parameter k on neuristor action is illustrated in fig. 30.

Remark. Load resistance was assumed as real and equal to Z_0 . It is rather a rough approximation of an infinite line. For a better calculation we should put :

$$Z_0' = Z_0 \sqrt{\left(\frac{s^2 \tau_c}{4} + \frac{s \tau_c}{s \tau_c + k} \right)}. \quad (4.18)$$

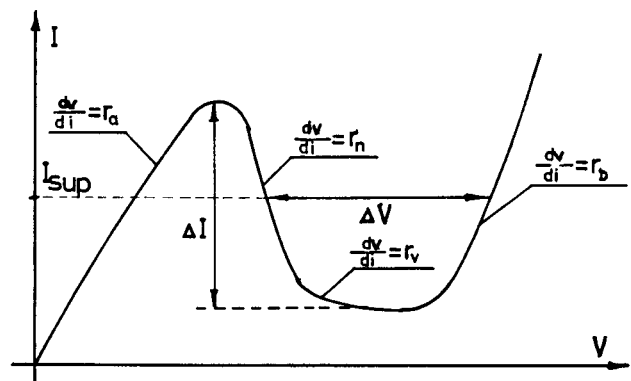
However, in this case also the simple linear theory cannot be used because the parameter $k = Z_0/\tau$ is a function of the pulse voltage.

Fig. 30



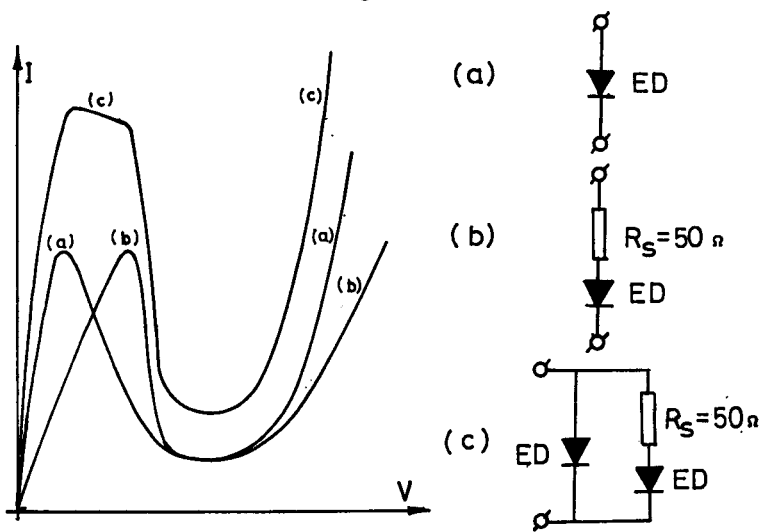
Influence of parameter k on a neuristor action.

Fig. 31



NRE characteristic with illustrated characteristic parameters.

Fig. 32



Synthesized characteristic of NRE using two Esaki diodes.

5. Design for optimum NRE characteristics for low impedance neuristor line

A design for a negative resistance element can be made by looking for optimum conditions for the characteristic parameters. I_{sup} , r_n , r_v , r_a , r_b , ΔV and ΔI . The parameters are illustrated in fig. 31.

From § 4.2 it is known that for an exciting threshold to exist the absolute value of the negative resistance of NRE must be lower than half of the characteristic impedance :

$$|r_n| < \frac{1}{2} \sqrt{\left(\frac{L}{C}\right)}. \quad (5.1)$$

From empirical data (§ 3.4) and theoretical calculation (§ 4.4), we see that the differential resistance of the diode in the high conductance region must be lower than the characteristic impedance :

$$|r_b| < \sqrt{\left(\frac{L}{C}\right)}. \quad (5.2)$$

The supply current should be high enough to obtain a low threshold voltage (fig. 25). For good width shaping action, r_n must have a high negative value (from eqn. (4.17)).

To make R-junction using only a few coupling resistor R_c , the line attenuation must be high for low supply current. It can be obtained using the NRE with a small value of r_a .

The following condition

$$\Delta V_{\text{max}} < \Delta I \cdot Z_0 \quad (5.3)$$

must be satisfied in order to have a clear and sharp threshold. However, if this condition is not satisfied and if the pulse amplitude is a little higher than the threshold, the output voltage will be strongly dependent on the input. (The pulse amplitude was slightly higher than the threshold in most of these experiments.) Equations (5.2) and (5.3) are non-critical. Such an element can be made using a tunnel diode with high peak current. It has a simple structure but also the following faults :

- (1) A high supply current for single section is needed.
- (2) It has a lower frequency operation, which is limited by junction capacitance.

The element presented in fig. 2 does not have these faults but the structure is more complicated. It was constructed for experimental investigation only. For practical use the battery (fig. 2) can be omitted if a parallel diode with the required $I-V$ characteristics is applied. A circuit in which both are tunnel type diodes is possible (fig. 32). From the above calculations the Josephsen tunnelling effect (Scott 1964 and Parmentier 1969) seems to be very useful to achieve a neuristor with an extremely low characteristic impedance.

6. Some considerations for neuristor logic

Crane (1962) described a logic network using neuristor lines with the following properties :

- (1) Constant signal transmission velocity.
- (2) Threshold action.
- (3) Wave form shaping action.
- (4) Destructive collision of pulses.

The neuristor lines were connected by two types of junctions. T (trigger) and R (refractory). Crane's network can be considered to be equivalent to a relay network where T-junctions correspond to connections and R-junctions to relays.

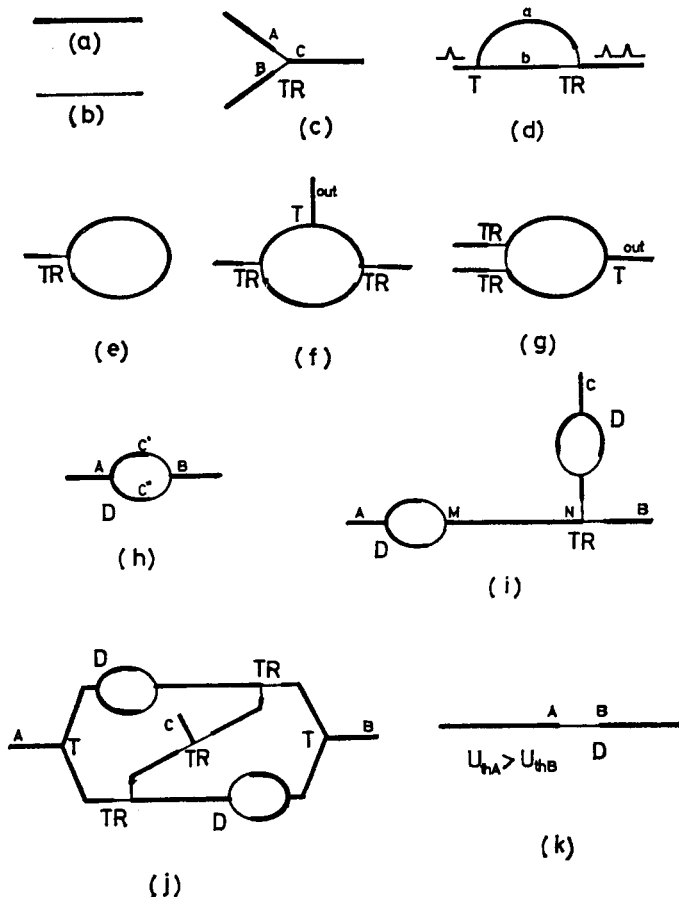
This system can perform the logic function too, even if the 4th condition is not satisfied. However, this condition considerably facilitates the logic design.

It will be shown below that if there are destructive collision phenomena it is possible to realize a logic network using only T-junctions and neuristor lines with various threshold. The R-junction, which is a most complicated element in neuristor logic, is unnecessary.

First, let us consider two kinds of the neuristor lines only.

- (1) With normal threshold (fig. 33 a);
- (2) with very high threshold (fig. 33 b).

Fig. 33



Neuristor logic. (a) neuristor line with normal threshold, (b) neuristor line with high threshold (attenuation line), (c) T-R-junction, (d) pair pulse generator, (e) storage ring, (f) (g) storage ring as memory, (h) neuristor diode, (i) one-directional neuristor gate, (j) two-directional neuristor gate, (k) neuristor diode using line with various thresholds.

Because the second line has attenuation only (i.e. ∞ threshold), it can be a line without active element.

By using a few sections with very high threshold voltage a T-R junction (Crane 1962) can be made (fig. 33 c). The pulse from A and from B arrives at C. But there is no pulse transmission between A and B or B and A, because these two points are separated by two lengths of high threshold (attenuating) lines. By using T and T-R-junctions a pair of pulses can be generated from one pulse. The time between the pulses is proportional to the difference of the length of a and b neuristor lines (fig. 33 d).

Using T and T-R-junctions, a storage ring can be made (fig. 33 e). To stop a circulating pulse it is necessary only to inject a pulse in the reverse direction by means of a similar T-R-junction. The pulses will suffer destructive collision.

The element presented in fig. 33 g can be considered as a memory element with three states :

- (1) Pulse circulates in one direction.
- (2) No circulating pulse.
- (3) Pulse circulates in another direction.

This element can realize flip-flop operation too. One directional propagation can be achieved by building a neuristor diode D (fig. 33 h). The forward direction pulses are joined at B and propagation occurs. The individual reverse direction pulses cannot pass threshold at the points marked C.

Using such diodes and T-R-junctions a gate can be made (fig. 33 i). Pulses from A to B can be propagated only, if there are no trigger pulses from C. If C is triggered the pulses will suffer destructive collision in segment MN.

The gate, which can stop pulses in both directions from A to B and from B to A, is presented in fig. 33 j. This circuit satisfies the junction of Crane's R-junction.

Until now neuristor lines with normal and very high thresholds have been considered. However, the system structure can be made more simple if the neuristors with various thresholds are to be used. The neuristor diode, for example, can be achieved if the threshold voltage in A is higher than in B (fig. 33 k). A pulse can be propagated from A to B only.

It was previously described that the threshold can be changed by a change of supply voltage. In this way the various conditions for pulse propagation can be achieved. In other words the pulses can be amplified or attenuated, depending on the supply voltage. The neuristor line can be considered as an adaptive element. The role of the weights can be played by lines in which attenuation is a function of the supply voltage. In one neuristor network various kinds of logic can be achieved. The learning process can be adapted for this system.

Remark. In this case optimum design of the NRE characteristic must be changed a little.

7. Conclusion

A neuristor line with a characteristic impedance Z_0 as low as 11Ω has been made. The achievement of a neuristor with an even lower impedance is possible. But from experimental data it was found that a decrease of characteristic impedance was accompanied by an increase of pulse width ; yet the

delay time remained almost constant (fig. 17). This means that to obtain the same network logic more single sections of lower impedance neuristor lines must be used. However, this is still better than in the neuristor models with a high refractory period published up to now.

7.1. *Shaping action*

Neuristors with lower Z_0 had smaller effect on width shaping action. For shaping action of the wide pulse, the neuristor line should have a frequency response like a band-pass filter. From this point of view, a system composed of two tunnel diodes (fig. 32) seems better. The neuristor using mutual inductance like m-type filter can be made. The other solution is to use capacitors which have the capacitance given by

$$C_c = 2 \sim 4C \quad (7.1)$$

as the coupling element between parts of the lines. It will be very convenient to use neuristor lines with variable thresholds (i.e. various supply voltage) for adaptive and learning systems.

7.2. *Inductance and frequency response*

The necessity to use inductance would be rather small for such a low impedance neuristor line given by :

$$L_{\min} = Z_0^2 C. \quad (7.2)$$

For stray and junction capacitance $C = C_s + C_j = 10$ pF and $Z_0 = 10 \Omega$ the minimum of unit inductance is 1 nH. But for $Z_0 = 1 \Omega$ this inductance $L_{\min} = 10$ pH only and naturally it has high frequency operation.

7.3. *Refractory period*

A refractory period exists in the actual body's nervous system (Freygang 1959). It is also necessary in some neuristor models in order to have destructive collisions and R-junctions (Crane 1960, 1962, Cote 1961). A refractory period longer than the width of the pulse is an unnecessary condition for logic. However, this condition requires the use of many stages in the neuristor line. From an economic point of view, the rate

$$k_r = \frac{\tau_r}{\tau_d}, \quad (7.3)$$

where τ_r is the refractory time, τ_d delay time, should be as small as possible. To obtain a high delay time per active element it seems possible to use an NRE in every second or third section only, because this neuristor model has a small coefficient of pulse attenuation. To achieve an R-junction using only a few coupling resistors, the attenuation line at a bias point must be high. It can be obtained by using NRE with a small r_a value (fig. 30). This model can also be made as a semi-distributed heterogeneous line. It is very similar to a real nervous axon with many node and internode sections (Fregang 1959). In a completely homogeneous distributed structure, such as that made by

Cote (1965), a width shaping action did not occur because $\tau_0 = \sqrt{LC} \rightarrow 0$. But the heterogeneous distributed neuristor line proposed by Nishizawa (1965, 1969) allows this possibility.

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