Dynamic Scan Clock Control for Test Time Reduction Maintaining Peak Power Limit

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***Abstract*—We dynamically monitor per cycle scan activity to speed up the scan clock for low activity cycles without exceeding the specified peak power budget. The activity monitor is implemented either as on-chip hardware or through pre-simulated and stored test data. In either case a handshake protocol controls the rate of test data flow between the automatic test equipment (ATE) and device under test (DUT). The test time reduction accomplished depends upon an average activity factor α. For low α, about 50% test time reduction is analytically shown. With moderate activity, α = 0.5, simulated test data gives about 25% test time reduction for ITC02 benchmarks. For full scan s38584, the dynamic scan clock control reduced the test time by 19% when fully specified ATPG vectors were used and by 43% for vectors with don't cares. BIST with dynamic clock showed about 19% test time reduction for the largest ISCAS89 circuits in which the hardware activity monitor and scan clock control required about 2-3% hardware overhead.**

***Index Terms*—Scan test, test time reduction, test power, on-chip activity monitor, adaptive test clock**

I. Introduction

Full scan [1], a commonly used method for testing digital VLSI circuits, spends a large fraction of the test time for loading (scan-in) and unloading (scan-out) test data in flip-flops that are chained as shift registers. During this process, random combinational logic activity can produce large unintentional power consumption resulting in power supply noise and heating. If this consumption is higher than that of the normal functional operation for which the circuit is designed [2] the test can cause yield loss [3]. Therefore, scan testing is carried out at a slower speed than the normal operation. The scan clock frequency is determined based on the maximum power consumption the circuit under test can withstand. The power P dissipated at a node is given by [4]:

$$P = \frac{1}{2}CV^2\alpha f \tag{1}$$

where C is the capacitance of the node, V is supply voltage, f is clock frequency and α is a node activity factor.

$$\alpha \; = \; Number\ of\ transitions\ per\ clock\ cycle \tag{2}$$

The activity factor α for a clock signal is 2 because there are two (rising and falling) transitions per cycle. For a combinational node, α ranges between 0 (no transition) and 1 (a toggle every clock cycle). In the worst case, scan clock frequency f_{test} can be based on the maximum activity, i.e., $\alpha = 1$, so that the test power can never exceed the power limit. Therefore,

$$P_{budget} = \frac{1}{2}CV^2 f_{test} \tag{3}$$

where P_{budget} is the maximum power dissipation the circuit can withstand without malfunctioning. Thus,

$$f_{test} = \frac{2P_{budget}}{CV^2} \tag{4}$$

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In general, the worst case assumption of $\alpha = 1.0$ can be relaxed. Although all vector bits are scanned in and scanned out at this frequency, many may not cause the maximum activity. It is possible to scan those in at higher clock frequencies without exceeding the power budget. When the number of transitions in the circuit reduces to a fraction $\frac{1}{i}$ of the maximum,

$$P = \frac{1}{2}CV^2\frac{1}{i}f_{test} \tag{5}$$

From Eq. (3) and Eq. (5),

$$\frac{P}{P_{budget}} = \frac{1}{i} \tag{6}$$

The capacitance and the voltage are constant for a node and so the power is proportional to the product of activity and frequency. Since the circuit can withstand a power P_{budget}, the frequency can be multiplied by i, and the power dissipated in every cycle can still be kept within the allowed limit. Girard [3] defines peak power as the highest energy consumed during one clock period divided by the clock period and the average power as the total energy consumed during test divided by the test time. Since the power must never exceed P_{budget} in any clock cycle, both peak power and average power will be below P_{budget} in spite of the increased shift frequency. Also, instantaneous peak power [3] is consumed right after the application of the clock edge. This power depends on the vectors scanned in and is unaffected by changes in the scan clock frequency. Hence, it can be reduced only by changing the test vectors. In this work we assume that the vectors conform to the instantaneous peak power requirement.

During scan tests, gates are either driven by outputs of the scan flip-flops or by primary inputs. Primary inputs do not change during scan in and scan out. Thus, scan chain activity is a direct measure of the test power and by *monitoring and controlling* this activity, we can speed up the test as well as limit the test power. That is the idea presented in this paper.

Section II discusses previous work on test time optimization. Section III discusses implementations of the proposed technique. Section IV gives a mathematical analysis of the scheme. Section V explains the experimental results obtained. Section VI discusses the conclusion of this work.

II. Previous Work

Many test time reduction methods for scan circuits use compression. In a simple compression technique, the number of scan chains is increased reducing the number of flip-flops per chain. This reduces the time for shifting the input vector bits through scan flip-flops resulting in an overall reduction in test time. However, compression techniques require alterations in the design and may also suffer from linear dependencies.

One compression technique keeps the functionality of the ATE intact by moving the decompression task to the circuit under test [5]. Another technique [6] uses a dynamically

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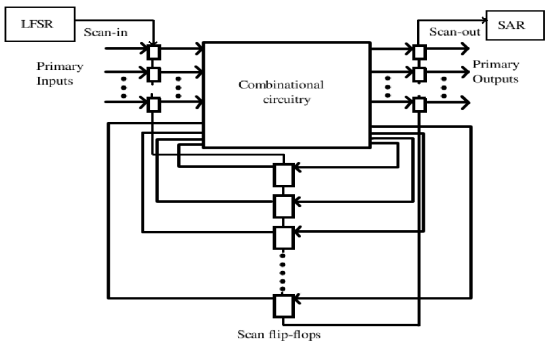


Fig. 1. Test-per-scan built-in self-test (BIST).

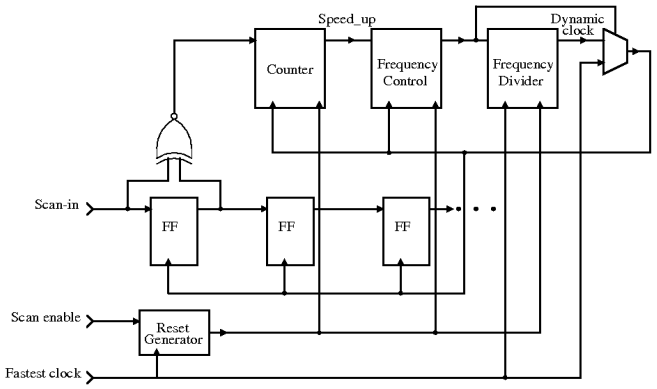


Fig. 2. Schematic of proposed dynamic frequency control.

reconfigurable scan tree that applies a part of the test sequence in scan tree mode and the other part in single scan mode. Reference [7] describes decompression hardware for test pattern compression. References [7] and [8] use compression algorithms with concurrent application of compaction and compression. Reference [9] gives a compression technique with embedded deterministic test logic on chip to provide vectors for the internal scan chains. Reference [10] employs alternating run-length codes [11] for test data compression.

Reference [12] employs a two phase testing strategy where the first phase is a scan-less phase for easy-to-detect faults and the second phase is a scan phase for hard to detect faults. Scan is performed only until all effective test bits are shifted to the right position and until all fault-affected response bits are shifted out. Reference [13] uses genetic algorithms to obtain compact test sets, which limit the scan operations. References [14] and [15] reduce test application time by generating a test for a sequential circuit using combinational test generation and sequential test generation adaptively. Reference [16] proposes a strategy to identify flip-flops to be removed from scan chains to increase the observability of the circuit so that faults activated during scan cycles can be observed at a primary output. The original technique of this paper whose details and some implementations are reported in recent documents [17], [18] can be additionally applied to any scan circuit that may include other methods mentioned above.

III. Implementation

A. BIST circuit with a single scan chain

We add flip-flops at primary inputs and outputs and as shown in Figure 1 connect all flip-flops into a single scan chain. A linear feedback shift register (LFSR), a signature analysis register (SAR) and a BIST controller are added to the circuit to implement the test per scan BIST architecture [16]. BIST vectors are scanned in and combinational outputs are captured through scan flip-flops. Application of a vector includes scanning in LFSR bits into flip-flops, normal mode capture and scan out (overlapped with next scan in) into SAR.

The proposed dynamic frequency control is shown in Figure 2. As test vectors are scanned in, the activity (or inactivity) in the scan chain is monitored at the first flip-flop of the chain. The entering transitions ripple through other flip-flops in subsequent cycles. Inversions along the chain do not change this activity. When a transition passes through an inverting flip-flop, a rising transition becomes a falling transition and vice-versa, leaving the number of transitions unchanged.

An XNOR gate between the input and output of the first flip-flop monitors the activity. The output of the XNOR gate is 0 when a transition enters the scan chain and is 1 when a no transition enters. The XNOR output is fed to a counter, which counts up for each 1, i.e., a non-transition. The counter is set to 0 at the start of every scan in sequence. According to Eq. (6), the scan frequency can be raised as the number of non-transitions entering the scan chain increases. This is accomplished through frequency control and frequency divider blocks in Figure 2. We assume that the response captured from the combinational circuit for the previous vector has a transition density of 1, i.e., the scan chain is filled with alternating 1s and 0s before scan-in begins. This pessimistic worst-case assumption guarantees that the power budget shall not be exceeded. Correspondingly, the scan in of each vector begins with the slowest frequency, f_{test}, permitted by the power budget for $\alpha = 1$. The f_{test} clock is the lowest frequency generated by the frequency divider that divides the frequency of an externally supplied fast tester clock. The frequency control circuit monitors the state of the counter. As the count goes up it lowers the frequency division ratio of the clock divider in several steps.

The reset generator in Figure 2 applies a reset signal to the counter, frequency control block and frequency divider at the positive edge of the scan enable signal, i.e., at the start of scan-in for every combinational vector. Since the frequency divider cannot generate a f/1 (divide by 1) clock, a multiplexer selects either the frequency divider output or the fastest clock.

Let us consider a circuit with 1000 flip-flops. If the slowest scan clock period based on the power budget is 80ns and we raise the frequency in 8 steps, then a modulo 125 (1000/8) counter will be implemented. *Assuming the worst-case activity by the captured states*, every scan-in is started with the 80ns clock and counter set to 0. The count goes up by 1 at every clock in which a non-transition enters the scan chain. When the count reaches 125, the counter is reset and the frequency divider generates a 70ns clock to scan-in the subsequent bits. The counter may again count up to 125 and the clock period would be reduced to 60ns. This process repeats until all 1000 bits are scanned in. Thus, if the input were a series of 1000 1s, the first 125 bits are scanned in at a clock of period 80ns, the second 125 bits at 70ns, until the last 125 bits are scanned in using a clock period 10ns. If the scan-in bits were a series of alternating 0s and 1s, the counter would never count up since there are no non-transitions entering the scan chain and hence the entire scan-in will use the 80ns clock. Notice that due to the *worst-case assumption* we start each scan-in with slowest clock and so the activity monitor only raises the clock rate without ever having to lower it during the same scan-in.

Clearly, a bit stream with fewer transitions will be scanned in faster than one with many transitions. Don‘t cares in deter-

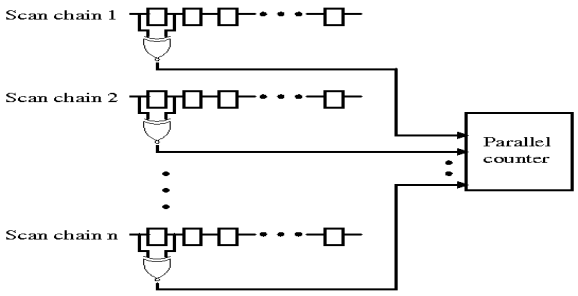


Fig. 3. Dynamic frequency control for multiple scan chains.

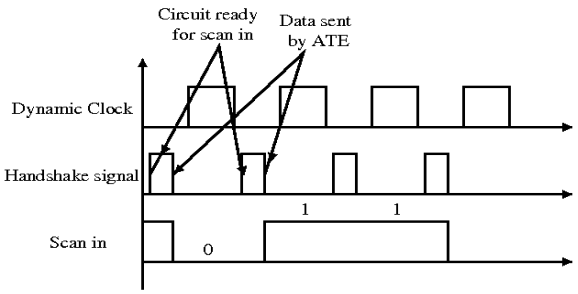


Fig. 4. Handshake protocol between ATE and circuit under test (CUT).

ministic ATPG patterns can be filled in such that the number of transitions is minimum [19]. Also, techniques to generate BIST patterns with low transition densities [20] may be useful. This technique would perform well for such patterns.

B. BIST circuit with multiple scan chains

When the circuit has multiple scan chains, the activity of all chains must be monitored. As shown in Figure 3, XNOR gates are added across the input and output of the first flip-flop in every scan chain. Outputs of XNOR gates are supplied to a parallel counter [21] that counts up by the number of 1s at its input. The rest of the circuitry remains unaltered and still resembles Figure 2. When the count reaches a certain threshold value, the frequency is stepped up and the counter is reset. Except for the use of the parallel counter the control scheme is similar to that in Figure 2.

C. Circuit tested with external ATE

Suppose we perform power analysis through simulation for scan sequences and use that information to scan in vectors at appropriate speeds. Ideally, we may scan in every bit with a customized minimum clock period such that the power dissipated in each clock cycle is pushed up to the maximum limit. Down sides are long simulation runs that must be repeated each time tests are modified and a large amount of per clock information to be stored in the ATE. Since tests are constrained by ATE memory capacity we explore alternatives.

A dynamic control of scan frequency for circuits tested by ATE can be similar to that used in BIST. However, BIST patterns are generated and applied under the control of the same on-chip dynamic clock. When patterns are supplied by an ATE and the activity monitor and dynamic clock control are implemented on the circuit under test (CUT), the CUT must transmit the clock information back to the ATE so that it can send the test data at a continuously changing rate. This problem is similar to that of communication between two systems operating at different clock frequencies. It can be solved by using a handshake protocol [22] that facilitates communication between asynchronous digital systems.

A simple handshake protocol is illustrated in Figure 4. When the circuit is ready to scan in data, a synchronizer, either residing on the chip or on the tester head, toggles a handshake signal. The ATE acknowledges this by scanning in the next bit into the scan-in pin, scanning out the next bit from the scan-out pin and toggling the handshake signal. The synchronizer recognizes the toggle on the handshake signal and accepts the new scan-in bit. This is shown in Figure 5.

We can reduces the hardware overhead required for the dynamic scan clock control if the data on activity is pre-generated by simulation. This data can be used by the test program. Thus, the chip would have an additional input

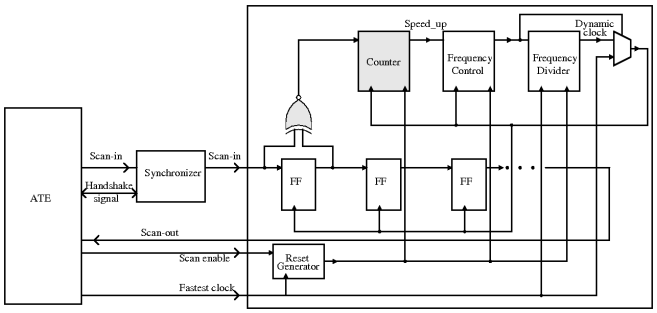


Fig. 5. Dynamic scan clock control for external ATE.

TABLE I
DETERMINATION OF CLOCK CYCLE RANGE FOR DIFFERENT FREQUENCIES.

S. No.	Clock period	Number of non-transitions		Clock cycles	
		Lower limit	Upper limit	Lower limit	Upper limit
1	vT	0	$\lceil \frac{N}{v} \rceil$	0	$\lceil \frac{N}{Av} \rceil$
2	(v-1)T	$\lceil \frac{N}{v} \rceil$	$\lceil \frac{2N}{v} \rceil$	$\lceil \frac{N}{Av} \rceil$	$\lceil \frac{2N}{Av} \rceil$
.	.	.	.	.	.
i	(v-i+1)T	$\lceil \frac{(i-1)N}{v} \rceil$	$\lceil \frac{iN}{v} \rceil$	$\lceil \frac{(i-1)N}{Av} \rceil$	$\lceil \frac{iN}{Av} \rceil$
.	.	.	.	.	.
v	T	$\lceil \frac{(v-1)N}{v} \rceil$	$\lceil \frac{vN}{v} \rceil$	$\lceil \frac{(v-1)N}{Av} \rceil$	$\lceil \frac{vN}{Av} \rceil$

pin (Speed_up) controlling the frequency control block. The frequency control block then receives its input directly from the ATE instead of from the counter. The ATE signals the frequency control block when the activity in the scan chains is low enough to speed up scan shift. This eliminates the XNOR gates at the front end of every scan chain and the counter that monitors the activity.

For circuits with multiple scan chains, an XNOR gate was added at the front end of every scan chain as shown in Figure 3 and a parallel counter monitored the activity and triggered the frequency control block once the activity threshold was reached. If simulation results are used to determine activity, the implementation does not change and the frequency control block that will then be driven directly by the ATE. In both cases, the use of compression does not affect the implementation since activity is monitored in every scan chain.

IV. ANALYSIS

From this point forward, α refers to the activity factor in the scan chain. Let N be the number of flip-flops, A be the non-transition density in the scan chain, $A = 1 - \alpha$, v be the number of frequencies and T be the time period corresponding to the fastest clock. The period of the fastest scan clock is v times shorter than the slowest clock. Therefore, the period of the slowest clock is given by vT. If the vectors were scanned in at the slowest clock, the total scan-in time per vector would

TABLE II
SCAN-IN TIME REDUCTION VS. NUMBER OF SCAN CLOCK SPEEDS FOR ACTIVITY FACTOR $\alpha = 0.5$.

Number of scan clock speeds	Test time reduction (%)		
	Simulation	Eq. (9)	Eq. (11)
1	0.00	0.00	0.00
2	0.34	0.00	0.00
4	12.64	12.50	12.50
8	18.78	18.75	18.75
16	22.03	21.90	21.88
32	23.56	23.48	23.44
64	25.17	24.26	24.22
128	27.41	24.66	24.61

TABLE III
SCAN-IN TIME REDUCTION VS. ACTIVITY FACTOR α FOR 8 SCAN-IN CLOCK SPEEDS.

Activity factor, α	Test time reduction (%)		
	Simulation	Eq. (9)	Eq. (11)
0	43.75	43.75	43.75
0.1	38.63	38.85	38.75
0.2	34.00	33.95	33.75
0.3	28.97	28.99	28.75
0.4	23.51	23.94	23.75
0.5	18.78	18.75	18.75
0.6	14.92	14.04	13.75
0.7	9.60	9.36	8.75
0.8	4.79	4.68	3.75
0.9	0.00	0.00	0.00
1	0.00	0.00	0.00

be NvT. The number of non-transitions in the scan-in bits equals AN. Thus, AN non-transitions occur in N cycles and a non-transition occurs every $\frac{1}{A}$ cycles.

The scan frequency is increased only after the counter counts up to $\frac{N}{v}$. If x is the maximum number of speeds the scan clock will reach within any scan-in sequence, then

$$\frac{N}{v}x = AN \tag{7}$$

$$x = Av \tag{8}$$

The total scan-in time per combinational vector is the sum of all clock periods used. The test time at each frequency is given by the product of the number of cycles run at that frequency and clock period. These values are given in Table I. Total time per vector is given by

$$\sum_{i=1}^{Av}\{\{\lceil\frac{iN}{Av}\rceil - \lceil\frac{(i-1)N}{Av}\rceil\}(v-i+1)T\} \tag{9}$$

where v is usually chosen as a power of 2 because we can design a divide by 2^n frequency divider with n flip-flops. If N was also chosen as a power of 2, the formula reduces to

$$\text{Total time per vector} = \sum_{i=1}^{Av}\{(\frac{N}{Av})(v-i+1)T\}$$

$$= (\frac{N}{Av})(v.Av - \frac{Av(Av+1)}{2} + Av)T \tag{10}$$

Time per vector if a single speed is used is NvT, and

$$\text{Reduction in test time} = \frac{\{NTv - NT(v - \frac{Av+1}{2} + 1)\}}{NTv}$$

$$= \frac{A}{2} - \frac{1}{2v} = \frac{(1-\alpha)}{2} - \frac{1}{2v} \tag{11}$$

A C program was written to generate random vectors for a circuit with 1000 flip-flops. The test time reduction for these vectors was estimated, and compared with the values obtained from the formula. Table II shows the test time reduction versus number of frequencies for an activity factor of 0.5. Table III shows the variation of test time reduction with activity factor when the number of frequencies is 8. Both tables compare the test times estimated for random vectors (column 2), with those obtained from the accurate formula Eq. (9) (column 3) and from the approximate formula Eq. (11) (column 4). Figure 6 shows the test time reduction as a function of the number of frequencies for different values of activity factor. Figure 7 gives the test time reduction as a function of α for different numbers of frequencies.

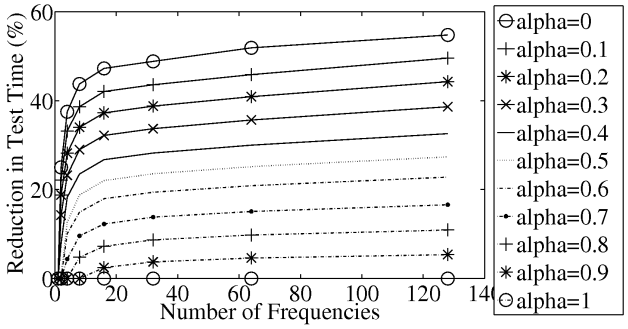


Fig. 6. Test time reduction vs. number of scan clock frequencies.

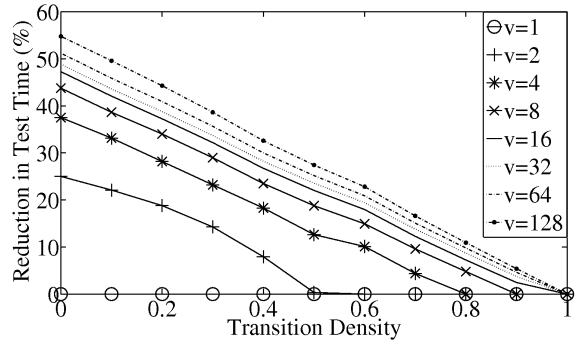


Fig. 7. Test time reduction vs. activity factor for various number of clock frequencies.

Figures 6 and 7 show that for a chosen number of frequencies, vectors with lower activity achieve higher reduction in test time. The test time reduction increases when the number of frequencies increases. The test time initially reduces rapidly for 8 frequencies and after that the reduction is gradual.

V. EXPERIMENTAL RESULTS

In verilog netlists of the ISCAS89 benchmark circuits flip-flops were added at all primary inputs and primary outputs. All flip-flops were converted to scan types and chained together. Thus, the number of flip-flops in the circuit would be the sum of the number of primary inputs, number of primary outputs and number of D-type flip-flops. A 23-bit linear feedback shift register (LFSR), a 23-bit signature analysis register (SAR), and a test-per-scan BIST controller were implemented [23], [24]. A single bit output of the LFSR supplied the scan input and the scan output was fed into the SAR. A suitable number for random patterns to achieve sufficient fault coverage for each circuit [25] was incorporated into the BIST controller. The sequential circuit along with the BIST circuitry was treated as

TABLE IV
REDUCTION IN TEST TIME FOR ISCAS89 CIRCUITS - TEST PER SCAN BIST WITH SINGLE SCAN CHAIN.

Circuit	Number of scan flip-flops	Number of frequencies	Test time reduction (%)	Increase in area (%)
s27	8	2	7.49	14.72
s298	23	4	14.57	16.25
s344	35	4	13.48	15.06
s349	35	4	13.81	13.38
s382	30	4	13.20	12.24
s386	20	4	15.25	15.29
s400	30	4	13.18	11.36
s420	35	4	13.81	13.02
s444	30	4	13.18	11.07
s510	32	4	14.30	7.14
s526	30	4	13.18	11.12
s526n	30	4	13.15	11.34
s641	78	4	13.15	11.81
s713	77	4	12.88	11.86
s820	42	4	13.20	10.69
s832	42	4	13.23	11.10
s838	67	4	13.51	11.73
s953	68	4	13.83	10.60
s1196	46	4	13.24	10.65
s1238	46	4	13.24	10.64
s1423	96	4	13.60	8.77
s1488	33	4	12.61	10.25
s1494	33	4	12.56	10.34
s5378	263	4	13.03	6.65
s9234	286	4	14.01	5.82
s13207	852	8	19.00	3.98
s15850	761	8	18.97	3.23
s35932	2083	8	18.74	2.55
s38417	1770	8	18.83	3.14
s38584	1768	8	18.91	2.13

the core circuit for test time and area analysis. The counter, frequency control circuitry, and frequency divider circuitry for dynamic frequency control were implemented as shown in Figure 2. The number of frequencies for each circuit was chosen according to the size of the circuit or the number of scan flip-flops.

ModelSim from MentorGraphics was used to simulate the circuits with and without the dynamic frequency control circuitry. The time required for test application was recorded in each case. DesignCompiler, a synthesis tool from Synopsys, was used to analyze the area of the circuits with and without the dynamic frequency control circuitry.

Since the LFSR generates pseudo random patterns, the activity factor is about 0.5. From (8), $x = 0.5v$, and hence, the number of frequencies the circuit will run at, is half the chosen number of frequencies. This corresponds to a clock period of $(0.5v + 1)T$ from Table I. However, during power analysis, the next higher frequency is taken into consideration, in order to obtain pessimistic data. Thus, power analysis is done for a clock period of $0.5vT$, i.e., for a clock having twice the lowest frequency. Therefore, the power dissipated by the circuit for an activity factor 0.5 at every node and operating at twice the lowest frequency, was estimated for every circuit. The dynamic frequency control circuitry was included in this analysis.

Table IV shows the results. The number of frequencies chosen for each circuit is shown in column 3. The percentage reduction in test time with respect to the test time for the core circuit is shown in column 4 and the percentage increase in area with respect to the area of the core circuit is shown in column 5. At any node, the capacitance and the voltage are constant. From (1), the power dissipated at any node is proportional to the product of activity and frequency. Thus, the activity per unit time is a direct measure of power dissipated in the circuit. Therefore, an analysis to find activity per unit time was performed on the s386 benchmark circuit. The Synopsys power analysis tool, PrimeTime PX, was used. The activity per unit time in every cycle was found for the circuit for a scan vector with an activity factor of 1. The peak among these values was set as the limit for activity per unit time. The values of activity per unit time of the circuit in every cycle were found for a vector with an activity factor of 0.25 using uniform clock and dynamic clock methods. The results are shown in Figure 8. Notably, the activity per unit time in every cycle is closer to the peak limit when dynamic clock method is used. Also, the peak limit is never exceeded in both methods. A reduction of 11.25% was observed when the dynamic clock method was used.

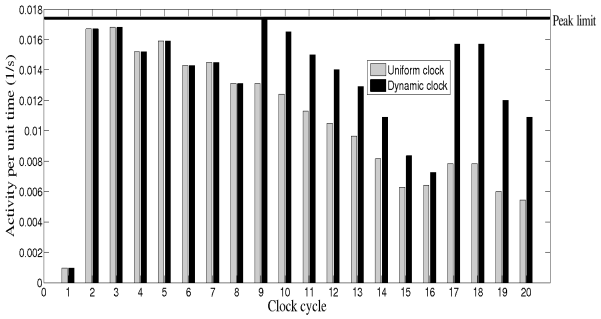


Fig. 8. Activity vs. number of clock cycle for s386 test.

The results for multiple scan chain implementation would be very similar to that obtained for single scan chain. The test time will not vary much since the activity of the circuit will be very similar in both single and multiple chain implementations. However, there would be a marginal increase in area due to the additional XNOR gates at the first flip-flop of every scan chain and also due to the use of a parallel counter as opposed to the simple counter used for the single scan chain.

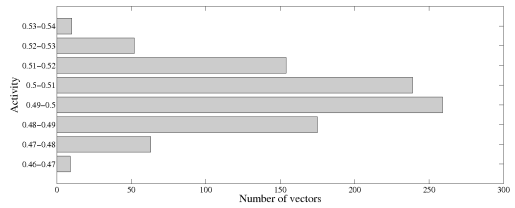
These results for reduction in test time conform to the theoretical results given in Figures 6 and 7. Two trends are clearly observed in Table IV. As circuit size increases, the area overhead drops and test time reduction improves. These circuits are not very large from today's standard and we can expect better results as predicted by the analysis.

To estimate the test time reduction for larger circuits, an accurate mathematical analysis was applied to ITC02 circuits. Test time reduction was computed for best ($\alpha \approx 0$), moderate (α = 0.5) and worst ($\alpha \approx 1$) cases of scan chain activity factors. The test-per-scan BIST was assumed. Table V shows the results. The number of scan flip-flops in column 2 is the sum of number of inputs, number of outputs and number of flip-flops. The number of frequencies for circuits are shown in column 3. The test time reductions achieved for best, moderate and worst case activity factors are shown in Columns 4, 5 and 6, respectively. Evidently, more test time reduction can be achieved in larger circuits. The reduction in test time varies from 0% for patterns causing very high activity to 50% for patterns with almost no activity.

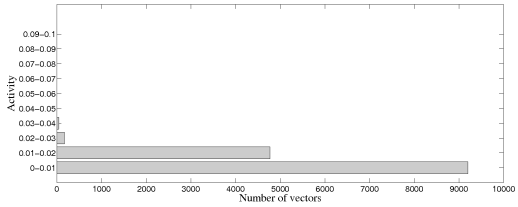
When external tests are used and an ATPG tool generates them, the vectors may have very few care bits. The don't care bits can be filled in using heuristics [26] to minimize scan transitions. Then, a dynamic control of scan clock will provide a large reduction in test time. This is illustrated using the ISCAS89 benchmark s38584. The Synopsys ATPG tool TetraMAX was used to generate two sets of vectors, a set of 961 vectors with no don't care bits and another set of 14,196 vectors with don't care bits. Figure 9 shows the activity vs. number of vectors distributions for the these sets. The vector set without don't cares has an activity factor around 0.5 and the vector set with don't care bits has an activity factor around

TABLE V
REDUCTION IN TEST TIME FOR ITC02 CIRCUITS.

Circuit	Number of scan flip-flops	Number of frequencies	Test time reduction (%)		
			$\alpha \approx 0$	α = 0.5	$\alpha \approx 1$
u226	1416	8	46.68	18.75	0
d281	3813	16	46.74	21.81	0
d695	8229	32	48.28	23.36	0
h953	5586	32	48.32	23.38	0
g1023	5253	32	48.19	23.32	0
f2126	15593	64	49.15	24.18	0
q12710	26158	128	49.45	24.53	0
p22810	29006	128	49.52	24.57	0
p34392	23005	128	49.53	24.57	0
p93791	96916	512	49.72	24.81	0
t512505	76714	512	49.85	24.87	0
a586710	41411	256	49.73	24.77	0



(a) 961 vectors without don't care bits.



(b) 14,196 vectors with don't care bits.

Fig. 9. Distribution of s38584 vectors according to their activity factor.

TABLE VI
REDUCTION IN TEST TIME IN S38584 CIRCUIT

Without don't care bits		With don't care bits	
Number of patterns	Reduction in time (%)	Number of patterns	Reduction in time (%)
961	18.8	14196	43.14

0.01. The don't care bits in the second set were filled using a minimum transition heuristic [26]. Reductions in test time achieved for both test vector sets are shown in Table VI.

In another typical scenario, a test set may initially contain few (say, 10%) high activity ($\alpha = 0.5$) vectors. These resemble fully-specified random vectors and achieve about 70-75% fault coverage. The latter 90% vectors then detect about 20-25% hard-to-detect faults and contain many don't cares, which may be filled in for reduced ($\alpha \leq 0.05$) activity. The adoptive test will be potentially beneficial in such cases.

VI. CONCLUSION

Reduction of test application time in power-constrained testing by adoptively adjusting the scan frequency to the circuit activity is demonstrated. On-chip hardware, whose overhead reduces as the circuit becomes large, provides the adoptive control. Self-test as well as external ATE test can be made adoptive. The technique is particularly beneficial when the peak circuit activity during test is very high but the average activity is quite low.

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