A DSP-Based Ramp Test for On-Chip High-Resolution ADC

Wei Jiang and Vishwani D. Agrawal
Electrical and Computer Engineering, Auburn University, Auburn, AL 36849
weijiang@auburn.edu, vagrawal@eng.auburn.edu

***Abstract*—Ramp test approach is widely used in analog-to-digital converter (ADC) built-in self-test (BIST), which generates linear and slow-slope analog ramp signals intended for histogram-based non-linearity test. The test time can be high for high-resolution ADCs. In this paper, a new DSP-based ramp test approach is presented to address the test time issue. The linear range of signal ramp is divided into two parts and a sum of measured ADC outputs is calculated in each part. Characteristics of ramp signals are derived from the two sums so that time-domain function of the ramp generator can be approximately reconstructed to determine non-linearity error of each ADC measurement. With the obtained testing signal function, non-linearity of each measured code is obtained. A minimal number of samples is required to make sure that quantization errors and the non-linearity of unmeasured code are acceptable. Simulations show that the proposed approach is suitable for quick static test of most on-chip high-resolution ADCs.**

***Index Terms*—BIST, mixed-Signal test, ADC.**

I. Introduction

In recent decades, mixed-signal system-on-chips (SoC) have been widely developed and used in various applications, especially telecommunication devices, replacing separate digital and analog integral circuits (IC) devices. Due to higher level of integration and new advanced deep sub-micron fabrication technology, demands for mixed-signal SoC will continue to grow in the future and more functionality will be integrated onto a single chip for the mixed-signal system to archive even lower total power consumption, higher reliability and reduced manufacturing costs. High resolution analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are required in such mixed-signal devices as interface between analog and digital systems as shown in Figure 1. While analog/mixed-signal device is an important area for designers and developers, mixed-signal testing is becoming the dominant factor of test costs associated with SoC validation [4]. In testing, linearity of converters is critical for determining the overall performance of a mixed-signal device. In particular, the test of high-resolution ADC is among the most challenging and demanding issues for engineers and may have great impact on test time and costs.

Several BIST methods have been developed for testing on-chip ADC, including servo-loop method [2], histogram method [3], and oscillation BIST (OBIST) method [1], etc. The histogram test method is widely used for obtaining a deterministic characterization of ADC by using a signal with known power density function as the test input signal and computing the transfer function of the ADC under test. The coefficients of the transfer function are related to offset, gain and distortion. Various forms of stimulating signals can be used. These typically are ramp signals and sinusoidal signals for easy implementation of signal generators. Several samples of each digital code are measured by ADC under test during BIST stage and the transfer characteristic is determined by comparing measured codes against the expected ones from a presumed ideal converter. An histogram is constructed by counting the number of samples of each code in the measured outputs. A cumulative histogram can also be constructed by counting the number of all samples with codes equal to or less than each measured output.

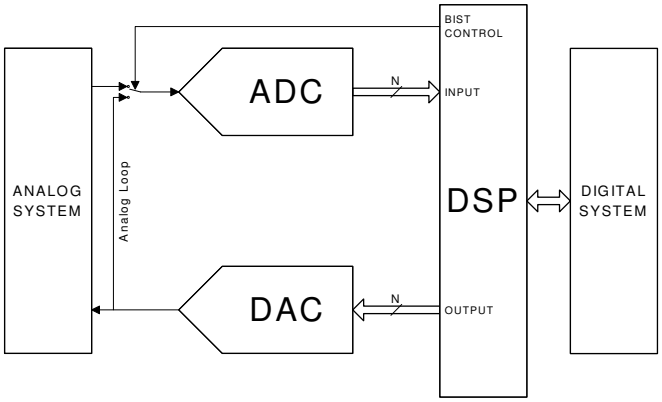

Fig. 1. A typical architecture of mixed-signal system-on-chip (SoC) with high resolution ADC and DAC.

However, it is difficult to apply the histogram testing method to high-resolution ADC because of the large amount of samples to be collected and the long test time that leads to. The method also needs a very slow-slope ramp signal or low-frequency sinusoidal test signals. In BIST, these requirements either are impractical to design or cause high overhead.

In this paper, a new ramp test approach is proposed to solve these BIST issues of high-resolution on-chip ADC. A ramp testing signal is generated to stimulate the ADC under test and the covered range is divided into two parts for later calculation. Measured outputs of each part are accumulated to get two sums and, subsequently, coefficients of time-domain transfer function of ADC are determined by processing the two sums. The time-domain testing signal function is then

978-1-4244-9593-1/11/$26.00 ©2011 IEEE

approximately reconstructed from the determined coefficients and non-linearities of each measured code are obtained. Unlike a conventional histogram method, all possible output codes of the ADC under test do not have to be measured for multiple times in the proposed method. This reduces the test time while the quantization error is reduced by accumulation. For some applications, only a portion of the possible ADC output codes may be measured and the non-linearity errors of the unmeasured codes can be estimated using a third-order polynomial fitting algorithm [5], [6].

II. Background

A. Non-Linearity Errors of ADC

Non-linearity errors of ADC and DAC are measured in terms of the least significant bits (LSB). LSB is the minimal voltage difference between consecutive codes of an ideal ADC or DAC, and 1 LSB is equal to:

$$LSB = \frac{V}{2^N} \tag{1}$$

where V is the full range of the converter with N-bit resolution.

For DAC, each code corresponds to a particular analog signal level and non-linearity errors can be calculated by comparing the measured levels with the expected ideal ones.

Unlike DAC, each code measured by an ADC has two transition edges corresponding to the lower and upper analog signal levels between which ADC outputs the code. Each transition edge represents change of consecutive ADC output codes. Let $\hat{V}_k$ and $\hat{V}_{k+1}$ be lower and upper transition edges of code k, respectively. Thus, $\hat{V}_k$ is the transition edge between code $k-1$ and k. An ideal ADC shall output code k for input analog signal level $v_k = k \cdot LSB$ and therefore the transition edges must be $0.5LSB$ away from v_k so that $\hat{V}_k = vk - 0.5LSB$, $\hat{V}_{k+1} = vk + 0.5LSB$, and

$$v_k = \frac{\hat{V}_k + \hat{V}_{k+1}}{2} \tag{2}$$

Equation (2) can also be applied to non-ideal ADC to calculate center signal level corresponding for each measured code because the transition edges are easy to be detected and measured. Differential non-linearity (DNL) and integral non-linearity (INL) errors can be calculated, respectively, as:

$$\begin{aligned} DNL_k &= \frac{\hat{V}_{k+1} + \hat{V}_{k+2}}{2} - \frac{\hat{V}_k + \hat{V}_{k+1}}{2} - LSB \\ &= \frac{\hat{V}_{k+2} - \hat{V}_k}{2} - LSB \end{aligned} \tag{3}$$

$$\begin{aligned} INL_k &= \sum_{i=0}^{k-1} DNL_k \\ &= \frac{\hat{V}_k + \hat{V}_{k+1}}{2} - v_k \end{aligned} \tag{4}$$

ADC codes 0 and $2^N - 1$ are special as code 0 does not have the lower transition edge and code $2^N - 1$ does not have an upper edge, so the analog signal level corresponding to these two codes cannot be calculated by (2).

B. Histogram Testing Method

Histogram testing method is widely used for determination of non-linearity errors of ADC as an alternative of servo-loop method. The excitation signals for ADC under test can be either a low-slope ramp signal or a low-frequency sinusoidal wave, but usually a ramp signal is used because histogram test with ramp signals (or equivalent triangular signals) is significantly faster than that with sinusoidal signals. When noise figure is comparable to ADC measurement accuracy and all conversion codes need to be tested, ramp histogram testing method is faster than servo-loop testing method and also has lower overhead and testing costs.

The histogram testing method requires an accurate and highly linear ramp signal to correctly test ADC under test. Any non-ideal factors in ramp testing signals, e.g., quantization errors, device parameter variances, or unbalanced elements, will influence the measured ADC output codes and therefore have an impact on the transfer function of ADC. For example, to test a 16-bit ADC to 1/8LSB accuracy requires a ramp with 19 bits of resolution and overall linearity error of better than 2 ppm. A histogram ramp testing of ADC has been proposed [7] for imperfect ramp signals by measuring more samples per code. In a typical case, 14 samples are needed for each code and 10,000 codes in total would then be about 140,000 samples, which require about 140ms to perform the full range testing of an ADC with conversion speed of 1μs.

However, the histogram ramp testing method of this type cannot be easily applied to high-resolution ADCs because of the large amount of possible measured code by such ADCs. Considering in the same typical case, 14 samples are needed for an ADC with 16-bit resolution which has 65,536 possible codes in total and then required testing time is close to 1s. Furthermore, generally a high-resolution ADC is significantly slower than a lower-resolution ADC and thus the required testing time would be much longer if conventional histogram ramp testing method is used.

Assuming an N-bit ADC with converting speed of S samples per second and average K samples per code for a reduced error margin, the total testing time for such an ADC using the histogram method is:

$$T = \frac{K2^N}{S} \tag{5}$$

Very low-slope ramp testing signals are also required to measure each possible code by ADC under test. Ramp signal generator typically consists of a current source (I) and a capacitance (C), and the open loop output voltage is $V = I \cdot t/C$. Further, assuming that the ADC measuring range is V volts, the ramp slope and current are:

$$\begin{aligned} \Delta V &= \frac{V}{T} = \frac{VS}{K2^N} \\ I &= \frac{CV}{T} = \frac{VSC}{K2^N} \end{aligned} \tag{6}$$

Suppose, $V = 3.3$V and $C = 47$pF for a typical design with reasonable testing hardware overhead, the calculated current

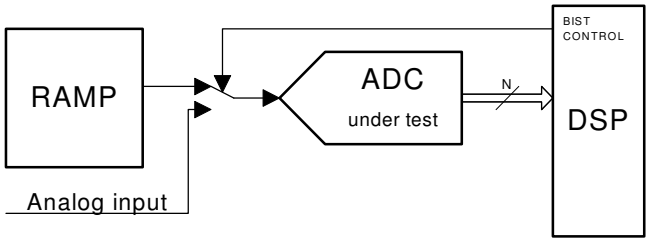

Fig. 2. The proposed ADC BIST architecture.

source is only about 0.15nA from (6), which is comparable to the background noise and hence impractical for real designs. Thus, both situations are unacceptable in most applications.

The errors introduced during a histogram test method are classified into two categories: deterministic errors for inaccuracy and random errors for uncertainty of measured results. The ADC output is a combination of these two kinds of errors. In characterizing ADC by measured results, the deterministic errors can be obtained by calculated coefficients because random errors will be greatly reduced by accumulation of measurements. Therefore, a minimal number of measurements must be determined.

III. Proposed Approach

The proposed approach is shown in Figure 2. Similar to a histogram testing method, this ADC BIST architecture also consists of three major components, a test signal generator, the on-chip ADC under test and a digital signal processor (DSP) for measured data processing and analysis.

Linear ramp testing signals are used to stimulate the ADC under test for simple implementation and short test time. Let the linear ramp signals sampled by the on-chip ADC be,

$$f(k) = a \cdot T \cdot k + b \tag{7}$$

where T is interval time between samples, a and b are coefficients of the linear function ($a > 0$), and k is the variable of samples.

Initially, b is presumed to be close enough to zero so that the measurements always begin with code 0. This condition can be satisfied by the implementation to always reset ramp signal generator to output signal close to zero. If the next sample is still measured as 0 then the previous sample is discarded until a non-zero output code is measured. On subsequent samples the output ascends until the measurement of K-th sample output $f(K)$ reaches $2^N - 1$ which is the maximum possible output code of N-bit ADC. Thus, we have following assumptions for the measured outputs of the ADC under test,

$$M(k)|_{k=0..K} = \begin{cases} 0 & k = 0 \\ M_{ADC}(f(k)) & k = 1..K-1 \\ 2^N - 1 & k = K \end{cases} \tag{8}$$

For an ideal ADC there is no non-linearity error and the ramp testing signals may be reconstructed using

$$f(k) \approx M(k) \cdot LSB + e_q \tag{9}$$

However, it must be noted that quantization errors (e_q) still exists in the reconstructed ramp signal function though the effect of these errors may be reduced by accumulation of a large number of samples as shown below.

Because $M(0)$ and $M(K)$ are the lower and upper bounds for all measurements and their corresponding signals $f(0)$ and $f(K)$ might fall outside ADC measurement range, these two measurement must not be considered during the characterization of the ADC. All other measurements, $M(1)$ through $M(K-1)$, are divided into two equally-sized parts and then accumulated into two sums so that we may get the time-domain functions of ramp testing signals from (9),

$$\begin{aligned} s_0 &= \sum_{k=1}^{K/2} M(k) = \frac{1}{LSB} \cdot \sum_{k=1}^{K/2} f(k) \\ &= \frac{1}{LSB} \cdot \left(\frac{1}{8} K(K+2) aT + \frac{1}{2} Kb \right) \end{aligned} \tag{10}$$

$$\begin{aligned} s_1 &= \sum_{k=K/2}^{K-1} M(k) = \frac{1}{LSB} \cdot \sum_{k=K/2}^{K-1} f(k) \\ &= \frac{1}{LSB} \cdot \left(\frac{1}{8} K(3K-2) aT + \frac{1}{2} Kb \right) \end{aligned} \tag{11}$$

Then, two syndromes can be obtained from the two sums using following equations,

$$S_0 = s_1 - s_0 \tag{12}$$

$$S_1 = -s_1 + 3 \cdot s_0 \tag{13}$$

Applying (10) and (11) to (12) and (13), respectively, we get

$$S_0 = \frac{1}{LSB} \cdot \left(\frac{1}{4} K(K-2) aT \right) \tag{14}$$

$$S_1 = \frac{1}{LSB} \cdot (K(aT+b)) \tag{15}$$

From these two equations, the coefficients of the ramp signal function can be found as,

$$a = LSB \cdot \frac{4S_0}{K(K-2)} \cdot \frac{1}{T} \tag{16}$$

$$b = LSB \cdot \left(\frac{S_1 K - 2S_1 - 4S_0}{K(K-2)} \right) \tag{17}$$

Finally, the two coefficients of time-domain ramp function (7) can be recovered from two sums by applying (12) and (13). Thus,

$$a = LSB \cdot \frac{4(s1 - s0)}{K(K-2)} \cdot \frac{1}{T} \tag{18}$$

$$b = LSB \cdot \frac{(3s_0 - s_1)K - 2(s_0 + s_1)}{K(K-2)} \tag{19}$$

A DSP block, presumed to be available on the mixed-signal SoC, is used to accomplish all computations shown above. The on-chip ADC measures test signals and the DSP reads and processes the ADC output codes. It uses (18) and (19) to approximately reconstruct the original ramp test signal function. The DSP then compares each ADC measurement to the expected code from the reconstructed test signal function to get INL errors of the ADC under test. The two coefficients

can also be used to determine offset errors of the ADC under test.

The principal steps of the proposed BIST approach for on-chip ADC can be described as follows:

1) Reset testing signal generator to output ramp signals.
2) Detect first non-zero output from ADC; all previous samples are discarded.
3) Measure all subsequent samples and record ADC output codes until the maximum possible code are detected.
4) Accumulate measured samples in two equally divided parts and get two sums.
5) Using (18) and (19) obtain approximate coefficients for the signal function.
6) Calculate expected code for each sample using the obtained signal function and compare it to the measured code to get INL errors.

The two coefficients of the test signal function can also be used for a preliminary estimation of INL error of the ADC under test. The absolute value of magnitude of coefficient b indicates overall offset error of ADC and the value of a indicates ramp slope of testing signals. The coefficient b should be around zero because $\|b\| < 0.5LSB$, and a should be close to the design specification of ramp signal generator for ADC under test to pass BIST. If the preliminary conditions are not satisfied, there will be a high probability that that ADC under test is faulty.

The same idea can also be applied when using low-frequency sinusoidal test signals for non-linearity test of an ADC under test. Let a sinusoidal test signal be in the form shown below:

$$f(k) = A\left[1 + \sin\left(\omega T \cdot k - \frac{pi}{2}\right)\right] \tag{20}$$

where $\omega = 2\pi F$ is the frequency of sinusoidal test signal generated, and T is unit time interval of samples. Assuming $f(0)$ is measured zero, $f(1)$ is measured non-zero, and $f(K)$ is the first measured highest possible code, we get $f(K) = A$ and thus, we can get the maximum time interval of sampling given a required minimal number of total samples:

$$T = \frac{\pi}{\omega K} = \frac{1}{2FK} \tag{21}$$

However, the design of such a sine-wave signal generator for ADC is more complicated than that of ramp signal generator because the former requires a stable low-frequency oscillator to generate test signals, a voltage shifter and a low-noise amplifier to move signal voltages to the working range of the ADC.

IV. Implementation and Simulation

The only new component added to a DSP-based mixed-signal system is ramp test signal generator, as shown in Figure 2. Measured samples by ADC under test are processed by DSP to detect non-linearity errors using (18) and (19).

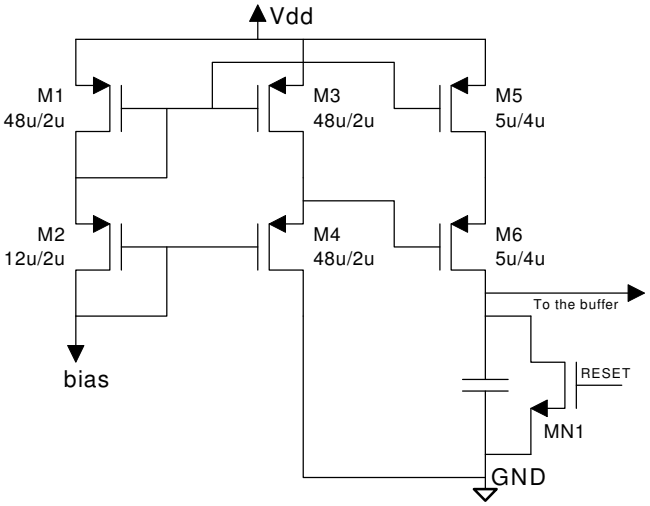

Fig. 3. Design of ramp testing signal generator [8].

A. Ramp Signal Generator

Design of a highly linear ramp signal generator based on MOSFET current mirror is shown in Figure 3 [8]. The slope of the generated ramp signal is slow enough and very linear to allow the static characterization of the entire dynamic range of an ADC under test. To avoid leakage current which is not negligible with extra discharge current through the load, a buffer must be added to the output terminal at the cost of some linear range sacrificed. A switch between output terminal and ground in parallel with ramp capacitor will reset ramp generator to zero and initialize a rising ramp signals for ADC to measure. The W/L ratio of each MOSFET is carefully assigned for low ramp slope. Suppose bias current is I and voltage drop over M1 is $\Delta V + V_{th}$, the mirror current through M3/M4 is also I and that through M5/M6 is $I/30$, and voltage drop through M5 is ΔV. So, the generated linear ramp signal is in the range of 0 though $V_{DD} - \Delta V$.

B. Minimal Number of Samples

Since measurements by ADC always contain quantization errors owing to its nature to convert continuous analog wave into discrete digital code, a minimal number of samples must be taken to ensure that such quantization errors are negligible in the process. Let us first consider an ideal ADC. The quantization errors of the ideal ADC can be anywhere between $\pm\frac{LSB}{2}$, and as more samples ADC measures less quantization errors remain after accumulating all measurements. A histogram approach can be considered as the extreme situation of the requirements, which needs multiple samples for each code to make sure that the quantization error is essentially removed from statistical distribution of codes.

However, for a non-ideal ADC under test, there are two possibilities that must be taken into consideration. It is always possible that some codes with greater non-linearity errors are not measured during BIST, and also it is possible that

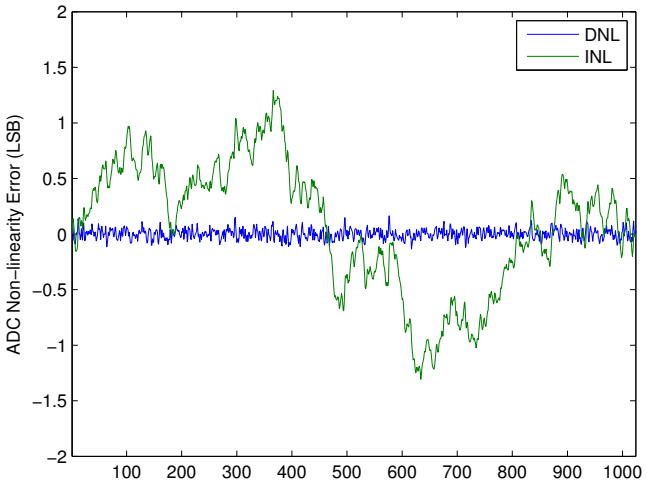

Fig. 4. Simulation results with 10-bit flash ADC.

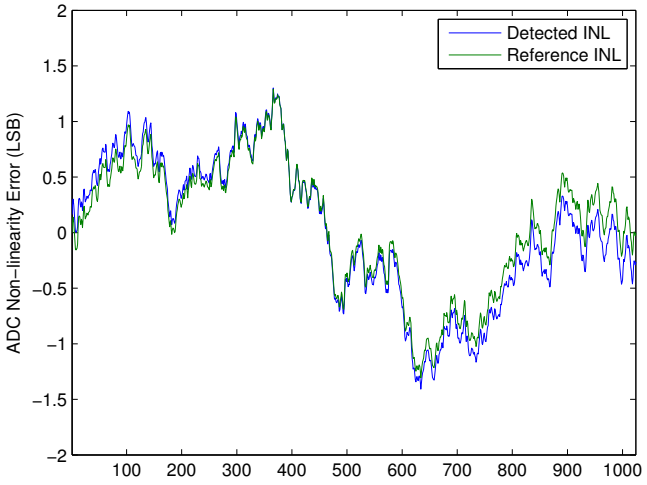

Fig. 5. Detected non-linearity errors using reconstructed transfer functions of ramp signals.

a measured non-linearity error introduces distortion to the reconstructed transfer function of ramp signals.

Generally, the first problem will be non-existent if every code is measured at least once, and the second problem will be effectively eliminated with large number of samples because such non-linearity errors will be attenuated to make little impact on the calculation. In practice, we found that at least 2^{N-2} samples should be measured to perform this BIST procedure on an N-bit ADC to avoid these two issues and ensure that ramp signals are reconstructed properly.

C. Simulation Results

A 10-bit flash ADC model is used for simulation to demonstrate non-linearity errors due to process variation. Figure 4 shows the simulation result for the 10-bit flash ADC with non-linearity errors. All samples are divided into two sections and the coefficients of reconstructed transfer function are calculated by (18) and (19), which in this case are $aT = 1.0004166157$ and $b = -0.6635025532$, respectively. After ramp signals are reconstructed, each measured sample will be compared against the calculated result from the transfer function to detect non-linearity errors. Comparison between detected non-linearity errors by this transfer function and calculated ones is shown in Figure 5.

V. Conclusion

In this paper a new non-linearity BIST method for high-resolution on-chip ADC is proposed. This technique greatly reduces the test time of a conventional histogram approach. Only a portion of all possible ADC digital output codes is measured in this method, so a series of ramp testing signals is used to stimulate ADC under test and the measured samples are divided into two sections for processing. Two syndromes are therefore obtained from the two sections to reconstruct transfer function of the ramp signal and then all non-linearity errors of measured samples can be calculated. To reduce the effects of quantization errors of measured samples and make sure that there are no non-linearity errors in the unmeasured ADC codes, certain minimal number of samples is required.

Acknowledgment: This research was supported in part by the National Science Foundation Grant CNS-0708962 and by the Wireless Engineering Research and Education Center at Auburn University.

References

[1] K. Arabi and B. Kaminska, "Efficient and Accurate Testing of Analog-to-Digital Converters Using Oscillation-Test Method," in *Proceedings of the 1997 European conference on Design and Test*, 1997, pp. 348–352.

[2] F. F. Dai and C. E. Stroud, *Analog and Mixed-Signal Test Architectures*, chapter 15. Morgan Kaufmann, 2008.

[3] J. Doernberg, H.-S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 820–827, Dec. 1984.

[4] http://www.itrs.net/Links/2007ITRS/Home2007.htm, "International technology roadmap for semiconductors," 2007.

[5] W. Jiang and V. D. Agrawal, "Built-in Self-Calibration of On-Chip DAC and ADC," in *Proc. IEEE International Test Conference*, Oct. 2008. Paper No. 32.2.

[6] W. Jiang and V. D. Agrawal, "Designing Variation-Tolerance in Mixed-Signal Components of a System-on-Chip," in *Proc. IEEE International Symposium on Circuits and Systems*, 2009, pp. 126–129.

[7] S. Max, "Ramp Testing of ADC Transition Levels using Finite Resolution Ramps," in *Proc. IEEE International Test Conference*, 2001, pp. 495–501. Paper No. 18.1.

[8] J. Wang, E. Sanchez-Sinencio, and F. Maloberti, "Very Linear Ramp-Generators for High Resolution ADC BIST and Calibration," in *Proc. 43rd IEEE Midwest Symp. on Circuits and Systems*, Aug. 2000, pp. 908–911.