Dynamic Scan Clock Control in BIST Circuits

Priyadharshini Shanmugasundaram and Vishwani D. Agrawal
Auburn University
Auburn, Alabama 36849
pzs0012@auburn.edu, vagrawal@eng.auburn.edu

Abstract—We dynamically monitor per cycle scan activity to speed up the scan clock for low activity cycles without exceeding the specified peak power budget. The activity monitor is implemented as on-chip hardware. Two models, one for test sets with peak activity factor of 1 and the other for test sets with peak activity factor lower than 1 have been proposed. In test sets with peak activity factors of 1, the test time reduction accomplished depends upon an average activity factor of α_{in}. For low α_{in}, about 50% test time reduction is analytically shown. With moderate activity, α_{in} = 0.5, simulated test data gives about 25% test time reduction for ITC02 benchmarks. BIST with dynamic clock showed about 19% test time reduction for the largest ISCAS89 circuits in which the hardware activity monitor and scan clock control required about 2-3% hardware overhead. In test sets with peak activity factors lower than 1, the test time reduction depends on an input activity factor of α_{in} and an output activity factor of α_{out}. For low α_{in} and high α_{out}, a test time reduction of about 50% is analytically shown.

Index Terms—Scan test, test time reduction, test power, on-chip activity monitor, adaptive test clock, activity factor, BIST.

I. INTRODUCTION

Scan testing [1] spends a large fraction of the test time for loading (scan-in) and unloading (scan-out) test data in flip-flops that are chained as shift registers. During this process, random combinational logic activity can produce large unintentional power consumption resulting in power supply noise and heating. If this consumption is higher than that of the normal functional operation for which the circuit is designed the test can cause yield loss [2]. Therefore, scan testing uses a slower speed than the normal operation. The scan clock frequency is determined based on the maximum power consumption the circuit under test can withstand. The power P dissipated at a node is given by [2]:

$$P = \frac{1}{2}CV^2\alpha f \qquad (1)$$

where C is the capacitance of the node, V is supply voltage, f is clock frequency and α is a node activity factor.

$$\alpha = Number\ of\ transitions\ per\ clock\ cycle \qquad (2)$$

The activity factor α for a clock signal is 2 because there are two (rising and falling) transitions per cycle. For a combinational node, α ranges between 0 (no transition) and 1 (a toggle every clock cycle). In the worst case, the frequency of the scan clock can be based on the maximum activity, i.e., $\alpha = 1$, so that the test power can never exceed the power limit. Therefore,

$$P_{budget} = \frac{1}{2}CV^2 f_{test} \qquad (3)$$

where f_{test} is the scan clock frequency and P_{budget} is the maximum power dissipation the circuit can withstand without malfunctioning. Thus,

$$f_{test} = \frac{2P_{budget}}{CV^2} \qquad (4)$$

In general, the worst case assumption ($\alpha = 1.0$) can be modified for any value. Although all vectors are scanned in and scanned out at this frequency, many may not cause the maximum activity. It is possible to scan in these vectors at higher clock frequencies without exceeding the power budget. When the number of transitions in the circuit reduces to a $\frac{1}{i}$ of the maximum,

$$P = \frac{1}{2}CV^2\frac{1}{i}f_{test} \qquad (5)$$

From (3) and (5),

$$\frac{P}{P_{budget}} = \frac{1}{i} \qquad (6)$$

The capacitance and the voltage are constant for a node and so the power is proportional to the product of activity and frequency. Since the circuit can withstand a power P_{budget}, the frequency can be multiplied by i, and the power dissipated in every cycle can still be kept within the allowed limit. Girard [2] defines peak power as the highest energy consumed during one clock period divided by the clock period and the average power as the total energy consumed during test divided by the test time. Since the power must never exceed P_{budget} in any clock cycle, both peak power and average power will be below P_{budget} in spite of the increased shift frequency. Also, instantaneous peak power [2] is consumed right after the application of the clock edge. This power depends on the vectors scanned in and is unaffected by changes in the scan clock frequency. Hence, it can be reduced only by changing the test vectors. In this work we assume that the vectors conform to the instantaneous peak power requirement.

During scan tests, gates are either driven by outputs of the scan flip-flops or by primary inputs. Primary inputs do not change during scan in and scan out. Thus, scan chain activity is a direct measure of the test power and by *monitoring and controlling* this activity, we can speed up the test as well as limit the test power. That is the idea presented in this paper.

Section II discusses previous work on test time optimization. Section III discusses implementations of the proposed technique. Section IV gives a mathematical analysis of the scheme. Section V explains the experimental results obtained. Section VI discusses the conclusion of this work.

II. PREVIOUS WORK

Many test time reduction methods for scan circuits use compression. In a simple compression technique, the number of scan chains is increased reducing the number of flip-flops per chain. This reduces the time for shifting the input vector bits through scan flip-flops resulting in an overall reduction in test time. However, compression techniques require alterations in the design and may also suffer from linear dependencies.

One compression technique keeps the functionality of the ATE intact by moving the decompression task to the circuit under test [3]. Another technique [4] uses a dynamically reconfigurable scan tree that applies a part of the test sequence in scan tree mode and the other part in single scan mode. Reference [5] describes a decompression hardware scheme for test pattern compression. References [5] and [6] use compression algorithms with concurrent application of compaction
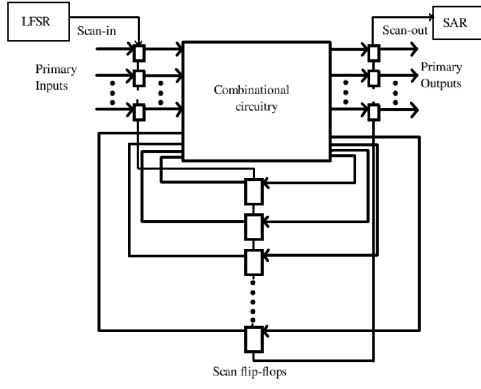
Fig. 1. Test-per-scan built-in self-test (BIST).

Fig. 2. Schematic of proposed dynamic frequency control.

and compression. Reference [7] implements a compression technique with embedded deterministic test logic on chip to provide vectors for the internal scan chains. Reference [8] employs alternating run-length codes [9] for test data compression.

Reference [10] employs a two phase testing strategy where the first phase is a scan-less phase for easy-to-detect faults and the second phase is a scan phase for hard to detect faults. Scan is performed only until all effective test bits are shifted to the right position and until all fault-affected response bits are shifted out. Reference [11] uses genetic algorithms to obtain compact test sets, which limit the scan operations. References [12] and [13] reduce test application time by generating a test for a sequential circuit using combinational test generation and sequential test generation adaptively. Reference [14] proposes a strategy to identify flip-flops to be removed from scan chains to increase the observability of the circuit so that faults activated during scan cycles can be observed at a primary output. The technique proposed in this paper can be applied to any scan circuitry, and can be used in addition to many of the methods mentioned above.

III. IMPLEMENTATION

A. BIST circuit with a single scan chain

We add flip-flops at primary inputs and outputs as shown in Figure 1 and connect all flip-flops into a single scan chain. A linear feedback shift register (LFSR), a signature analysis register (SAR) and a BIST controller are added to the circuit to implement the test per scan BIST architecture [14]. BIST vectors are scanned in and combinational outputs are captured through scan flip-flops. Application of a vector includes scanning in LFSR bits into flip-flops, normal mode capture and scan out (overlapped with next scan in) into SAR. The proposed dynamic frequency control is shown in Figure 2. The shaded parts of the circuit are not used for this implementation. As test vectors are scanned in, the activity (or inactivity) in the scan chain is monitored at the first flip-flop of the chain. The entering transitions ripple through other flip-flops in subsequent cycles. This activity does not change if there are inversions in the chain. When a transition passes through an inverting flip-flop, a rising transition becomes a falling transition and vice-versa, leaving the number of transitions unchanged.

An XNOR gate between the input and output of the first flip-flop monitors the activity. The output of the XNOR gate is 0 when a transition enters the scan chain and is 1 when a non-transition enters. The XNOR output is fed to a counter, which counts up for each 1, i.e., a non-transition. The counter is set to 0 at the start of every scan in sequence. According
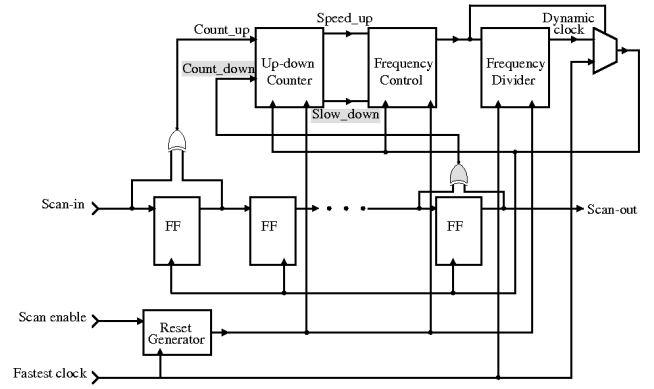
to (6), the scan frequency can be raised as the number of non-transitions entering the scan chain increases. This is accomplished through frequency control and frequency divider blocks in Figure 2. We assume that the response captured from the combinational circuit for the previous vector has a transition density of 1, i.e., the scan chain is filled with alternating 1s and 0s before scan-in begins. This pessimistic worst-case assumption guarantees that the power budget shall not be exceeded. Correspondingly, the scan in of each vector begins with the slowest frequency, f_{test}, permitted by the power budget for $\alpha = 1$. The f_{test} clock is the lowest frequency generated by the frequency divider that divides the frequency of an externally supplied fast tester clock. The frequency control circuit monitors the state of the counter. As the count goes up it lowers the frequency division ratio of the clock divider in several steps.

The counter states at which the clock is sped up can be found by simulation, which establishes correlation between the circuit activity and scan chain activity. If each transition in the scan chain causes a large number of transitions in the circuit, power consumption reaches large values for low scan chain transition numbers. Thus, a large number of scan chain non-transitions should be counted before the scan clock frequency is stepped up. Similarly, if a transition in the scan chain has a small effect on the circuit activity, then only a few non-transitions in the scan chain are sufficient to increase the scan clock frequency.

The reset generator in Figure 2 applies a reset signal to the counter, frequency control block and frequency divider at the positive edge of the scan enable signal, i.e., at the start of scan-in for every combinational vector. Since the frequency divider cannot generate a f/1 (divide by 1) clock, a multiplexer selects either the frequency divider output or the fastest clock.

Let us consider a circuit with 1000 flip-flops. If the slowest scan clock period based on the power budget is 80ns and we raise the frequency in 8 steps, then a modulo 125 (1000/8) counter will be implemented. *Assuming the worst-case activity by the captured states*, every scan-in is started with the 80ns clock and counter set to 0. The count goes up by 1 at every clock in which a non-transition enters the scan chain. When the count reaches 125, the counter is reset and the frequency divider generates a 70ns clock to scan-in the subsequent bits. The counter may again count up to 125 and the clock period would be reduced to 60ns. This process repeats until all 1000 bits are scanned in. Thus, if the input were a series of 1000 1s, the first 125 bits are scanned in at a clock of period 80ns, the second 125 bits at 70ns, until the last 125 bits are scanned in using a clock period 10ns. If the scan-in bits were a series of alternating 0s and 1s, the counter would never count up since there are no non-transitions entering the scan chain and

hence the entire scan-in will use the 80ns clock. Notice that due to the *worst-case assumption* we start each scan-in with slowest clock and so the activity monitor only raises the clock rate without ever having to lower it during the same scan-in.

Clearly, a bit stream with fewer transitions will be scanned in faster than one with many transitions. Don't cares in deterministic ATPG patterns can be filled in such that the number of transitions is minimum [15]. Also, techniques to generate BIST patterns with low transition densities [16] may be useful. This technique would perform well for such patterns.

B. BIST circuit with multiple scan chains

When the circuit has multiple scan chains, the activity of all chains must be monitored. XNOR gates are added across the input and output of the first flip-flop in every scan chain. Outputs of XNOR gates are supplied to a parallel counter [17] that counts up by the number of 1s at its input. The rest of the circuitry remains unaltered and still resembles the unshaded part of Figure 2. When the count reaches a certain threshold value, the frequency is stepped up and the counter is reset. Except for the use of the parallel counter the control scheme is similar to that in the unshaded portion of Figure 2.

C. BIST circuit with single scan chain and $\alpha_{peak} < 1$

The proposed implementation works well for circuits with test vectors having peak activity factors of 1. It does not require simulation of test vectors in order to estimate the peak activity factor and has low area overhead. However, it is not suitable when the scan clock frequency is computed based on a peak activity factor (α_{peak}) lower than 1. In such cases, it becomes necessary to modify the proposed model.

The slowest scan clock frequency is chosen using Eq. 1 using values of α_{peak} and peak power limit. The number of transitions in the scan chain is continuously monitored at the input and output of the scan chain.

Figure 2 shows the implementation of the technique for BIST circuits with single scan chain and peak activity factors lesser than 1. The activity monitor comprises of an xnor gate connected between the input and output of the first flip-flop, and an xnor gate connected between the input and output of the last flip-flop. The former monitors the number of non-transitions entering the scan chain and the latter monitors the number of non-transitions leaving the scan chain. An up-down counter keeps track of the number of non-transitions in the scan chain. Thus, the former xnor drives the count_up signal and the latter drives the count_down signal of the up-down counter. The number of non-transitions in the scan chain during any cycle is the difference between that entering the scan chain and that leaving the scan chain.

Since power is proportional to the activity in the scan chain, test power is lower when the number of transitions in the scan chain is lower or, in other words, when the number of non-transitions in the scan chain is higher. As discussed earlier, from (6), the scan frequency can be increased when the number of non-transitions in the scan chain increases.

The up-down counter is reset to 0 at the start of scan-in. When a non-transition enters the scan chain, the counter counts up and when a non-transition leaves the scan chain, the counter counts down. When the counter counts up to a certain threshold value, it signals the frequency control block to increase the frequency of scan clock and the counter is reset to 0. Similarly, when the counter counts down to 0, the frequency control block is signaled to lower the frequency of scan clock and is reset to the threshold value. Thus, whenever the number of non-transitions in the scan chain increases, the frequency is increased and when the number reduces, the

frequency is decreased. The rest of the circuitry functions the same as described earlier.

At the start of scan-in of a vector, the frequency control block is reset such that the frequency of scan clock is the slowest possible. This is based on the assumption that the activity factor of the vector captured in the scan chain before the start of scan-in equals α_{peak}. The scan clock frequency is never increased beyond the highest or decreased below the lowest possible frequency regardless of the signal from the counter.

It can be observed that this implementation can be easily modified for circuits with activity factors equal to 1, by removing the flip-flop at the end of the scan chain and tying the count_down signal of the up-down counter to 0.

D. BIST circuit with multiple scan chains and $\alpha_{peak} < 1$

When the circuit has multiple scan chains, the activity of all chains must be monitored. XNOR gates are added across the input and output of the first flip-flop and across the input and output of the last flip-flop in every scan chain. The outputs of the XNOR gates at the inputs of the scan chains are fed to the count_up inputs of a parallel counter [17] which counts up by the number of 1s at its count_up inputs. Similarly, the outputs of the XNOR gates at the end of the scan chains are fed to the count_down inputs of the parallel counter [17] which counts down by the number of 1s at its count_down inputs. The rest of the circuitry remains unaltered and still resembles Figure 2. When the count reaches a certain threshold value, the frequency is stepped up and the counter is reset. Except for the use of the parallel counter the control scheme is similar to that in Figure 2.

IV. ANALYSIS

Let N be the number of flip-flops, k be the peak activity factor of the test vectors (k = α_{peak}), α_{in} be the activity factor of the scan-in vector, α_{out} be the activity factor of the vector captured in the scan chain prior to scan-in, A be the number of non-transitions that enter the scan chain per cycle, v be the number of frequencies and T be the time period corresponding to the fastest clock.

The period of the fastest scan clock is v times shorter than the slowest clock. Therefore, the period of the slowest clock is given by vT. If the vectors were scanned in at the slowest clock, the total scan-in time per vector would be NvT.

If the scan-in vector has a uniform activity factor that is higher than that of the captured vector, the number of non-transitions entering the scan chain will be lower than that leaving it and hence there will be no change in scan clock frequency. However, if the scan-in vector has a uniform activity factor that is lower than that of the captured vector, the number of non-transitions entering the scan chain exceeds that leaving the scan chain. Therefore, the scan clock frequency is continuously increased. The scan-in of test vectors is started at the slowest possible clock period which equals vT and then continuously increased.

The number of transitions in the scan chain can range from 0 to kN. Therefore the number of non-transitions in the scan chain can range from $N - kN$ to $N - 0$ i.e., from $N(1-k)$ to N. In order to simplify the values, $N(1-k)$ is subtracted from both limits. Thus, the number of non-transitions can be monitored between $N(1-k) - N(1-k)$ and $N - N(1-k)$ i.e. between 0 and kN.

Since the maximum number of non-transitions encountered by the activity monitor is kN, a scan clock frequency is specified for every $\frac{kN}{v}$ non-transitions, in order to enable frequency control for all ranges of non-transitions. The scan

frequency is therefore increased every time the counter counts up to $\frac{kN}{v}$. Since A is the rate at which non-transitions enter the scan chain, A non-transitions enter the scan chain in 1 cycle. Because 1 non-transition enters the scan chain in $\frac{1}{A}$ cycles, x non-transitions will enter the chain in $\frac{x}{A}$ cycles.

The first bit in the scan-in vector is shifted at the lowest possible frequency (first frequency employed) which corresponds to a time period of vT. The frequency is not increased until $\frac{kN}{v}$ non-transitions enter the scan chain as discussed earlier. Since a non-transition enters the scan chain every $\frac{1}{A}$ cycles, $\frac{kN}{v}$ non-transitions are encountered in $\frac{kN}{Av}$ cycles. Thus, the frequency is not increased until about $\frac{kN}{Av}$ cycles. The counter is then reset and the frequency is increased to the next step which corresponds to a time period of $(v-1)T$. The frequency is not increased any further until the counter counts up to $\frac{kN}{v}$, i.e., until the number of non-transitions in the scan chain increases by $\frac{2kN}{v}$. This occurs after about $\frac{2kN}{Av}$ cycles (since a non-transition enters every $\frac{1}{A}$ cycles). Thus, the scan clock frequency (second frequency employed) whose clock period is $(v-1)T$ is used between the cycles $\frac{kN}{Av}$ and $\frac{2kN}{Av}$. The clock period can reach a maximum of T (v^{th} frequency employed). This frequency is used when the number of non-transitions in the scan chain increases by a value in the range between $\frac{(v-1)kN}{v}$ and kN or in other words, this frequency is used between clock cycles $\frac{(v-1)kN}{Av}$ and $\frac{kN}{A}$. Thus, by observation, the ith frequency corresponds to a clock period of $(v-i+1)T$ when the scan chain has between $\frac{(i-1)kN}{v}$ and $\frac{ikN}{v}$ increase in number of non-transitions. The ith frequency is employed between clock cycles $\frac{(i-1)kN}{Av}$ and $\frac{ikN}{Av}$.

The scan clock initially has a clock period of vT in cycle 1. The scan clock period is decreased in steps until the Nth cycle. Thus, the clock cycle corresponding to the last scan clock frequency is N. If the maximum number of speeds the scan clock will reach, for any vector is given by i, then

$$\frac{ikN}{Av} = N \qquad (7)$$

$$i = \frac{Av}{k} \qquad (8)$$

The total scan-in time per combinational vector is the sum of all clock periods used. The test time at each frequency is given by the product of the number of cycles run at that frequency and the clock period. Total time per vector is given by

$$\sum_{i=1}^{\frac{Av}{k}} \{\{\lceil \frac{ikN}{Av} \rceil - \lceil \frac{(i-1)kN}{Av} \rceil\}(v-i+1)T\} \qquad (9)$$

where v is usually chosen as a power of 2 because we can design a divide by 2^n frequency divider with n flip-flops. Time per vector if a single speed is used is NvT, and hence, the reduction in test time is given by

$$\frac{NTv - \sum_{i=1}^{\frac{Av}{k}} \{\{\lceil \frac{ikN}{Av} \rceil - \lceil \frac{(i-1)kN}{Av} \rceil\}(v-i+1)T\}}{NTv} \qquad (10)$$

If N and v were chosen as powers of 2, Eq. 9 reduces to

$$\text{Total time per vector} = \sum_{i=1}^{\frac{Av}{k}} \{(\frac{kN}{Av})(v-i+1)T\}$$

TABLE I
SCAN-IN TIME REDUCTION VS. NUMBER OF SCAN CLOCK SPEEDS FOR ACTIVITY FACTOR $\alpha_{in} = 0.5$.

Number of scan clock speeds	Test time reduction (%)		
	Simulation	Eq. (10)	Eq. (14)
1	0.00	0.00	0.00
2	0.34	0.00	0.00
4	12.64	12.50	12.50
8	18.78	18.75	18.75
16	22.03	21.90	21.88
32	23.56	23.48	23.44
64	25.17	24.26	24.22
128	27.41	24.66	24.61

TABLE II
SCAN-IN TIME REDUCTION VS. ACTIVITY FACTOR α_{in} FOR 8 SCAN-IN CLOCK SPEEDS.

Activity factor, α_{in}	Test time reduction (%)		
	Simulation	Eq. (10)	Eq. (14)
0	43.75	43.75	43.75
0.1	38.63	38.85	38.75
0.2	34.00	33.95	33.75
0.3	28.97	28.99	28.75
0.4	23.51	23.94	23.75
0.5	18.78	18.75	18.75
0.6	14.92	14.04	13.75
0.7	9.60	9.36	8.75
0.8	4.79	4.68	3.75
0.9	0.00	0.00	0.00
1	0.00	0.00	0.00

$$= (\frac{kN}{Av})(v.\frac{Av}{k} - \frac{\frac{Av}{k}(\frac{Av}{k}+1)}{2} + \frac{Av}{k})T \qquad (11)$$

Time per vector if a single speed is used is NvT, and

$$\text{Reduction in test time} = \frac{\{NTv - NT(v - \frac{Av}{2k} + \frac{1}{2})\}}{NTv}$$

$$= \frac{A}{2k} - \frac{1}{2v} \qquad (12)$$

The number of non-transitions in the scan chain in any cycle equals the difference between the number of non-transitions entering and leaving the scan chain. Non-transitions enter the scan chain at a rate of $(1 - \alpha_{in})$ and leave at the rate of $(1 - \alpha_{out})$. The non-transition density, A is therefore given by $A = \alpha_{out} - \alpha_{in}$. Thus, the reduction in test time is given by

$$\frac{(\alpha_{out} - \alpha_{in})}{2k} - \frac{1}{2v} \qquad (13)$$

where $k = 1$ for the model where the peak activity factor is assumed to be 1. In this model, the scan chain is assumed to be filled with transitions prior to scan-in and hence, the scan-in vector is assumed to be the sole contributor of non-transitions in the scan chain is . Thus, non-transitions enter the scan chain at a rate of $(1 - \alpha_{in})$ and hence, $A = 1 - \alpha_{in}$. The reduction in test time for this model is given by

$$\frac{(1 - \alpha_{in})}{2} - \frac{1}{2v} \qquad (14)$$

A C program was written to generate random vectors for a circuit with 1000 flip-flops. The test time reduction for these vectors was estimated, and compared with the values obtained from the formula. Table I shows the test time reduction versus number of frequencies for an activity factor of 0.5. Table II shows the variation of test time reduction with activity factor when the number of frequencies is 8. Both tables compare the test times estimated for random vectors (column 2), with those obtained from the accurate formula (9) (column 3) and from the approximate formula (14) (column 4).

Tables I and II show that for a chosen number of frequencies, vectors with lower activity achieve higher reduction in test time. The test time reduction increases when the number

TABLE III
REDUCTION IN TEST TIME FOR ISCAS89 CIRCUITS - TEST PER SCAN
BIST WITH SINGLE SCAN CHAIN.

Circuit	Number of scan flip-flops	Number of frequencies	Reduction in time (%)	Increase in area (%)
s27	8	2	7.49	14.72
s298	23	4	14.57	16.25
s420	35	4	13.81	13.02
s838	67	4	13.51	11.73
s1423	96	4	13.60	8.77
s5378	263	4	13.03	6.65
s9234	286	4	14.01	5.82
s13207	852	8	19.00	3.98
s15850	761	8	18.97	3.23
s35932	2083	8	18.74	2.55
s38417	1770	8	18.83	3.14
s38584	1768	8	18.91	2.13

of frequencies increases. The test time initially reduces rapidly for 8 frequencies and after that the reduction is gradual.

V. EXPERIMENTAL RESULTS

A. Circuits with $\alpha_{peak} = 1$

In verilog netlists of the ISCAS89 benchmark circuits flip-flops were added at all primary inputs and primary outputs. All flip-flops were converted to scan types and chained together. Thus, the number of flip-flops in the circuit would be the sum of the number of primary inputs, number of primary outputs and number of D-type flip-flops. A 23-bit linear feedback shift register (LFSR), a 23-bit signature analysis register (SAR), and a test-per-scan BIST controller were implemented [18], [19]. A single bit output of the LFSR supplied the scan input and the scan output was fed into the SAR. A suitable number for random patterns to achieve sufficient fault coverage for each circuit [20] was incorporated into the BIST controller. The sequential circuit along with the BIST circuitry was treated as the core circuit for test time and area analysis. The counter, frequency control circuitry, and frequency divider circuitry for dynamic frequency control were implemented as shown in the unshaded portions of Figure 2. The number of frequencies for each circuit was chosen according to the size of the circuit or the number of scan flip-flops.

ModelSim from MentorGraphics was used to simulate the circuits with and without the dynamic frequency control circuitry. The time required for test application was recorded in each case. DesignCompiler, a synthesis tool from Synopsys, was used to analyze the area of the circuits with and without the dynamic frequency control circuitry.

Since the LFSR generates pseudo random patterns, the activity factor is about 0.5. From (8), $x = 0.5v$, and hence, the number of frequencies the circuit will run at, is half the chosen number of frequencies. This corresponds to a clock period of $(0.5v + 1)T$. However, during power analysis, the next higher frequency is taken into consideration, in order to obtain pessimistic data. Thus, power analysis is done for a clock period of $0.5vT$, i.e., for a clock having twice the lowest frequency. Therefore, the power dissipated by the circuit for an activity factor 0.5 at every node and operating at twice the lowest frequency, was estimated for every circuit. The dynamic frequency control circuitry was included in this analysis. Table III shows the results. The number of frequencies chosen for each circuit is shown in column 3. The percentage reduction in test time with respect to the test time for the core circuit is shown in column 4 and the percentage increase in area with respect to the area of the core circuit is shown in column 5. At any node, the capacitance and the voltage are constant. From (1), the power dissipated at any node is proportional to the product of activity and frequency. Thus, the activity per unit time is a direct measure of power dissipated in the circuit. Therefore, an analysis to find activity per unit time
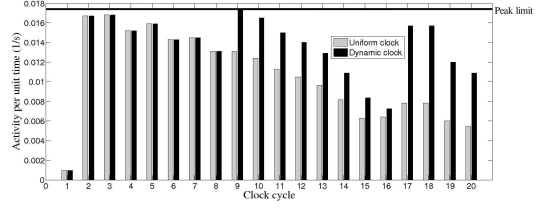

Fig. 3. Activity vs. number of clock cycle for s386 circuit.

TABLE IV
REDUCTION IN TEST TIME FOR ITC02 CIRCUITS.

Circuit	Scan flip-flops	Number of frequencies	Test time reduction (%)		
			$\alpha_{in} \approx 0$	$\alpha_{in} = 0.5$	$\alpha_{in} \approx 1$
u226	1416	8	46.68	18.75	0
d281	3813	16	46.74	21.81	0
d695	8229	32	48.28	23.36	0
f2126	15593	64	49.15	24.18	0
q12710	26158	128	49.45	24.53	0
p93791	96916	512	49.72	24.81	0
a586710	41411	256	49.73	24.77	0

was performed on the s386 benchmark circuit. The Synopsys power analysis tool, PrimeTime PX, was used. The activity per unit time in every cycle was found for the circuit for a scan vector with an activity factor of 1. The peak among these values was set as the limit for activity per unit time. The values of activity per unit time of the circuit in every cycle were found for a vector with an activity factor of 0.25 using uniform clock and dynamic clock methods. The results are shown in Figure 3. Notably, the activity per unit time in every cycle is closer to the peak limit when dynamic clock method is used. Also, the peak limit is never exceeded in both methods. A reduction of 11.25% was observed when the dynamic clock method was used.

The results for multiple scan chain implementation would be very similar to that obtained for single scan chain. The test time will not vary much since the activity of the circuit will be very similar in both single and multiple chain implementations. However, there would be a marginal increase in area due to the additional XNOR gates at the first flip-flop of every scan chain and also due to the use of a parallel counter as opposed to the simple counter used for the single scan chain.

These results for reduction in test time conform to the theoretical results given in Tables I and II. Two trends are clearly observed in Table III. As circuit size increases, the area overhead drops and test time reduction improves. These circuits are not very large from today's standard and we can expect better results as predicted by the analysis.

To estimate the test time reduction for larger circuits, an accurate mathematical analysis was applied to ITC02 circuits. Test time reduction was computed for best ($\alpha_{in} \approx 0$), moderate ($\alpha_{in} = 0.5$) and worst ($\alpha_{in} \approx 1$) cases of scan chain activity factors. The test-per-scan BIST was assumed. Table IV shows the results. The number of scan flip-flops in column 2 is the sum of number of inputs, number of outputs and number of flip-flops. The number of frequencies for circuits are shown in column 3. The test time reductions achieved for best, moderate and worst case activity factors are shown in Columns 4, 5 and 6, respectively. Evidently, more test time reduction can be achieved in larger circuits. The reduction in test time varies from 0% for patterns causing very high activity to 50% for patterns with almost no activity. When external tests are used and an ATPG tool generates them, the vectors may have very few care bits. The don't care bits can be filled in using heuristics [21] to minimize scan transitions. Then, a dynamic control of scan clock will provide a large reduction in test time. This is illustrated using the ISCAS89 benchmark s38584. The Synopsys ATPG tool TetraMAX was used to generate two sets of vectors, a set of 961 vectors

TABLE V
REDUCTION IN TEST TIME IN T512505 CIRCUIT.

α_{in}	α_{out}							
	0	0.1	0.2	0.3	0.4	0.5	0.6	0.65
0	0	7.59	15.29	22.98	30.67	38.36	46.06	49.9
0.1	0	0	7.59	15.29	22.98	30.67	38.36	42.21
0.2	0	0	0	7.59	15.29	22.98	30.67	34.52
0.3	0	0	0	0	7.59	15.29	22.98	26.83
0.4	0	0	0	0	0	7.59	15.29	19.13
0.5	0	0	0	0	0	0	7.59	11.44
0.6	0	0	0	0	0	0	0	3.75
0.65	0	0	0	0	0	0	0	0

with no don't care bits and another set of 14,196 vectors with don't care bits. The vector set without don't cares was found to have an activity factor around 0.5 and the vector set with don't care bits was found to have a low activity factor around 0.01. The don't care bits in the second set were filled using a minimum transition heuristic [21]. Reductions of 43.14% and 18.8% were achieved for the test vector sets with and without don't care bits.

In another typical scenario, a test set may initially contain few (say, 10%) high activity ($\alpha_{in} = 0.5$) vectors. These resemble fully-specified random vectors and achieve about 70-75% fault coverage. The latter 90% vectors then detect about 20-25% hard-to-detect faults and contain many don't cares, which may be filled in for reduced ($\alpha_{in} \leq 0.05$) activity. The adoptive test will be potentially beneficial in such cases.

B. Circuits with $\alpha_{peak} < 1$

In order to estimate the reduction in scan-in time achieved with the model proposed for dynamic scan clock frequency control in circuits with peak activity factors lower than 1, the t512505 ITC02 benchmark circuit was chosen. This circuit is large enough to employ 512 different scan clock frequencies because it has 76714 scan flip-flops.

The pattern sets of various large benchmark circuits were studied to analyze trends in peak activity factors. The mean value of peak activity factor (α_{peak}) in these pattern sets was found to be around 0.57 and the standard deviation (σ) was around 0.025. The value of mean + 3σ was found to be around 0.65. This indicates that the probability that the peak activity factor of the test patterns of a circuit would lie below 0.65 is 99.7%. Therefore, the peak activity factor for the t512505 circuit was set at 0.65. The pattern sets generated by TetraMAX ATPG for large benchmark circuits were analyzed and it was found that the peak activity factor in these test vectors never exceeded 0.65.

It is important to note that the value of 0.65 for peak activity factor can be used only for large circuits having flip-flop numbers in the range of a few hundreds. For smaller circuits with flip-flop numbers in the order of a few tens, the peak activity factor was found to be 1.

Mathematical analysis was used to estimate the reduction in scan-in time achieved in the t512505 circuit when $\alpha_{peak} = 0.65$ and 512 steps of frequencies were chosen. The results are listed in Table V. It can be seen from Table V that when the activity factor of the scan-out vector (α_{in}) is greater than or equal to the activity factor of the captured vector (α_{out}), there is no reduction in scan-in time. The frequency is increased only when the number of non-transitions in the scan chain increases. However, when $\alpha_{in} > \alpha_{out}$ the number of non-transitions (as counted by the counter) never increases and hence the scan-in is carried out at the starting frequency which is the frequency employed when dynamic scan clock frequency control is not implemented. Thus, the reduction in scan-in time is 0% in such cases.

Table V shows the variation of scan-in time reduction with variation in α_{in} and α_{out}. It indicates that scan-in time reduction is higher for lower values of α_{in} and for higher values of α_{out}. This can be explained from the perspective of number of non-transitions in the scan chain. If α_{in} is low, the number of non-transitions entering the scan chain is high and if α_{out} is high, the number of non-transitions leaving the scan chain is low. Thus, the net number of non-transitions in the scan chain is high giving a higher reduction in scan-in time.

VI. CONCLUSION

Reduction of test application time in power-constrained testing by adoptively adjusting the scan frequency to the circuit activity is demonstrated. On-chip hardware, whose overhead reduces as the circuit becomes large, provides the adoptive control. The technique is particularly beneficial when the peak circuit activity during test is very high but the average activity is quite low.

REFERENCES

[1] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Springer, 2000.
[2] P. Girard, "Survey of Low-Power Testing of VLSI Circuits," *IEEE Design and Test of Computers*, vol. 19, pp. 80–90, May–June 2002.
[3] I. Bayraktaroglu and A. Orailoglu, "Test Volume and Application Time Reduction through Scan Chain Concealment," in *Proc. Des. Automation Conf.*, pp. 151–155, 2001.
[4] Y. Bonhomme, T. Yoneda, H. Fujiwara, and P. Girard, "An Efficient Scan Tree Design for Test Time Reduction," in *Proc. IEEE European Test Symposium*, pp. 174–179, 2004.
[5] I. Bayraktaroglu and A. Orailoglu, "Decompression Hardware Determination for Test Volume and Time Reduction through Unified Test Pattern Compaction and Compression," in *Proc. 21st IEEE VLSI Test Symp.*, pp. 113–118, 2003.
[6] I. Bayraktaroglu and A. Orailoglu, "Concurrent Application of Compaction and Compression for Test Time and Data Volume Reduction in Scan Designs," *IEEE Trans. Computers*, vol. 52, pp. 1480–1489, Nov. 2000.
[7] J. Rajski, J. Tyszer, M. Kassab, N. Mukherjee, R. Thompson, H. Tsai, A. Hertwig, N. Tamarapalli, G. Mrugalski, G. Eide, and J. Qian, "Embedded Deterministic Test for Low Cost Manufacturing Test," in *Proc. Int. Test Conf.*, pp. 301–310, 2002.
[8] A. Chandra and K. Chakrabarty, "Reduction of SoC Test Data Volume, Scan Power and Testing Time Using Alternating Run-Length Codes," in *Proc. Int. Conf. Computer Aided Design*, pp. 673–678, 2002.
[9] A. Chandra and K. Chakrabarty, "Frequency-Directed Run-Length (FDR) Codes With Applicatin to System-on-A-Chip Test Data Compression," in *Proc. 19th IEEE VLSI Test Symposium*, pp. 42–47, 2001.
[10] W. J. Lai, C. P. Kung, and C. S. Lin, "Test Time Reduction in Scan Designed Circuits," in *Proc. European Des. Automation Conf.*, pp. 489–493, 1993.
[11] E. M. Rudnick and J. H. Patel, "A Genetic Approach to Test Application Time Reduction for Full Scan and Partial Scan Circuits," in *Proc. Int. Conf. on VLSI Design*, pp. 288–293, Jan. 1995.
[12] S. Y. Lee and K. K. Saluja, "Test Application Time Reduction for Sequential Circuits with Scan," *IEEE Trans. CAD*, pp. 1128–1140, Sept. 1995.
[13] S. Y. Lee and K. K. Saluja, "An Algorithm to Reduce Test Application Time in Full Scan Designs," in *Proc. Int. Conf. CAD*, pp. 17–20, 1992.
[14] H. C. Tsai, S. Bhawmik, and K. T. Cheng, "An Almost Fullscan BIST Solution - Higher Fault Coverage and Shorter Test Application Time," in *Proc. Int. Test Conf.*, pp. 1065–1073, Oct. 1998.
[15] R. Sankaralingam, R. R. Oruganti, and N. A. Touba, "Static Compaction Techniques to Control Scan Vector Power Dissipation," in *Proc. IEEE VLSI Test Symp.*, pp. 35–40, April-May 2000.
[16] S. Wang and S. K. Gupta, "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," in *Proc. Int. Test Conf.*, pp. 85–94, 1999.
[17] E. E. Swartzlander, Jr., "A Review of Large Parallel Counter Designs," in *Proc. IEEE Computer Society Annual Symposium on VLSI*, pp. 89–98, Feb. 2004.
[18] V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A Tutorial on Built-In Self-Test, Part 1: Principles," *IEEE Design and Test of Computers*, vol. 10, pp. 73–82, Mar. 1993.
[19] C. Stroud, *A Designer's Guide to Built-In Self-Test*. Springer, 2002.
[20] F. Brglez, D. Bryan, and K. Kozminski, "Combinational Profiles of Sequential Benchmark Circuits," in *Proc. Int. Symp. Circuits and Systems*, pp. 1929–1934, May 1989.
[21] N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault, and A. Virazel, "Minimizing Peak Power Consumption during Scan Testing: Test Pattern Modification with X Filling Heuristics," in *Proc. Int. Conf. on Design and Test of Integrated Systems in Nanoscale Technology*, pp. 359–364, Sept. 2006.