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Ultra Low Energy CMOS Logic Using Below-Threshold Dual-Voltage Supply

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This paper investigates subthreshold voltage operation of digital circuits. Starting from the previously known single supply voltage for minimum energy per cycle, we further lower the energy consumption by using dual subthreshold supplies. Level converters, commonly used in the above threshold design, are found to be unacceptably slow for subthreshold voltage operation. Therefore, special constraints are used to eliminate level converters. We give a new mixed integer linear program (MILP) that automatically and optimally assigns gate voltages, avoids the use of level converters, and holds the minimum critical path delay, while minimizing the total energy per cycle. Using examples of a 16-bit ripple-carry adder and a 4×4 multiplier we show energy savings of 23% and 5%, respectively. The latter is a worst case example because most paths are critical. Alternatively, for the same energy as that of single below-threshold supply, an optimized dual voltage design can operate at 3 to 4 times higher clock rate. Also, we show energy saving up to 22.2% from the minimum energy point over ISCAS'85 benchmark circuits. The MILP optimization with special consideration for level converters is general and applicable to any supply voltage range.

Keywords: Ultra Low Power Design, Subthreshold Circuits, Dual Voltage Design, Mixed Integer Linear Program.

1. INTRODUCTION

The ubiquitous era of emerging portable devices demands long battery lifetime as a primary design goal. Subthreshold circuit design can reduce energy per cycle by one or more orders of magnitude by scaling power supply voltage (V_{dd}) below the device threshold voltage (V_{th}). Ultra-low power applications such as micro-sensor networks, pacemakers, and many portable devices operate under extreme energy constraint for long battery lifetime.[17–19] Subthreshold circuit design is suitable for such emerging energy-constrained applications.[4, 12, 28, 34, 36, 37, 42]

As the power supply voltage is scaled down below the device threshold voltage, the subthreshold current ever so slowly charges and discharges nodes according to the logic function of the circuit.[36] Despite a very high energy efficiency, the subthreshold design has been applied only in niche markets due to its low performance.

Ultra-dynamic voltage scaling (UDVS) can provide useful system applications by switching between a highly energy efficient subthreshold V_{dd} mode and a normal above-threshold V_{dd} mode.[3] The normal or subthreshold mode may be chosen according to the workload of the system.

According to the available literature, most low-power techniques exploit time slack on non-critical paths of a circuit to reduce power consumption without performance loss. These techniques have been applied to circuits operating with the nominal supply voltage by sizing device widths, using multi-V_{th} devices, or using multiple V_{dd}.[23, 30, 38] For subthreshold circuits, the technique of sizing device width affects the correct logic function of CMOS circuits at low supply voltage.[36] The multi-V_{th} technique does not adequately utilize the time slack in the subthreshold regime,[1] because semiconductor foundries normally provide standard cell libraries with two to three fixed V_{th} values, namely, high V_{th}, standard V_{th}, and low V_{th}, for low-power design. Gate delay exponentially depends on V_{th} in a subthreshold circuit. Therefore, we cannot utilize all possible time slack on non-critical paths in a subthreshold circuit without further manipulation of these device threshold voltages.

The multi-V_{dd} technique has been widely implemented for two supply voltages.[20] The dual-V_{dd} design is best suited for exploiting the time slack in a subthreshold circuit as well.[13, 15, 16] Although the gate delay exponentially depends on V_{dd} in the subthreshold region it may be possible to find an optimal lower supply voltage for the available time slack in the circuit. A DC to DC voltage

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converter[26] will then allow the voltage management. Utilizing the time slack for dual-V_{dd} assignment can give valuable energy saving with small extra cost in physical design.

There are two scenarios for applying dual-V_{dd} design to subthreshold circuits in energy constrained low-performance applications. Consider a digital circuit working in an absolutely minimum energy consumption mode. The supply voltage for such an operation is known to be in the subthreshold range.[36] We can further reduce the energy consumption without changing the performance by assigning an extra lower supply voltage only to gates on non-critical paths. Alternatively, the subthreshold circuit can be sped up by several times by selecting two supply voltages, one of which is higher than the optimal single V_{dd}. Small energy increase from the absolute minimum energy point of a subthreshold circuit can notably improve performance.[7] In this scenario, the dual-V_{dd} design retains the energy consumption close to that of the single-V_{dd} minimum energy point but operates at a higher speed obtained by using the higher supply for gates on critical paths.

Our contribution provides a framework for finding the optimal dual-V_{dd} assignment in a subthreshold circuit with given speed requirement. The design procedure formulates mixed integer lineal programs (MILP) that, given today's computing capabilities, can deal with moderately large circuit complexity.[8]

In a dual voltage circuit, signal level converters are considered essential. A level converter simply changes a logic 1 level from one V_{dd} voltage to another V_{dd} voltage. Even though level converters insert delays and consume power,[24, 39] in their absence certain interfaces become unsatisfactory. This is because the logic 1 level produced by a gate has the same voltage level as its V_{dd}. However, for a proper switching operation another receiving gate with a different V_{dd} requires the input signal to match its own V_{dd}. In particular, driving a high V_{dd} gate with a low voltage signal causes high leakage and long delay. We characterize all multi-level interfaces and our MILP contains constraints to eliminate interfaces where level converters may otherwise be essential.

The paper is organized as follows. Section II introduces properties of subthreshold operating circuits with key terms. In Section III, we extend the existing dual-V_{dd} techniques of above-threshold operation, clustered voltage scaling (CVS)[32] and extended-CVS (ECVS)[33] to the subthreshold regime. New MILP solutions are presented in Section IV. Section V reports SPICE simulation results to validate MILP solutions. Finally, a conclusion of this work appears in Section VI.

2. SUBTHRESHOLD CIRCUITS

Before discussing the original method of dual-V_{dd} optimization of subthreshold circuits, we briefly summarize the properties of the subthreshold circuits in terms of functional operation and failure, performance and energy on which some of the earliest work was reported by Swanson and Meindl[31] and Vittoz and Fallrath.[35]

2.1. Minimum Operating Voltage

For the correct functional operation of a subthreshold logic circuit, the supply voltage V_{dd} should be higher than a certain minimum voltage (V_{min}). The theoretical V_{min} is given as,[22, 40]

$$V_{min} = 2 \cdot V_T \cdot \ln\left(1 + \frac{S}{\ln 10 \cdot V_T}\right) \quad (1)$$

where $V_T = kT/q$ is the thermal voltage, $k = 1.381 \times 10^{-23}$ J/K is Boltzmann's constant, T is absolute temperature in Kelvin, $q = 1.602 \times 10^{-19}$ C is electronic charge. At 300 K (room temperature), $V_T = 26$ mV. S is the slope of drain to source current (I_{ds}) in the subthreshold region, usually referred to as *subthreshold swing*. For example, for 0.18 μm technology $S \approx 90$ mv/decade.[40] That means that a 90 mV reduction in V_{gs} will reduce I_{ds} by a factor of 10. That gives $V_{min} = 48$ mV at 300 K.

We define the on-current I_{on} as I_{ds} for $V_{gs} = V_{ds} = V_{dd}$ and off-current I_{off} as I_{ds} for $V_{gs} = 0$ and $V_{ds} = V_{dd}$ in the subthreshold region ($V_{dd} < V_{th}$). From Ref. [9], S is degraded with the downscaling trend of the CMOS technology, which means that the reduced ratio of I_{on} to I_{off} will cause smaller noise margins and possible functional logic failures at or below V_{min}.

Figure 1 shows the simulation of a chain of 1,000 inverters for different supply voltages and inputs of logic 0 (ground) and logic 1 (V_{dd}). The circuit was simulated in 90 nm CMOS in the Predictive Technology Model (PTM)[43] using HSPICE simulator.[10] The minimum operating voltage for the inverter chain is found to be 80 mV to guarantee a 10% to 90% output voltage swing. As we move from the input toward the output we observe degrading logic levels, which eventually stabilize between the depth of 10 to 20. Basically, this means that the logic 0

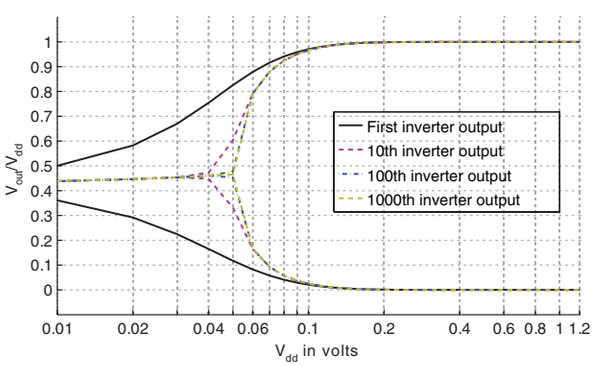


Fig. 1. HSPICE[10] simulation for output logic levels in an 1,000-inverter chain normalized to supply voltage V_{dd} in PTM 90nm CMOS (INV: $W_p = 5.5 \cdot L_g$, $W_n = 2.4 \cdot L_g$).

Table I. HSPICE[10] simulation of a 1,000-inverter chain using a single supply voltage V_{dd} and PTM 90 nm CMOS technology.[43]

	First inverter output				10th inverter output				100th inverter output				1000th inverter output			
	Logic (mV)		Delay (ns)		Logic (mV)		Delay (ns)		Logic (mV)		Delay (ns)		Logic (mV)		Delay (ns)	
V_{dd} (mV)	1	0	Rise	Fall	1	0	Rise	Fall	1	0	Rise	Fall	1	0	Rise	Fall
80	75.3	3.3	101.0	103.0	74.0	4.6	129.0	107.0	74.0	4.6	129.0	107.0	74.0	4.6	130.0	106.0
100	97.1	2.1	50.9	42.7	96.6	2.5	58.9	50.3	96.6	2.5	58.8	50.4	96.6	2.5	58.2	50.3
200	199.7	0.2	4.1	3.86	199.7	0.2	4.32	3.99	199.7	0.2	4.29	3.94	199.7	0.2	4.29	3.94

and 1 levels stabilize close to ground and supply voltages, respectively, and do not continue to degrade with the logic depth of the circuit. The data in Table I, which is directly obtained from the HSPICE[10] simulation, clearly shows this.

A new noise tolerant circuit design was proposed based on differential Schmitt trigger gates.[6] This approach increases noise immunity for low voltage subthreshold circuits compared to standard CMOS subthreshold logic circuits.

Rise and fall transition times for outputs of inverters are not degraded through an 1000 inverter chain at lower supply voltages as shown Figure 2. From these simulation results, subthreshold logic circuits guarantee the correct functional operation above the minimum energy point.

2.2. Delay

The delay of a gate in a subthreshold circuit can be simply formulated from the gate delay equation,[9]

$$t_d = \frac{K \cdot C_L \cdot V_{dd}}{I_{on}} \tag{2}$$

where K is a fitting parameter and C_L is the load capacitance of the gate. By replacing I_{on} with subthreshold drain current (I_{sub}),[36]

$$I_{sub} = I_o \cdot 10^{((V_{gs}-V_{th}+\eta V_{ds})/S)} \cdot (1 - e^{-V_{ds}/V_T}) \tag{3}$$

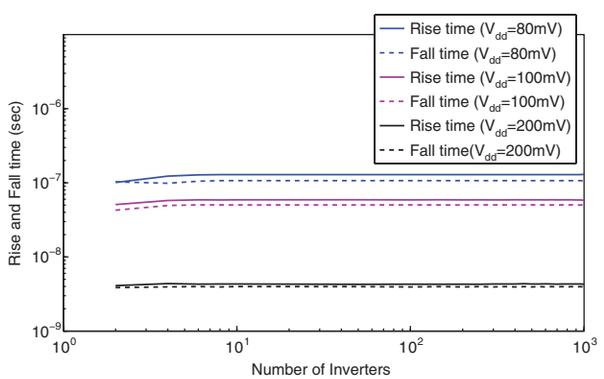


Fig. 2. Rise and fall transition times for the outputs of inverters in an 1000 inverter chain at lower supply voltages with HSPICE simulations in PTM 90 nm CMOS (INV: $W_p = 5.5 \cdot L_g$, $W_n = 2.4 \cdot L_g$).

where η is *drain-induced barrier lowering* (DIBL) coefficient and I_o is drain current at $V_{gs} = V_{th}$. When $V_{gs} = V_{ds} = V_{dd} \gg V_T$ (≈26 mV at 300 K), we get gate delay as,

$$t_d = \frac{K \cdot C_L \cdot V_{dd}}{I_o \cdot 10^{(((\eta+1)V_{dd}-V_{th})/S)}} \tag{4}$$

Thus, t_d is exponentially dependent on V_{dd}, V_{th}, η, and S.

2.3. Energy

Energy per cycle of a circuit is a key parameter for energy efficiency in ultra-low power applications. Because computing workload is characterized in terms of clock cycles, this measure directly relates energy consumption to the workload. Before considering the energy consumed by a circuit, we start by examining the total energy per cycle (E_{tot}) of a single gate, which is composed of dynamic energy (E_{dyn}) and leakage energy (E_{leak}):

$$E_{dyn} = \alpha_{0\to1} \cdot C_L \cdot V_{dd}^2 \tag{5a}$$

$$\begin{aligned} E_{leak} &= P_{leak} \cdot t_d \\ &= I_{off} \cdot V_{dd} \cdot t_d \\ &= K \cdot C_L \cdot V_{dd}^2 \cdot 10^{-V_{dd}/S} \end{aligned} \tag{5b}$$

$$\begin{aligned} E_{tot} &= E_{dyn} + E_{leak} \\ &= (\alpha_{0\to1} + K \cdot 10^{-V_{dd}/S}) \cdot C_L \cdot V_{dd}^2 \end{aligned} \tag{5c}$$

where $\alpha_{0\to1}$ is the low to high transition activity for the gate output node and P_{leak} is static leakage power. I_{off} is static leakage current and presented by (3):

$$I_{off} = I_o \cdot 10^{((-V_{th}+\eta V_{ds})/S)} \quad V_{ds} \gg V_T \tag{6}$$

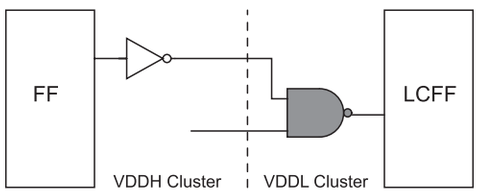
Successful hardware implementations of single-voltage subthreshold circuits have been reported. An FFT chip was built by Wang and Chandrakasan[37] in 180 nm CMOS technology and was shown to work with $V_{dd} = 350$ mV at a clock rate of 10 kHz. The threshold voltage was 450 mV. Its power consumption of the chip was 0.6 μW. Subthreshold voltage processor chips have been built and tested by Seok et al.[28] A subthreshold SRAM (256 kb) in 65 nm CMOS has been reported by Calhoun and Chandrakasan.[2]

3. DUAL-V_{dd} SCHEME FOR SUBTHRESHOLD OPERATION

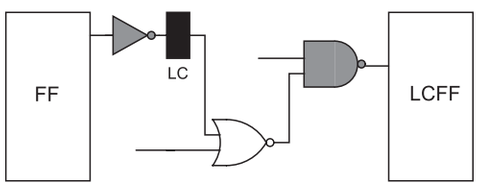
Scaling V_{dd} down in circuits reduces both dynamic power and static leakage power besides reducing the performance. To reduce power consumption without degrading performance, a multi-V_{dd} technique exploits time slacks and lowers voltage V_{DDL} for gates on non-critical paths.

As shown in Figure 3(a), a *clustered voltage scaling* (CVS) algorithm[32] does not allow the V_{DDL} cells to feed directly into V_{DDH} cells and so level converting is implemented inside the flip-flop (LCFF).[11] This topological limitation reduces full use of time slacks that exist in a circuit. The *extended clustered voltage scaling* (ECVS) in Figure 3(b) eliminates this constraint by inserting a level converter (LC) with each V_{DDL} cell feeding into a V_{DDH} cell. ECVS gives better power saving than CVS but LC adds to power and delay overheads.

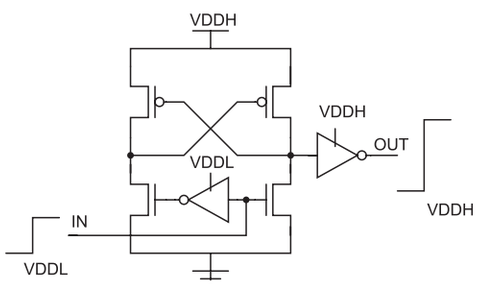
Without a level converter the low to high output transition delay of the second stage inverter in Figure 4 is not affected by the input voltage swing V_{DDL} from the previous stage, because the delay of the pull-up PMOS is only dependent on its own power supply V_{DDH}.[27] During the high to low output transition of the second inverter, the pull-down NMOS delay is affected by both the input



(a) Clustered voltage scaling (CVS).



(b) Extended clustered voltage scaling (ECVS).



(c) Level converter (LC).

Fig. 3. Dual V_{dd} schemes and level converter schematic.[32, 33]

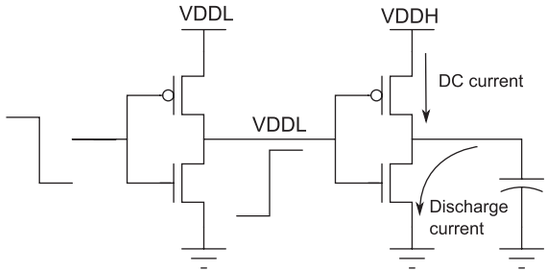


Fig. 4. A two-inverter chain without level converter.

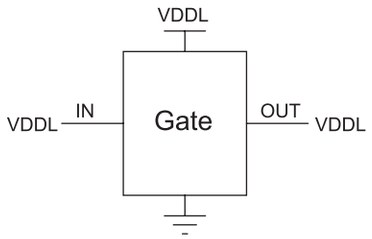
swing V_{DDL} and the power supply V_{DDH}. Therefore, lower input swing reduces discharge current through the NMOS, which increases the pull-down delay. Because the pull-up PMOS in the inverter could not be shut off completely by the lower input swing level, severe DC current from the power supply V_{DDH} induces higher static leakage power consumption.

In subthreshold operation, the lower input swing exponentially increases the delay (4) of the driven gate. We investigate the delay and leakage power penalty from lower input swing voltage. For simplicity, in this paper, we use only four types of cells, namely, INV, NAND2, NAND3 and NOR2, to synthesize example circuits. For cell characterization, all simulation results are from HSPICE using PTM 90 nm CMOS. The device threshold voltages are $V_{th,\,PMOS} = 0.21$ V and $V_{th,\,NMOS} = 0.29$ V at nominal $V_{dd} = 1.2$ V and room temperature (300 K).

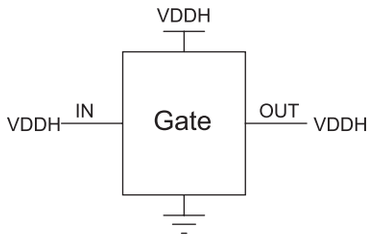
Various input and output configurations interfacing gates in dual V_{dd} assignments are shown in Figure 5. Table II summarizes the delay and static leakage power for each case where $V_{DDH} = 250$ mV and $V_{DDL} = 200$ mV such that the entire operation is in subthreshold region. The difference between LL and HH delays shows that gate delay (4) is exponentially sensitive to the power supply voltage, while P_{leak} has a smaller change.

In Table II, as expected, due to smaller discharging time constants HL delays for NAND2 and NAND3 gates are lower than those for the LL configuration. However, that is not the case for INV and NOR2 gates, which are faster in the LL configuration. This speed increase is due to a higher logic 0 level for the LL configuration in charging time. In the case of leakage power for HL, all gates suppress the leakage current through the pull-up PMOS ($V_{gs} > 0$) from the power supply. Severe increases of the delay and power in dual-V_{dd} scheme are from LH, which is prohibited in CVS methodology and is allowed in ECVS with LC. But, a common LC used for above-threshold in Figure 3(c) cannot be used due to its unacceptable delay overhead besides the power overhead.

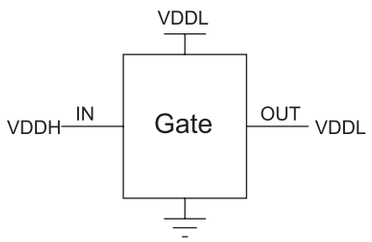
From Table III, the LC delay penalty in subthreshold operation is around 80 fanout-of-four (FO4) inverter delays, which exceeds a clock cycle time of a low voltage shallow pipelined microprocessor (40 FO4 delays) or



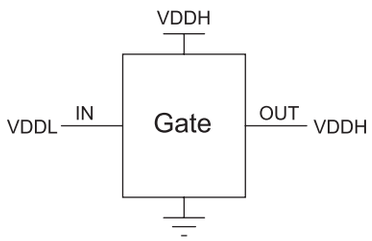
(a) LL: Low input swing driving a low V_{dd} gate.



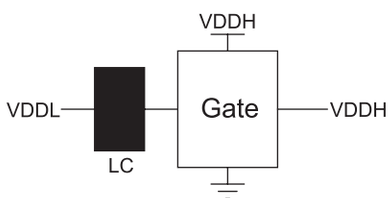
(b) HH: High input swing driving a high V_{dd} gate.



(c) HL: High input swing driving a low V_{dd} gate.



(d) LH: Low input swing driving a high V_{dd} gate.



(e) L-LC-H: Low input swing driving a high V_{dd} gate through a level converter.

Fig. 5. Driven gates and input swing levels.

ASIC processor (44 FO4 delays).[5, 29] A new LC design suitable for subthreshold circuits may be needed but is out of the scope of the present work. In the next section, we include additional constraints in the MILP that will not allow the LH configuration (similar to CVS) for energy optimization.

4. MILP FOR V_{DDL} ASSIGNMENT

In this section, we design minimum energy circuits with dual-V_{dd} assignment using mixed integer linear programming (MILP).[8] First, the optimal (i.e., minimum energy per cycle) supply voltage (V_{opt}) for a single V_{dd} operation is determined. The critical path delay (or clock cycle time) of this design is used as the timing requirement for the dual voltage design. Thus, the MILP automatically applies higher supply voltage $V_{DDH} = V_{opt}$ to gates on critical paths to maintain the performance and finds an optimal lower supply voltage V_{DDL} assigned to gates on non-critical paths to reduce the total energy consumption by a global optimization considering all possible V_{DDL}. This differs from the backward traversal CVS heuristic algorithms that tend to be non-optimal. Note that more paths now may have delays that are either equal or close to the critical path delay.

Let X_i be an integer variable that is 0 for V_{DDH} or 1 for V_{DDL} for the power supply assignment of gate i. Let T_c be a predetermined critical path delay for the circuit. The optimal minimum energy voltage assignment problem is formulated as an MILP model:

$$\text{Minimize} \sum_{i \in \text{all gates}} [E_{\text{tot},\, V_{DDL},\, i} \cdot X_i + E_{\text{tot},\, V_{DDH},\, i} \cdot (1 - X_i)] \quad (7)$$

$E_{\text{tot, i}}$ for V_{DDL} and V_{DDH} are given by (5a) and (5b)

$$E_{\text{tot, i}} = \alpha_i \cdot C_{\text{L},\, i} \cdot V_{\text{dd},\, i}^2 + P_{\text{leak},\, V_{\text{dd}},\, i} \cdot T_c \quad (8)$$

Subject to timing constraints:

$$t_{d,i} = t_{d,\, V_{DDL},\, i} \cdot X_i + t_{d,\, V_{DDH},\, i} \cdot (1 - X_i) \quad \forall i \in \text{all gates} \quad (9)$$

$$T_i \geq T_j + t_{d,i} \quad \forall j \in \text{all fanin gates of gate } i \quad (10)$$

$$T_i \leq T_c \quad \forall i \in \text{all primary output gates} \quad (11)$$

Subject to topological constraints:

$$X_i - X_j \geq 0 \quad \forall j \in \text{all fanin gates of gate } i \quad (12)$$

In above constraints, T_i is the latest arrival time at the output of gate i corresponding to a primary input event.[25] As mentioned in Section III, the unacceptable delay penalty of asynchronous LC prohibits its use in a dual V_{dd} scheme in the subthreshold region. The MILP model does not allow a V_{DDL} cell to drive a V_{DDH} cell as its fanout gate on account of topological constraint (12) as shown in Figure 6. Thus, the LH configuration of Figure 5(d) never occurs in the optimized circuit. Within the given timing constraint T_c, originally obtained for the best energy per cycle for single subthreshold V_{DDH} operation, the MILP searches recursively for the best V_{DDL} such that the energy per cycle is further reduced to a true minimum. The MILP needs to run multiple times for searching the optimal V_{DDL}, but we presented a new MILP algorithm that runs only one-time for finding the best V_{DDL} in 13, 14.

Table II. Measurement of a gate delay with a single INV load and static leakage power in Figure 5 configurations at $V_{DDH} = 250$ mV and $V_{DDL} = 200$ mV through HSPICE simulation for PTM 90 nm CMOS.

	Gate delay, t_d (ns)					Leakage power, P_{leak} (pW)				
Gate	(a) LL	(b) HH	(c) HL	(d) LH	(e) L-LC-H	(a) LL	(b) HH	(c) HL	(d) LH	(e) L-LC-H
INV	2.81	0.83	2.98	2.70	255.04	30.9	46.2	22.8	126.2	260.8
NAND2	6.82	2.10	5.31	7.92	260.32	31.1	45.3	26.2	101.5	259.9
NAND3	9.72	3.04	7.31	11.17	264.16	53.1	75.6	49.0	135.5	290.2
NOR2	8.33	2.54	8.91	5.73	262.27	32.6	48.4	20.8	156.6	263.0

Table III. Comparison of conventional LC (Figure 3(c)) delays normalized to INV(FO = 4) delay ($V_{DD} = V_{DDH}$) for normal and subthreshold operations in PTM 90 nm CMOS.

Gate delay	Normal $V_{DDH} = 1.2$ V $V_{DDL} = 0.8$ V	Subthreshold $V_{DDH} = 300$ mV $V_{DDL} = 250$ mV
INV(FO = 4)	23.64 ps	1.52 ns
LC	112.33 ps	121.86 ns
LC norm. to INV(FO4)	4.8	80.2

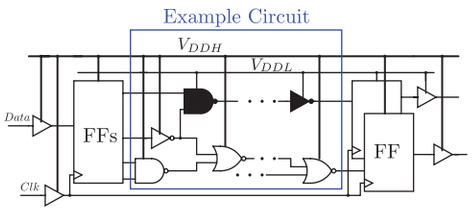


Fig. 7. Simulation setup.

5. RESULTS

As mentioned before, we use only simple four basic cells (INV, NAND2, NAND3 and NOR2) for synthesizing two example circuits, a 16-bit ripple carry adder and a 4×4 multiplier, and ISCAS'85 benchmark circuits in PTM 90 nm CMOS technology. The delay, capacitance and average leakage power of these four basic cells are characterized for the MILP model by scaling V_{dd} with a 10 mV resolution in HSPICE simulations. Switching activity α is the average number of low to high transitions at circuit nodes, which is calculated using a logic simulator with randomly generated input vectors. These randomly generated input vectors are the same as input signal vectors to the circuit for HSPICE simulation to measure energy consumption.

As shown in Figure 7, our example circuit, embedded in a test bench, is driven by randomly generated high input swing flip-flops. Two subthreshold voltages may be provided by a DC to DC voltage converter.[20, 26, 37] The energy per cycle measurement is for combinational circuit excluding flip-flops.

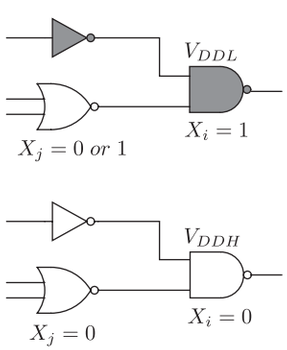
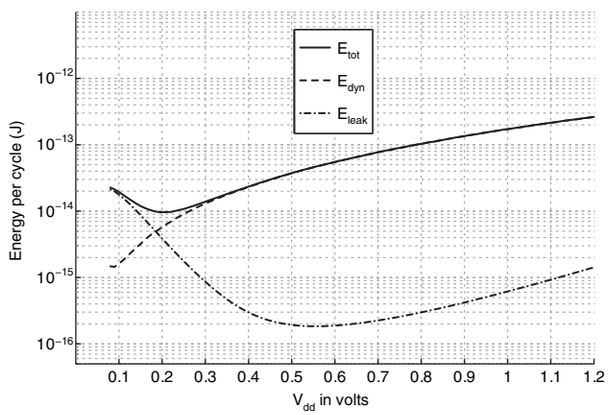
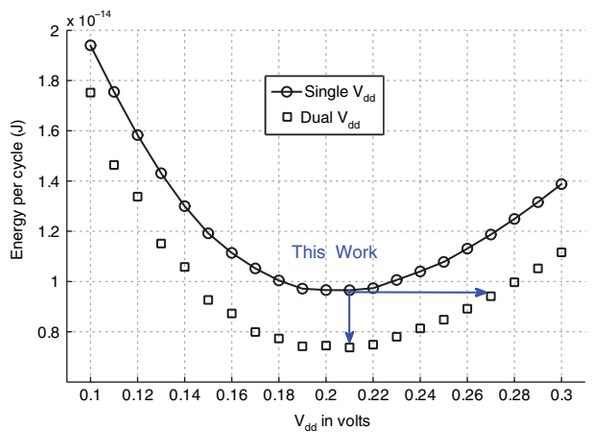


Fig. 6. Topological constraints.



(a) Energy per cycle for single V_{dd}.



(b) Energy per cycle for single and dual subthreshold supply voltages.

Fig. 8. Energy per cycle for a 16-bit ripple carry adder for single V_{dd} and dual V_{dd} in subthreshold region, activity factor $\alpha = 0.21$, PTM 90 nm CMOS.

Table IV. Total energy per cycle with optimal V_{DDL} for given V_{DDH} and maximum corresponding speed.

	16-bit ripple carry adder ($\alpha = 0.21$, total gates = 176)						4×4 multiplier ($\alpha = 0.32$, total gates = 140)					
V_{DDH} (V)	V_{DDL} (V)	V_{DDL} gate #	$E_{tot,\,single}$ (fJ)	$E_{tot,\,dual}$ (fJ)	Reduction (%)	Freq. (MHz)	V_{DDL} (V)	V_{DDL} gate #	$E_{tot,\,single}$ (fJ)	$E_{tot,\,dual}$ (fJ)	Reduction (%)	Freq. (MHz)
0.10	0.09	108	19.40	17.52	9.7	0.13	0.09	18	13.78	13.35	3.1	0.16
0.11	0.09	106	17.55	14.64	16.6	0.17	0.09	18	12.44	11.80	5.1	0.21
0.12	0.10	106	15.83	13.38	15.5	0.22	0.10	18	11.41	10.85	4.9	0.27
0.13	0.10	101	14.31	11.51	19.6	0.28	0.10	15	10.61	10.08	5.0	0.35
0.14	0.11	101	13.00	10.58	18.6	0.37	0.11	15	10.04	9.56	4.8	0.46
0.15	0.11	99	11.92	9.27	22.3	0.48	0.11	15	9.69	9.13	5.8	0.60
0.16	0.12	99	11.14	8.73	21.6	0.62	0.12	15	9.51	8.98	5.6	0.78
0.17	0.12	95	10.52	7.99	24.0	0.80	0.12	13	9.48	8.99	5.2	1.00
0.18	0.13	95	10.04	7.73	23.0	1.02	0.13	13	9.59	9.11	5.0	1.30
0.19	0.13	88	9.72	7.42	23.6	1.32	0.13	13	9.74	9.19	5.6	1.67
0.20	0.14	88	9.66	7.45	22.9	1.68	0.14	13	10.21	9.65	5.5	2.14
0.21	0.14	84	9.65	7.37	23.6	2.15	0.15	13	10.66	10.08	5.4	2.73
0.22	0.15	84	9.73	7.49	23.1	2.72	0.15	12	11.06	10.60	4.2	3.46
0.23	0.16	84	10.06	7.80	22.5	3.44	0.16	12	11.83	11.24	5.0	4.37
0.24	0.17	84	10.40	8.14	21.8	4.33	0.17	12	12.53	11.93	4.8	5.50
0.25	0.18	84	10.78	8.48	21.3	5.43	0.18	13	13.28	12.61	5.0	6.87
0.26	0.18	78	11.31	8.91	21.2	6.77	0.19	13	14.14	13.43	5.0	8.55
0.27	0.19	78	11.87	9.42	20.7	8.41	0.19	12	15.03	14.30	4.9	10.60
0.28	0.20	78	12.49	9.97	20.2	10.39	0.20	12	15.98	15.22	4.8	13.06
0.29	0.22	88	13.16	10.52	20.1	12.79	0.21	12	16.98	16.19	4.7	16.02
0.30	0.23	88	13.88	11.16	19.6	15.65	0.22	12	18.03	17.21	4.5	19.54
Average					20.5						4.9	

From Figure 8(a), the minimum energy point for a 16-bit ripple carry adder with an activity factor $\alpha = 0.21$ is 9.65 fJ at $V_{dd} = 0.21$ V. The clock frequency was found to be 2.15 MHz. With dual-V_{dd} assignment the optimized circuit with $V_{DDH} = 0.21$ V and $V_{DDL} = 0.14$ V reduces the energy per cycle by up to 23.6% retaining the same performance. This energy reduction is shown by the downward arrow in Figure 8(b).

Consider again the minimum energy per cycle (9.65 fJ) operation of the 16-bit ripple-carry adder circuit with a single subthreshold voltage 0.21 V and a clock frequency of 2.15 MHz.

In an alternative design, we may hold the minimum energy constant and improve the performance. From the MILP results in Table IV, we find that operation with two voltages 0.27 V (V_{DDH}) and 0.19 V (V_{DDL}) consumes 9.42 fJ, which is just under the minimum energy but has a clock frequency 8.41 MHz. This, as shown by the right arrow in Figure 8(b), has about 4X speed improvement.

As a worst case example, a path balanced 4×4 multiplier reduces the energy per cycle to 5% below the minimum energy point with $V_{DDH} = 0.17$ V and $V_{DDL} = 0.12$ V, where the performance is not degraded. For better performance, the 4×4 multiplier can operate at 1.67 MHz from a clock frequency 1 MHz on minimum energy with single V_{dd}, where two supply voltages 0.19 V (V_{DDH}) and 0.13 V (V_{VDDL}) are provided and minimum energy increases slightly.

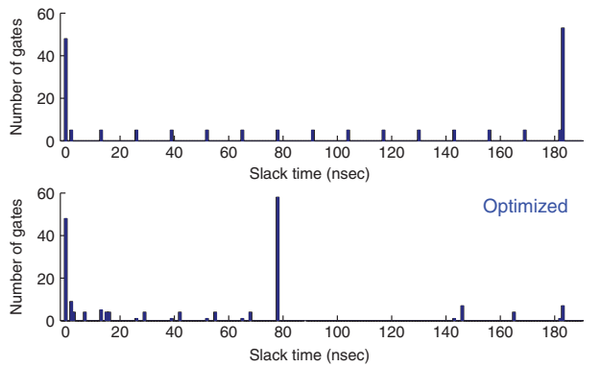
Two example circuits using dual-V_{dd} show that performance improves largely for a circuit with large positive slack. Figures 9(a) and (b) illustrate gate slack distribution[13, 14] of a 16-bit ripple carry adder and a 4×4 multiplier, respectively, for single and dual V_{dd} (Optimized) design at the minimum energy point.

Table IV summarizes SPICE simulation giving the total energy per cycle for the single voltage $V_{dd} = V_{DDH}$ reference and the optimized dual voltage $V_{dd} = \{V_{DDH},\ V_{DDL}\}$ circuits. Voltages vary from 0.1 V to 0.3 V. Both single and dual V_{dd} circuits have the same speed because all gates on critical paths have the same V_{DDH} for either circuit.

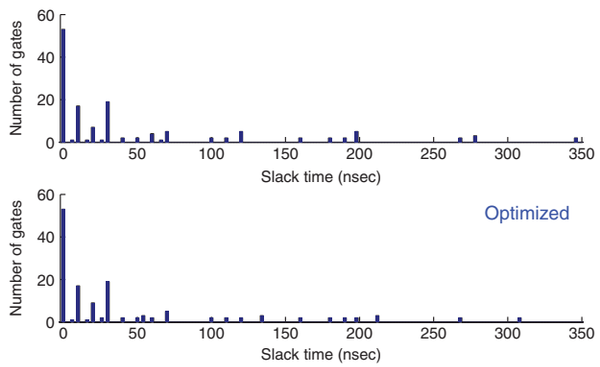
The energy savings at minimum energy operating points using dual-V_{dd} are obtained from HSPICE simulations for ISCAS'85 benchmark circuits, as shown in Table V. The optimized c880 (an 8-bit ALU) shows 22.2% energy saving as the best case. The energy saving for c6288 (a 16×16 multiplier) is only about 2.1%. Gate slack distribution is shown for c880 and c6288, respectively, in Figure 10.

Logic function failure occurs at 0.08 V in NAND3, so the possible lowest V_{DDL} assignment in MILP optimization is 0.09 V. This minimum operating voltage guarantees 10% to 90% output voltage swing for all four cells in the full range of operational voltages used. Figure 11 shows sample signal waveforms from an optimized 16-bit ripple carry adder circuit for $V_{DDH} = 0.11$ V and $V_{DDL} = 0.09$ V. This has V_{DDL} assigned to cells on a non-critical path that leads to the least significant sum bit (s1). The output flip-flop (s1q) holds correct signal values at the minimum operating voltage on positive clock edges.

When V_{DDH} is 100 mV, it is approaching the lower end of its range beyond which the circuit would fail to operate. The MILP now has limited choices for a solution and gives a V_{DDL} that provides smaller energy saving.

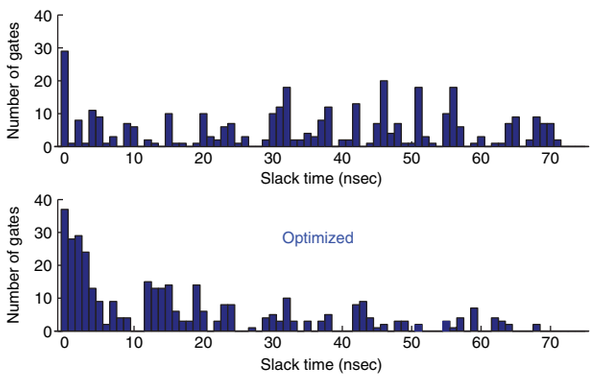


(a) 16-bit ripple carry adder at $V_{DDH} = 0.21$V and $V_{DDL} = 0.14$V.

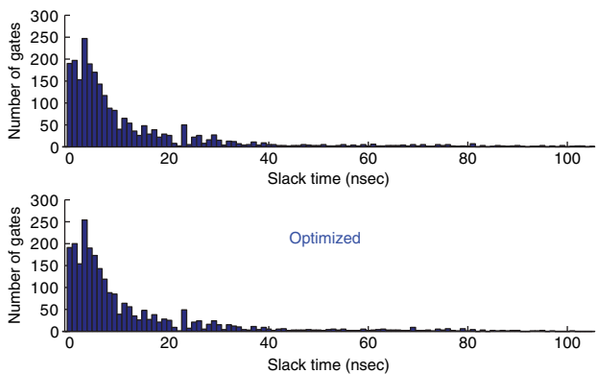


(b) 4×4 multiplier at $V_{DDH} = 0.17$V and $V_{DDL} = 0.12$V.

Fig. 9. Gate slack distribution (number of gates vs. slack) of a 16-bit ripple carry adder and a 4×4 multiplier for single-V_{dd} ($= V_{DDH}$) and dual-V_{dd} ($= V_{DDH}$, V_{DDL}) at the minimum energy point; slacks obtained by static timing analysis using gate delays for PTM 90 nm CMOS.



(a) c880 at $V_{DDH} = 0.24$V and $V_{DDL} = 0.18$V.



(b) c6288 at $V_{DDH} = 0.29$V and $V_{DDL} = 0.18$V.

Fig. 10. Gate slack distribution of c880 and c6288 for single-V_{dd} and dual-V_{dd} at the minimum energy point in PTM 90 nm CMOS.

The 16-bit ripple carry adder has better energy reduction because it can utilize more time slack from non-critical paths compared to the 4×4 multiplier with more balanced paths. The gate delay in subthreshold operation increases exponentially with reducing supply voltage, which forces the optimal V_{DDL} close to V_{DDH}.

Even though the MILP model only allows HL configuration and eliminates the use of LC for a dual V_{dd} circuit block, level conversion may be needed at outputs to match signal levels across block to block connections of a system. The differential cascode voltage switch (DCVS) based level converter of a normal standard cell library in Figure 3(c) is not suitable for dual subthreshold design due to its huge delay penalty. Realizing that the design of LC for ultra low voltage is an open

Table V. Energy saving with optimal V_{DDL} for given V_{DDH} (minimum energy operating point) in ISCAS'85 benchmark circuits for PTM 90 nm CMOS.

Benchmark circuit	Total gates	Activity α	V_{DDH} (V)	V_{DDL} (V)	V_{DDL} gates (%)	E_{single} (fJ)	E_{dual} (fJ)	$E_{reduc.}$ (%)	Freq. (MHz)
c432	154	0.19	0.25	0.23	5.2	7.9	7.8	1.1	14.4
c499	493	0.21	0.22	0.18	9.7	20.2	19.8	2.0	11.9
c880	360	0.18	0.24	0.18	46.4	14.4	11.2	22.2	13.6
c1355	469	0.21	0.21	0.18	10.2	19.5	19.0	2.5	9.8
c1908	584	0.20	0.24	0.21	24.3	26.5	25.0	5.8	11.8
c2670	901	0.16	0.25	0.21	46.4	32.8	28.0	14.8	17.4
c3540	1270	0.33	0.23	0.14	7.0	88.0	84.6	3.8	7.2
c5315	2077	0.26	0.24	0.19	47.1	116.8	98.0	16.1	9.8
c6288	2407	0.28	0.29	0.18	2.7	165.4	162.0	2.1	9.4
c7552	2823	0.20	0.25	0.21	42.3	131.7	117.1	11.1	13.6
Average					24.1			8.2	

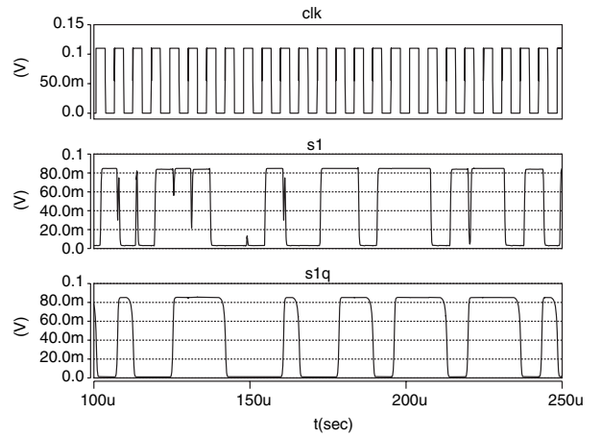


Fig. 11. Output signal waveforms of s1 and s1q in a 16-bit ripple carry adder ($V_{\mathrm{DDH}} = 0.11$ V, $V_{\mathrm{DDL}} = 0.09$ V) from HSPICE simulation, PTM 90nm CMOS.

problem, our design refrains from using level converters while taking the penalty of energy saving into account. For level converting, we always assign V_{DDH} to primary output (PO) gates before the output flip-flops at multiple voltage boundaries between circuit blocks. The PO gates driven by V_{DDL} cells are found to correctly execute their logic functions if, for a given V_{DDH}, V_{DDL} is bounded as shown in Figure 12. This lowest possible V_{DDL} raises the minimum operating voltage for the dual voltage optimized circuit block. The optimal V_{DDL} in MILP model can be higher than its true optimal value to suppress DC leakage power of the LH configured PO gates. Using two small example circuits, a 16-bit ripple-carry adder and a 4×4 multiplier show average reduced energy savings of 11.9% and 2.6%, respectively. The penalty of energy saving from level converting may be negligible for a large system in which most blocks would operate at V_{DDL} and only a few need V_{DDH}.

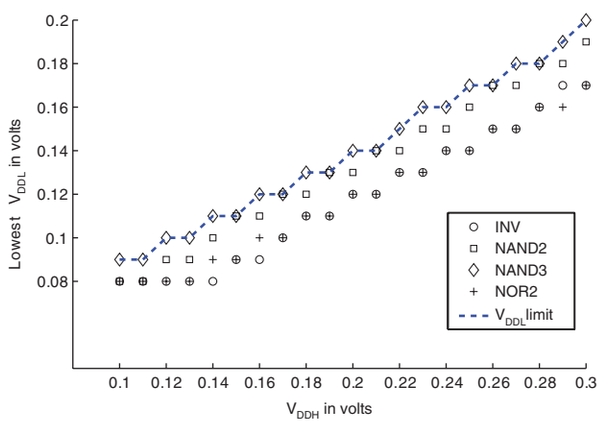


Fig. 12. V_{DDL} bound for given V_{DDH} with LH configured cells.

6. CONCLUSION

In this paper, we investigate the validation of dual-V_{dd} assignment to a bulk CMOS subthreshold circuit. Some applications in the market may need minimum energy consumption without a performance concern. This work could provide a framework for solving those design problems. For a wide range of speed requirements, the MILP determines globally minimum energy optimized circuit configurations by assigning an extra supply voltage V_{DDL} to gates on non-critical paths.

A 16-bit ripple carry adder shows on average 20.5% reduced energy consumption, while maintaining same performance as the original single V_{dd} circuit. The worst case example of 4×4 multiplier still gives on average 4.9% reduction. Further, allowing a small amount of increase in the energy consumption can significantly speed-up the subthreshold operation of a logic circuit. The methodology of dual-V_{dd} assignment is valid for substantial speed-up without energy increase, as well as for energy reduction below the minimum achievable in a single voltage circuit. With the proposed MILP, ISCAS'85 benchmark circuits could save up to 22.2% (c880) energy per cycle.

The MILP techniques of this paper are not restricted to subthreshold operation alone. When a higher performance, impossible to achieve in the subthreshold region, is required we would then obtain two above-threshold voltages that will satisfy the performance criteria and minimize the energy per cycle.[13,14] There may be potential for greater energy saving as circuit size increases due to larger critical path delay leading to greater slack for many gates. The process variation of the device threshold voltage (V_{th}) can seriously affect a subthreshold voltage design and this needs to be studied especially for nanometer technologies.[21,41] Higher leakage technologies may display higher speed in the subthreshold region because the logic operation relies on leakage currents. These aspects of dual-V_{dd} design in subthreshold region are worth exploring in the future.

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