4-day Intensive Course on
"Design for Testability – Theory and Practice"
Organized by VLSI Society of India

In cooperation with IEEE Circuits and Systems Society, Bangalore Chapter

Dates – July 27-30, 2005

Venue – Bangalore (*Exact venue will be anno unced*)

Corporate Sponsor: TESSOLVE test is our business

Instructors

Prof. Adit Singh and Prof. Vishwani Agrawal, Auburn University

Adit D. Singh is James B. Davis Professor of Electrical & Computer Engineering at Auburn University, where he directs the VLSI Design & Test Laboratory. Earlier he has held faculty positions at the University of Massachusetts in Amherst, and Virginia Tech in Blacksburg. His research interests are in VLSI design, test, and reliability, and he has published extensively in these areas. Over the years he has taught approximately 50 short courses in-house for companies including IBM, National Semiconductor, TI, AMD, Bell Labs and Sandia Labs (earlier also for Digital, Control Data, and Data General), and at IEEE technical meetings, and through university extension programs. These have primarily been in the areas of VLSI design, test, reliability and fault tolerance. Prof. Singh currently serves on the Executive Committee of the IEEE Test Technology Technical Council, on the Editorial Board of IEEE Design and Test, and is the General Chair of the 2003 IEEE Memory Test Workshop. He is a Fellow of IEEE and a Golden Core Member of the IEEE Computer Society.

Vishwani D. Agrawal is James J. Danaher Professor of Electrical & Computer Engineering at Auburn University, Auburn, Alabama, USA. He has over thirty years of industry and university experience, working at Bell Labs, Rutgers University, TRW, IIT in Delhi, EG&G, and ATI. His areas of research include VLSI testing, low-power design, and microwave antennas. He has published over 250 papers, holds thirteen U.S. patents and has co-authored 5 books including Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits with Michael Bushnell at Rutgers. He is the founder and Editor-in-Chief of the Journal of Electronic Testing: Theory and Applications, was a past Editor-in-Chief of the IEEE Design & Test of Computers magazine, and is the Founder and Consulting Editor of the Frontiers in Electronic Testing Book Series.
Dr. Agrawal is a co-founder of the International Conference on VLSI Design, and the International Workshops on VLSI Design and Test, held annually in India. He served on the Board of Governors of the IEEE Computer Society in 1989 and 1990, and, in 1994, chaired the Fellow Selection Committee of that Society. He has received seven Best Paper Awards, the Harry H. Goode Memorial Award of the IEEE Computer Society, and the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign. Dr. Agrawal is a Fellow of the IETE-India, a Fellow of the IEEE and a Fellow of the ACM. He has served on the advisory boards of the ECE Departments at University of Illinois, New Jersey Institute of Technology, and the City College of the City University of New York.

Course contents

- The exponential nature of the testing problem
- Fault models
- Stuck-at faults
- Test generation for combinational circuits
- D algorithm
- PODEM, FAN and learning based ATPG
- Fault coverage
- Fault simulation
- Fault grading
- Testability measures
- Test generation algorithms for sequential circuits
- Scan and partial scan design
- Functional testing of microprocessor/controllers
- Design for testability
- Built in self-test (BIST)
- Test compression techniques for test data volume reduction
- Boundary scan and the IEEE 1149 testability standard
- Memory testing
- Memory BIST
- SOC test issues
- P1500 core test standard
- Current testing: IDDQ and IDDT
- Structural delay testing
- Fmax and MinVDD testing
- Test cost and effective ness
- Test coverage and defect levels
- Stress testing
- Reliability Screens for burn -in minimization

Course Fee

Before June 1, 2005		After June 1, 2005	
Working Indian Professional (Non-member)	Rs 12000/-	Working Indian Professional (Non-member)	Rs 13000/-
Working Indian Professional (VSI individual member)	Rs 10,000/-	Working Indian Professional (VSI individual member)	Rs 11,000/-
Student or faculty from Indian academic/ governmental organization (Non-member)	Rs 8000/-	Student or faculty from Indian academic/ governmental organization (Non-member)	Rs 9000/-
Academic/governmental organizations from India (Individual Member of VSI)	Rs 6000/-	Academic/governmental organizations from India (Individual Member of VSI)	Rs 7000/-
Foreign registrant	USD 300/-	Foreign registrant	USD 350/-

4-day Intensive Course on

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Registration Form

Name of the participant: (Please use block letters. *The certificate will be made in this name* .)			
Category: Circle appropriate			
Working Professional (Non-member)	Working Professional (VSI member)	Academic/governmental organization from India (Non-member)	Academic/governmental organization from India (Member of VSI)
If you are a student, mention Semester/Year:			
Contact Address:			
E-mail:			
Background in DFT: (Courses/Reading/Projects)			
VSI Membership Number (if applicable):			
Details of DD enclosed *For office use:* *Regn No:*	DD Number		
	Drawn on Bank		
	Dated		
If you have specific questions that you want instructors to address, please indicate:			
After completing the registration form, mail it with the DD to the following address. Mr Gopal Naidu, Treasurer , VLSI Society of India Finance Department Texas Instruments (India) Pvt Ltd Bagmane Tech Park CV Raman Nagar Bangalore 560093			
• *Please make the DD to " **VLSI Society of India** " payable at **Bangalore*** • *On the back of the DD, please write " **DFT Course** "* • *Partial registration is not permitted* • *Registration is not transferable* • *Queries may please be sent to: vsi_india@rediffmail.com*			
Note:	Course fee includes registration material, lunch and refreshments on all the days. Transport and stay arrangements are the responsibility of the participants. Processing fee of Rs 1000/ - will be charged against cancellations.		