Organized by

http://vlsi-india.org/vsi
VLSI Society of India

In cooperation with

C-DAC Hyderabad and
IEEE TTTC

3-day Short Course on
Design for Testability – Theory and Practice

July 27-29, 2006
Hyderabad
Venue: Hotel Fortune Katriya (www.fortunekatriya.com)

Instructors:
Prof. Adit Singh and Prof. Vishwani Agrawal, Auburn University

Overview:

The three-day course on "Design for Testability" is intended for practicing engineers as well as faculty and students. It will provide an overview of the subject by two leading experts in the field, who will sprinkle the contents with recent developments in the area.

Vishwani D. Agrawal is James J. Danaher Professor of Electrical & Computer Engineering at Auburn University, Auburn, Alabama, USA. He has over thirty years of industry and university experience, working at Bell Labs, Rutgers University, TRW, IIT in Delhi, EG&G, and ATI. His areas of research include VLSI testing, low-power design, and microwave antennas. He has published over 250 papers, holds thirteen U.S. patents and has co-authored 5 books including Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits with Michael Bushnell at Rutgers. He is the founder and Editor-in-Chief of the Journal of Electronic Testing: Theory and Applications, was a past Editor-in-Chief of the IEEE Design & Test of Computers magazine, and is the Founder and Consulting Editor of the Frontiers in Electronic Testing Book Series. Dr. Agrawal is a co-founder of the International Conference on VLSI Design, and the International Workshops on VLSI Design and Test, held annually in India. He served on the Board of Governors of the IEEE Computer Society in 1989 and 1990, and, in 1994, chaired the Fellow Selection Committee of that Society. He has received seven Best Paper Awards, the Harry H. Goode Memorial Award of the IEEE Computer Society, and the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign. Dr. Agrawal is a Fellow of the IETE-India, a Fellow of the IEEE and a Fellow of the ACM. He has served on the advisory boards of the ECE Departments at University of Illinois, New Jersey Institute of Technology, and the City College of the City University of New York.

Adit D. Singh is James B. Davis Professor of Electrical & Computer Engineering at Auburn University, where he directs the VLSI Design & Test Laboratory. Earlier he has held faculty positions at the University of Massachusetts in Amherst, and Virginia Tech in Blacksburg. His research interests are in VLSI design, test, and reliability, and he has published extensively in these areas. Over the years he has taught approximately 50 short courses in-house for companies including IBM, National Semiconductor, TI, AMD, Bell Labs and Sandia Labs (earlier also for Digital, Control Data, and Data General), and at IEEE technical meetings, and through university extension programs. These have primarily been in the areas of VLSI design, test, reliability and fault tolerance. Prof. Singh currently serves on the Executive Committee of the IEEE Test Technology Technical Council, on the Editorial Board of IEEE Design and Test, and is the General Chair of the 2003 IEEE Memory Test Workshop. He is a Fellow of IEEE and a Golden Core Member of the IEEE Computer Society.

Course contents

The exponential nature of the testing problem
Fault models
Stuck-at faults
Test generation for combinational circuits
D algorithm
PODEM, FAN and learning based ATPG
Fault coverage
Fault simulation
Fault grading
Testability measures
Test generation algorithms for sequential circuits
Scan and partial scan design
Functional testing of microprocessor/controllers
Design for testability
Built in self-test (BIST)
Test compression techniques for test data volume reduction
Boundary scan and the IEEE 1149 testability standard
Memory testing
Memory BIST
SOC test issues
P1500 core test standard
Current testing: IDDQ and IDDT
Structural delay testing
Fmax and MinVDD testing
Test cost and effective ness
Test coverage and defect levels
Stress testing
Reliability Screens for burn -in minimization

Course Fee

Before July 1, 2006		After July 1, 2006	
Professionals (Non- Members)	Rs.9,000/-	Professionals (Non- Members)	Rs.10,000/-
Professionals (VSI/ IEEE members)	Rs.7,500/-	Professionals (VSI/ IEEE members)	Rs.8,500/-
Students/Faculty (Non-members)	Rs.4,500/-	Students/Faculty (Non-members)	Rs.6,500/-
Students/Faculty (Members of VSI/ IEEE)	Rs.3,500/-	Students/Faculty (Members of VSI/ IEEE)	Rs.4,500/-

3-day Short Course on
Design for Testability – Theory and Practice

July 27-29, 2006

Hotel Fortune Katriya, Hyderabad

Organized by VLSI Society of India

http://vlsi-india.org/

In cooperation with:

C-DAC Hyderabad and IEEE TTTC

REGISTRATION FORM

Name of the participant:

(Please use block letters. The certificate will be made in this name)

Category: Tick appropriate	Industry Member (Non-VSI)	☐	Member of:	Membership No:
	VSI/ IEEE member	☐	VSI/ IEEE Membership No:	
	Academic/governmental organization from India (Non-VSI)	☐	Member of:	Membership No:
	Academic/governmental organization from India (VSI/ IEEE member)	☐	VSI/ IEEE Membership No:	

If you are a student, mention Semester/Year:

Contact Address: (Provide permanent mailing address)	**Designation:** Student ☐ Faculty ☐ Industry ☐ Other ☐ **College/ Company:** **Permanent address:**			
E-mail: (Compulsory)				
Background in VLSI: (Courses/Reading/Projects)				
Details of DD enclosed	DD Number			
	Drawn on Bank		Dated	

Your background and expectations from the workshop:

Signature

After completing the registration form, mail it with the DD to the following address:

Mr. Gopal Naidu
Treasurer, VLSI Society of India
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore 560093

Please also e-mail the details of payment to ***vsi_india@rediffmail.com***

- *Please make the DD to "**VLSI Society of India**" payable at **Bangalore**.*
- *On the back of the DD, please write "**3-day Course on Design for Testability – Theory and Practice, Bangalore**" to avoid confusion.*
- *Partial registration is not permitted. Processing fee of Rs.1000/= will be charged against cancellation.*
- *Queries may please be sent to: **vsi_india@rediffmail.com***
- *Seats are limited to 50. Spot Registration against cancellations, and strictly by cash payment.*
- ***Venue:** To be Announced*

Note:

- Course fee includes registration material, vegetarian lunch and refreshments on all the days.
- Transport and stay arrangements are the responsibility of the participants.
- Registration can be transferred to a colleague with intimation 15 days prior to the event.
- Registration on Day-1 at 8.30 AM, Course on all days from 9.00 AM to 6.00 PM.
- DD Acknowledgement through mail confirms registration.