

- ABnb, 590
 ABnN, 589
 Abraham, 266, 396
 Abramovici, 78, 171, 206, 621
 absolute dominator, 197
 AC, 36
 AC parametric test, 30, 32
 AC voltmeter, 346
 acceptance test, 17, 48, 596
 access time test, 303
 activation cost, 243
 activation energy, 261
 active and passive neighborhood pattern, 288
 active and passive neighborhood pattern sensitive fault, 258
 active area, 476
 active gate, 103
 active neighborhood pattern, 288
 active neighborhood pattern sensitive fault, 258, 272
 activity list, 103
 ad-hoc DFT, 466
 Adams, 626
 adaptive GA, 247
 ADC, 322, 338
 address decoder, 264
 address decoder fault, 63, 258, 273
 address descrambler, 26
 address failure memory, 26
 address formatting, 306
 address generator, 530
 address set-up time sensitivity test, 303
 address stepper, 533
 Advantest Model T6682 tester, 24
 AF, 258, 273
 Agarwal, 532
 age defect, 58
 aging factor, 37
 Agrawal, P., 53, 160, 239, 502
 Agrawal, V. D., 53, 65, 129–131, 160, 239, 477, 479, 502, 621, 624, 628
 AI, 18
 air pollution, 259
 Aitken, 441, 447
 Akers, 158, 206
 alias image, 352
 aliasing, 512, 514, 518
 aliasing probability, 518
 all instructions with random data fault model, 597
 alloying, 261
 alternate assignment, 162, 174
 Ambler, 53, 627
 Amerasekera, 627
 analog automatic test-pattern generation (ATPG), 397, 411
 analog backtrace, 407
 analog bipartite graph, 400, 401, 403
 analog boundary module, 580, 583
 analog circuit connectivity matrix, 399
 analog circuit design for testability, 401, 404, 413
 analog circuit element, 399
 analog circuit graph, 399
 analog circuit parameter, 399
 analog circuit performance, 399, 401
 analog component deviation, 398
 analog double-fault model, 403, 405, 406
 analog element observability, 404
 analog element tolerance, 401
 analog element tolerance box, 400, 403
 analog element variation, 399
 analog fault coverage, 398, 401
 analog fault observation, 401
 analog fault ordering, 393
 analog fault simulation, 390
 analog multiple fault model, 398
 analog output parameter, 398, 400
 analog output parameter measurement, 399
 analog reverse simulation, 407, 410
 analog signal flow graph inversion, 408
 analog single-fault model, 405
 analog switch resistance, 591
 analog switch sizing, 591
 analog test access port, 579
 analog test bus, 576
 analog test bus chaining, 579
 analog test bus switching pattern, 581
 analog testability analysis, 401
 analog tolerance computation, 398
 analog triple-fault model, 405, 406
 AND bridging fault, 61, 258, 271
 ANP, 288
 ANPSF, 258, 272, 286
 aperture uncertainty, 352
 APNP, 288
 APNPSF, 258
 appearance fault, 61, 65
 application specific integrated circuit, 8
 Arabian, 622, 628
 arbitration priority set-up time, 306
 arbitration test, 305
 architectural design, 7
 area overhead, 475, 493
 Armstrong, 109, 176
 array level, 261
 artificial intelligence, 18
 ASIC, 8
 assertion fault, 60
 asymmetric coupling fault, 270
 asynchronous clear, 230
 asynchronous loop, 233
 asynchronous preset, 230
 at-speed test, 9, 42, 490, 611
 at-speed testing, 435
 AT1, 580
 AT1N, 589
 AT2, 580
 AT2N, 589
 AT&T standard telecom test, 359