Power-Aware SoC Test Optimization through Dynamic Voltage and Frequency Scaling

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Abstract

Emerging cellular and wireless technologies such as WiMAX and LTE require high data rates, low latency at very low power budgets. SoCs are well suited for such requirements as they offer small area, low power, programmable and cost-effective hardware solutions. A SoC device is an integration of a complete system, including multiple programmable processors, onto a single chip. In recent times, SoCs are extensively used in networking and communication applications.

Increased complexity in the SoCs, due to technological advances, have resulted in high volumes of test data and, consequentially, lengthy test times. The process of testing SoC device is also constrained by high power consumption and testing resource limitations. Hence, power-aware test strategies have been developed to optimize SoC testing under a power constraint; test scheduling is one such strategy. Test schedules for SoCs can be optimized to reduce test time while managing the power consumption. This talk will present a scheme for optimizing the test schedule of a SoC, for a given power constraint, by dynamically scaling the test clock and the supply voltage

Bio

Vijay Sheshadri is a doctoral student in the Department of Electrical and Computer Engineering at Auburn University. He is jointly advised by Professors Prathima and Vishwani Agrawal. Prior to joining Auburn University, Vijay obtained his M.S. degree in Electrical Engineering, in 2010, from Vanderbilt University. His research interests include Single Event Upsets in integrated circuits and Design-for-Testability of System-on-Chip devices. At present, Vijay's research focus is on Optimization of System-on-Chip (SoC) testing.

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