

# The Effects of Geometrical Scaling on the Frequency Response and Noise Performance of SiGe HBTs

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**Abstract**—We examine the geometrical scaling issues in SiGe HBT technology. Width scaling, length scaling, and stripe-number scaling are quantified from a radio frequency (RF) design perspective at 2 GHz. We conclude that a SiGe HBT with emitter area  $A_E = 0.5 \times 20 \times 6 \mu\text{m}^2$  is optimum for low noise applications at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$  using the design methodology, which guarantees optimal noise and input impedance matching with the simplest matching network. Finally, the optimal device sizes at  $f = 4, 6 \text{ GHz}$  for low noise applications are also obtained using the same method.

**Index Terms**—Geometrical scaling, low noise amplifier (LNA), noise figure, noise model, SiGe HBT.

## I. INTRODUCTION

WHILE vertical profile scaling of emerging SiGe HBT technologies has received significant recent attention, the design issues and tradeoffs associated with geometrical scaling of a given SiGe technology generation have not been explored in detail. This is particularly true with respect to radio frequency (RF) performance metrics, where an empirical approach to optimum device geometry is frequently adopted (i.e., measure a large matrix of device sizes to determine the best one). We attempt to shed light on these geometrical scaling issues in SiGe HBT technology by addressing the following question: Given a specific SiGe HBT technology generation (i.e., vertical doping and Ge profile fixed), what is the device geometry that best optimizes a given RF performance metric? In this work, we focus on the frequency response and broadband noise performance at the practical RF frequencies of 2, 4 and 6 GHz and which would be required in the development of a low noise amplifier (LNA), for instance. Our results are based on a commercial  $0.5 \mu\text{m}$  SiGe HBT technology [1], but our approach can be easily extended to any SiGe technology.

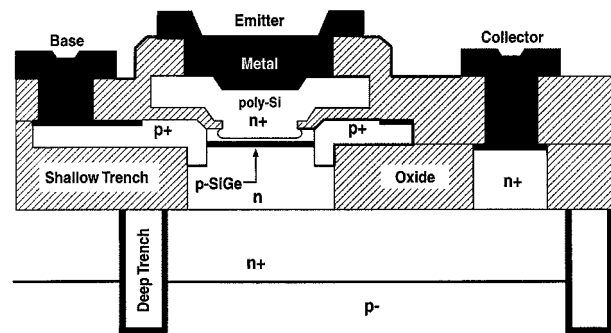


Fig. 1. Schematic cross-section of the UHV/CVD SiGe HBT.

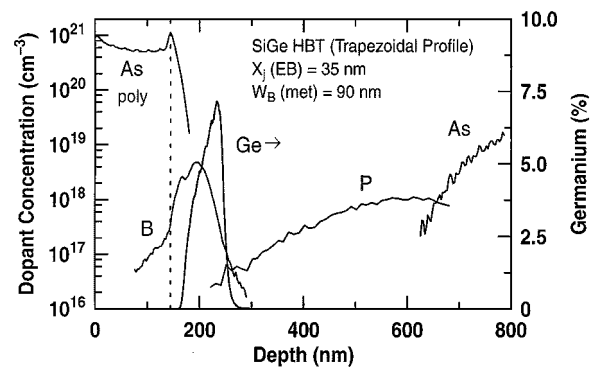


Fig. 2. Representative SIMS doping and Ge profiles of the UHV/CVD SiGe HBTs.

## II. DEVICE TECHNOLOGY AND PARAMETER EXTRACTION

The SiGe HBT was fabricated using a self-aligned epitaxial-base technology [1]. It has a planar structure and deep trench/shallow trench isolation, as shown in Fig. 1. The SiGe base is deposited in an ultrahigh-vacuum/chemical vapor deposition (UHV/CVD) low temperature epitaxy (LTE) system. The intrinsic collector was formed by a double ion implantation to realize high performance. Representative vertical doping and Ge profiles of the SiGe HBT are shown in Fig. 2.

There are in general three geometrical variables associated with scaling: emitter stripe width  $W$ , emitter stripe length  $L$ , and the number of stripes  $S$  of a given emitter stripe width and length. We present results on SiGe HBTs with:  $A_E = 0.3 \times 2.5 \mu\text{m}^2$ ,  $A_E = 0.4 \times 2.5 \mu\text{m}^2$ ,  $A_E = 0.6 \times 2.5 \mu\text{m}^2$  (variable  $W$ ),  $A_E = 0.5 \times 2.5 \mu\text{m}^2$ ,  $A_E = 0.5 \times 5 \mu\text{m}^2$ ,  $A_E = 0.5 \times 20 \mu\text{m}^2$  (variable  $L$ ),  $A_E = 0.5 \times 20 \times 2 \mu\text{m}^2$ ,  $A_E = 0.5 \times 20 \times 4 \mu\text{m}^2$ ,  $A_E = 0.5 \times 20 \times 8 \mu\text{m}^2$  (variable  $S$ ) and  $50 A_E = 0.5 \times 2.5 \mu\text{m}^2$  in parallel. These devices were measured

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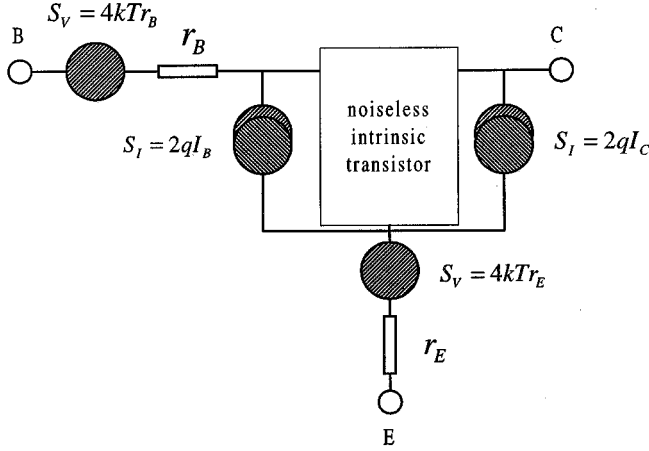


Fig. 3. Circuit schematic of the SPICE noise model.

at room temperature ( $T = 300$  K) using an HP4155 semiconductor parameter analyzer (dc) and an HP8510C vector network analyzer [scattering ( $S$ ) parameters]. The cutoff frequency  $f_T$ , the maximum oscillation frequency  $f_{max}$ , and the total emitter and base resistance  $r_{BE}$  of the devices were extracted from measured  $S$ -parameters, while the noise parameters (the minimum noise figure  $NF_{min}$ , the noise resistance  $R_n$ , and the optimum source reflection coefficient  $\Gamma_{S,opt}$ ) and the associated available gain  $G_{A,assoc}$  were obtained using the measured  $S$ -parameters and the appropriate noise model [2], [3].

### III. NOISE MODEL

Direct measurement of noise figure in the GHz range requires substantial experimental effort. An alternative approach is to measure the transistor  $S$ -parameters, convert to  $Y$ -parameters, and calculate the noise figure through an appropriate noise model [3], which relates the  $Y$ -parameters to the noise figure. Such an approach has been demonstrated and its accuracy verified in the SiGe HBT technology under study [3]. This model is accurate at the ranges of collector current density  $J_C = 0.05$ – $0.2$  mA/ $\mu\text{m}^2$  and frequency  $f = 2$ – $10$  GHz. At higher current densities (up to  $1$  mA/ $\mu\text{m}^2$ ), this model can still be used for the relative comparison, meaning that this model can determine which device has better noise performance. Fig. 3 illustrates the circuit schematic used in deriving the noise model. The principal noise sources in this model are the base and collector shot noise ( $2qI_B$ ,  $2qI_C$ ), emitter thermal noise, and base thermal noise. At a given bias and frequency, the noise figure (NF) is a function of the source admittance. The minimum noise figure ( $NF_{min}$ ) occurs at the optimum source admittance ( $Y_{S,opt}$ ). The equations for the minimum noise figure ( $NF_{min}$ ) and the optimum source admittance ( $Y_{S,opt}$ ) can be found in [3]. In noise measurements, the source reflection coefficient ( $\Gamma_{S,opt}$ ) is often used instead of the admittance  $Y_{S,opt}$

$$\Gamma_{S,opt} = \frac{1 - Y_{S,opt}Z_0}{1 + Y_{S,opt}Z_0} \quad (1)$$

where  $Z_0$  is the characteristic impedance.

TABLE I  
EFFECTS OF EMITTER WIDTH VARIATION

$A_E = W \times L$ ( $\mu\text{m}^2$ )	0.3×2.5	0.4×2.5	0.6×2.5
$\beta$ @ $J_C = 0.1$ mA/ $\mu\text{m}^2$	91	89	88
Peak $f_T$ (GHz)	43	46	50
Peak $f_{max}$ (GHz)	80	79	68
$\tau_{ec}$ (ps)	3.14	2.88	2.84
$C_{j,eb} + C_{j,cb}$ (fF)	21	24	29
$(C_{j,eb} + C_{j,cb})/A_E$ (fF/ $\mu\text{m}^2$ )	28	24	19.3
$r_{BE}$ ( $\Omega$ ) @ $J_C = 0.1$ mA/ $\mu\text{m}^2$	97	111	132

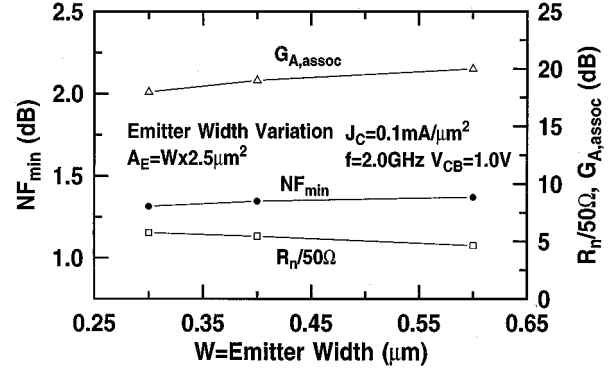


Fig. 4. Minimum noise figure  $NF_{min}$ , normalized noise resistance  $R_n$  (to  $50 \Omega$ ), and the associated available gain  $G_{A,assoc}$  versus emitter width at  $J_C = 0.1$  mA/ $\mu\text{m}^2$  and  $f = 2$  GHz.

Another important parameter is the associated available gain ( $G_{A,assoc}$ ), which is derived by noise matching at the input and power matching at the output

$$G_{A,assoc} = \left| \frac{Y_{21}}{Y_{11} + Y_{S,opt}} \right|^2 \frac{\text{Re}(Y_{S,opt})}{\text{Re}(Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_{S,opt}})} \quad (2)$$

### IV. RESULTS AND DISCUSSION

#### A. Emitter Width Variation

The effects of emitter width variation are given in Table I. As emitter width decreases from  $0.6$  to  $0.4 \mu\text{m}$ , the reduction of the base resistance leads to a considerable improvement in  $f_{max}$ . However, as emitter width decreases from  $0.4$  to  $0.3 \mu\text{m}$ ,  $f_{max}$  is almost unchanged mainly due to nonlinear scaling of total base-emitter resistance  $r_{BE}$  with emitter width, meaning as emitter width decreases, the intrinsic base resistance is no longer dominant in  $r_{BE}$  and the extrinsic base resistance becomes more important. Fig. 4 illustrates the emitter width dependence of the noise parameters of SiGe HBTs at  $f = 2$  GHz and  $J_C = 0.1$  mA/ $\mu\text{m}^2$ , the relevant collector current density for low noise applications. Although as the emitter width decreases,  $NF_{min}$  decreases slightly, both the noise resistance ( $R_n$ ) and the associated available gain ( $G_{A,assoc}$ ) are degraded slightly, which means that the smaller emitter width is not necessarily better at  $f = 2$  GHz and  $J_C = 0.1$  mA/ $\mu\text{m}^2$  for low noise applications. However, using constant power (constant collector current here) comparison (which is the case from design point of view),  $NF_{min}$  does improve considerably (about  $0.25$  dB at  $I_C = 0.1$  mA) as emitter width decreases at  $I_C \leq 0.2$  mA,

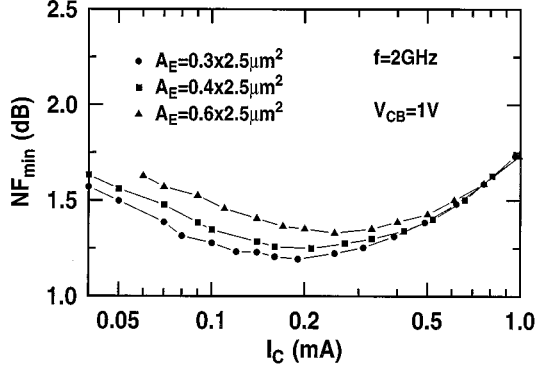


Fig. 5. Minimum noise figure  $NF_{min}$  versus collector current  $I_C$  for three devices with different emitter width at  $f = 2$  GHz.

TABLE II  
EFFECTS OF EMITTER LENGTH VARIATION

$A_E = W \times L$ ( $\mu m^2$ )	0.5x2.5	0.5x5	0.5x20
$\beta$ @ $J_C = 0.1 \text{ mA}/\mu m^2$	106	100	96
Peak $f_T$ (GHz)	51	53	54
Peak $f_{max}$ (GHz)	66	64	64
$\tau_{ec}$ (ps)	2.68	2.64	2.63
$C_{j,eb} + C_{j,cb}$ (fF)	20.2	40.1	148
$(C_{j,eb} + C_{j,cb})/A_E$ (fF/ $\mu m^2$ )	16.16	16.04	14.8
$r_{BE}$ ( $\Omega$ ) @ $J_C = 0.1 \text{ mA}/\mu m^2$	130	72.3	22.5

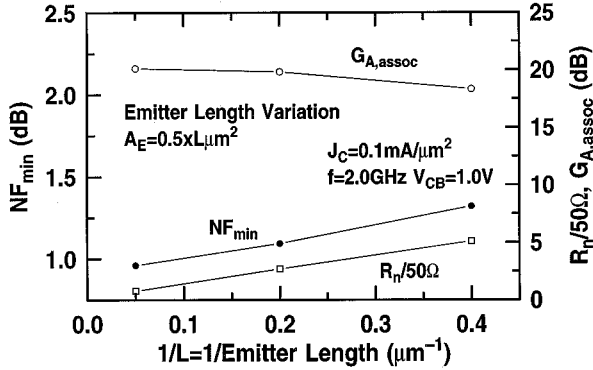


Fig. 6. Minimum noise figure  $NF_{min}$ , normalized noise resistance  $R_n$  (to  $50 \Omega$ ), and the associated available gain  $G_{A,assoc}$  versus reciprocal of emitter length at  $J_C = 0.1 \text{ mA}/\mu m^2$  and  $f = 2$  GHz.

as shown in Fig. 5. Another way to understand Fig. 5 is to plot  $NF_{min}$  versus  $J_C$  using the same data and it is not hard to image that as emitter width decreases,  $NF_{min}$  are very close at  $J_C \leq 0.2 \text{ mA}/\mu m^2$ , but  $NF_{min}$  decreases significantly at  $J_C \geq 0.3 \text{ mA}/\mu m^2$ . Therefore, smaller emitter width does improve  $NF_{min}$  at higher current densities or using constant power comparison.

### B. Emitter Length Variation

Table II compares typical transistor parameters for emitter length variations. As expected, the changes of  $f_T$  and  $f_{max}$  are small as emitter length varies. Fig. 6 gives the emitter length dependence of the noise parameters of the SiGe HBTs at  $J_C = 0.1 \text{ mA}/\mu m^2$  and  $f = 2$  GHz. As emitter length increases from  $2.5 \mu m$  to  $20 \mu m$ ,  $NF_{min}$  is reduced by a considerable amount (0.3 dB) and  $R_n$  and  $G_{A,assoc}$  are also improved. Therefore, a

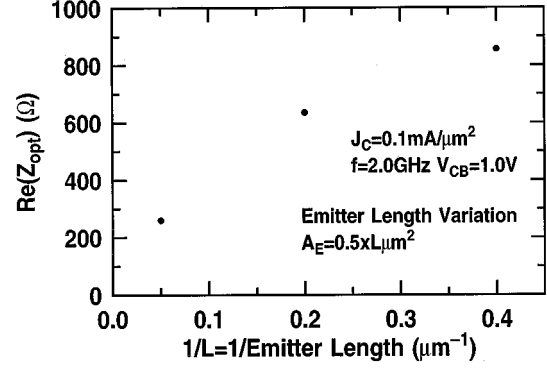


Fig. 7. Real part of the optimum source impedance as a function of reciprocal of emitter length at  $J_C = 0.1 \text{ mA}/\mu m^2$  and  $f = 2$  GHz.

TABLE III  
EFFECTS OF EMITTER STRIPE NUMBER VARIATION

$A_E = W \times L \times S$ ( $\mu m^2$ )	0.5x20x2	0.5x20x4	0.5x20x8
$\beta$ @ $J_C = 0.1 \text{ mA}/\mu m^2$	104	101	100
$f_T$ @ $J_C = 0.1 \text{ mA}/\mu m^2$ (GHz)	23	22.8	22.5
$f_{max}$ @ $J_C = 0.1 \text{ mA}/\mu m^2$ (GHz)	41	40.5	37.9
$\tau_{ec}$ (ps)	2.7	2.8	2.9
$C_{j,eb} + C_{j,cb}$ (fF)	324	625	1336
$(C_{j,eb} + C_{j,cb})/A_E$ (fF/ $\mu m^2$ )	16.2	15.6	16.7
$r_{BE}$ ( $\Omega$ ) @ $J_C = 0.1 \text{ mA}/\mu m^2$	11.4	6.1	3.8

device with longer emitter length has better noise performance at  $J_C = 0.1 \text{ mA}/\mu m^2$  and  $f = 2$  GHz and thus it is preferred for LNA design. On the other hand, the real parts of the optimized source impedance  $Re(Z_{opt})$  of these devices, as shown in Fig. 7, are well above  $50 \Omega$ . Since substrate and interconnect losses are significantly higher in Si than in GaAs, Si RF circuit designs should target the optimization of the size of the transistors in order to simplify matching, rather than design the matching circuit around a given transistor [2]. Therefore, in the design of an Si LNA,  $Re(Z_{opt})$  of the transistor is usually chosen to be close to  $50 \Omega$  so that the transistor becomes noise-matched to the characteristic impedance of the system, typically  $50 \Omega$ , at the desired frequency. Therefore, devices with multiple stripes are often needed for low noise applications.

### C. Emitter Stripe Number Variation

Table III compares typical transistor parameters for emitter stripe number variations. For the device with  $A_E = 0.5 \times 20 \times 8 \mu m^2$ ,  $f_{max}$  at  $J_C = 0.1 \text{ mA}/\mu m^2$  is slightly lower mainly due to nonlinear scaling of total base-emitter resistance  $r_{BE}$  with the reciprocal of the stripe number  $1/S$ . Since other parameters such as  $\beta$ ,  $f_T$ ,  $C_j/A_E$  and  $\tau$  of the device with  $A_E = 0.5 \times 20 \times 8 \mu m^2$  are either worse or comparable with those of other two devices with 2 and 4 stripe numbers, we expect that the device with 8 stripe number has worse noise performance than those of the devices with 2 and 4 stripe numbers.

Fig. 8 gives the emitter stripe number dependence of  $Re(Z_{opt})$  at  $J_C = 0.1 \text{ mA}/\mu m^2$  and  $f = 2$  GHz, from which the optimized device area ( $A_E = 0.5 \times 20 \times 6 \mu m^2$ , referred to as device A) to match  $50 \Omega$  is extracted. Basically, we can choose any unit cell as a building block ( $A_E = 0.5 \times 20 \mu m^2$  or  $A_E = 0.5 \times 2.5 \mu m^2$ ) to get this optimized device area.

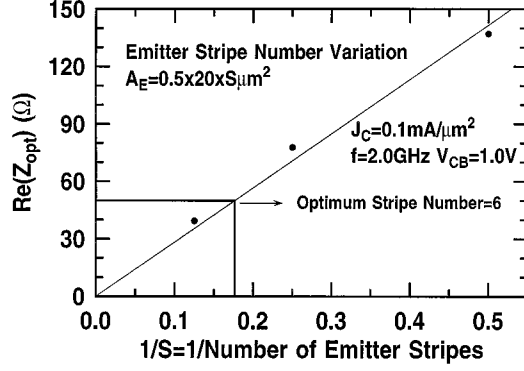


Fig. 8. Real part of the optimum source impedance as a function of reciprocal of emitter stripe number at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$ .

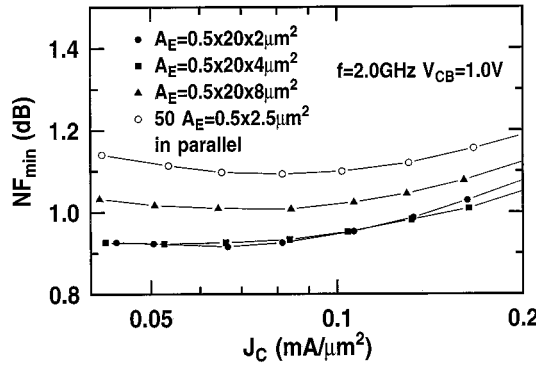


Fig. 9. Minimum noise figure versus collector current density for four different devices at  $f = 2 \text{ GHz}$ .

50  $A_E = 0.5 \times 2.5 \mu\text{m}^2$  transistors in parallel (referred to as device B with  $A_E = 0.5 \times 2.5 \times 50 \mu\text{m}^2$ , which can be viewed as a device with 50  $0.5 \times 2.5 \mu\text{m}^2$  stripes), for instance, has a similar optimized device area and at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$  its  $\text{Re}(Z_{\text{opt}})$  is  $47.75 \Omega$ , which is very close to  $50 \Omega$ . Although both device A and device B can match  $50 \Omega$  very well, the  $\text{NF}_{\text{min}}$  of device A is at least  $0.1 \text{ dB}$  smaller than that of device B at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$ , which can be seen in Fig. 9, which is consistent with the conclusion that longer emitter length is preferred for LNA design at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$ .

To understand the differences in  $\text{NF}_{\text{min}}$  observed in Fig. 9, the contributions of the various noise sources need to be investigated. Any linear noisy two-port can be represented by its noiseless counterpart, an input current noise source  $i_n$ , an input voltage noise source  $v_n$ , and their correlation [4]. Basically,  $\text{NF}_{\text{min}}$  is determined by  $i_n$  and  $v_n$  [5], and the smaller  $i_n$  and  $v_n$  are, the smaller  $\text{NF}_{\text{min}}$  is.  $i_n$  and  $v_n$  are given by [5]

$$\langle i_n^2 \rangle = 2qI_B + \frac{2qI_C}{|h_{21}|^2} \quad (3)$$

$$\langle v_n^2 \rangle = 4kTr_{BE} + \frac{2qI_C}{|y_{21}|^2}. \quad (4)$$

In order to compare devices with  $A_E = 0.5 \times 20 \times 2 \mu\text{m}^2$ ,  $A_E = 0.5 \times 20 \times 4 \mu\text{m}^2$ ,  $A_E = 0.5 \times 20 \times 8 \mu\text{m}^2$  and device

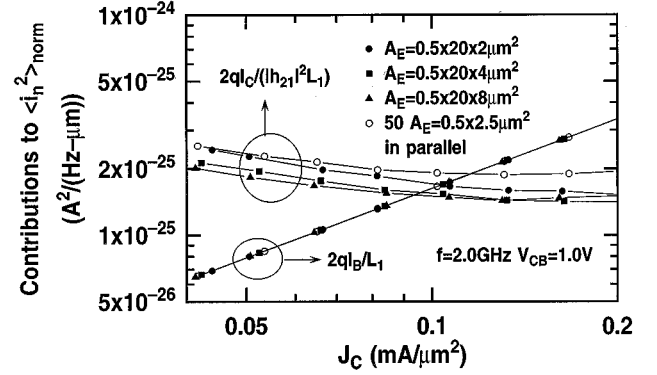


Fig. 10.  $2qI_B/L_1$  and  $2qI_C/(|h_{21}|^2 L_1)$  contributions to  $\langle i_n^2 \rangle_{\text{norm}}$  versus collector current density at  $f = 2 \text{ GHz}$  for four different devices.

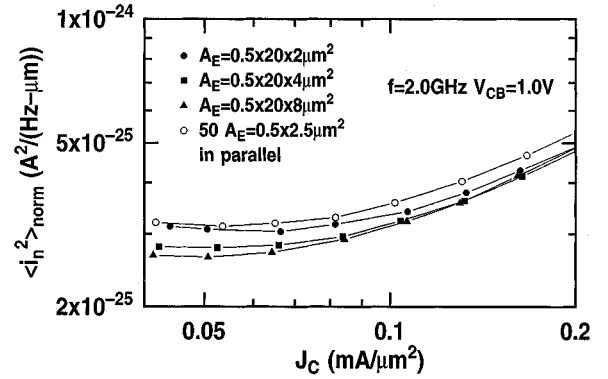


Fig. 11.  $\langle i_n^2 \rangle_{\text{norm}}$  versus collector current density at  $f = 2 \text{ GHz}$  for four different devices.

B with  $A_E = 0.5 \times 2.5 \times 50 \mu\text{m}^2$ ,  $\langle i_n^2 \rangle$  and  $\langle v_n^2 \rangle$  need to be normalized by the total emitter length  $L_1$  of the device

$$\langle i_n^2 \rangle_{\text{norm}} \equiv \frac{\langle i_n^2 \rangle}{L_1} = \frac{2qI_B}{L_1} + \frac{2qI_C}{|h_{21}|^2 L_1} \quad (5)$$

$$\langle v_n^2 \rangle_{\text{norm}} \equiv \langle v_n^2 \rangle \times L_1 = 4kTr_{BE}L_1 + \frac{2qI_C L_1}{|y_{21}|^2} \quad (6)$$

where  $L_1$  is the product of the emitter length of a single emitter stripe and the emitter stripe number.

Fig. 10 compares the  $2qI_B/L_1$  and  $2qI_C/(|h_{21}|^2 L_1)$  contributions to  $\langle i_n^2 \rangle_{\text{norm}}$  and Fig. 11 gives  $\langle i_n^2 \rangle_{\text{norm}}$  as a function of collector current density at  $f = 2 \text{ GHz}$  for these four different devices. Since the current gain in the RF bias region is similar for these four devices, the  $2qI_B/L_1$  contributions of these four devices are very close, while the  $2qI_C/(|h_{21}|^2 L_1)$  contribution of device B is the largest among these four devices because of its smallest  $|h_{21}|$ . Therefore device B has the largest  $\langle i_n^2 \rangle_{\text{norm}}$  among these four devices.

Fig. 12 illustrates the  $4kTr_{BE}L_1$  and  $2qI_C L_1/|y_{21}|^2$  contributions to  $\langle v_n^2 \rangle_{\text{norm}}$  and Fig. 13 shows  $\langle v_n^2 \rangle_{\text{norm}}$  as a function of collector current density at  $f = 2 \text{ GHz}$  for these four different devices. The higher  $\langle v_n^2 \rangle_{\text{norm}}$  of device B and device with  $A_E = 0.5 \times 20 \times 8 \mu\text{m}^2$  is mainly due to the larger  $4kTr_{BE}L_1$  contributions of these two devices, which lead to their larger  $\text{NF}_{\text{min}}$  (Fig. 9). As shown in Fig. 12, the  $4kTr_{BE}L_1$  contribution dominates  $\langle v_n^2 \rangle_{\text{norm}}$  across most of the bias current range,

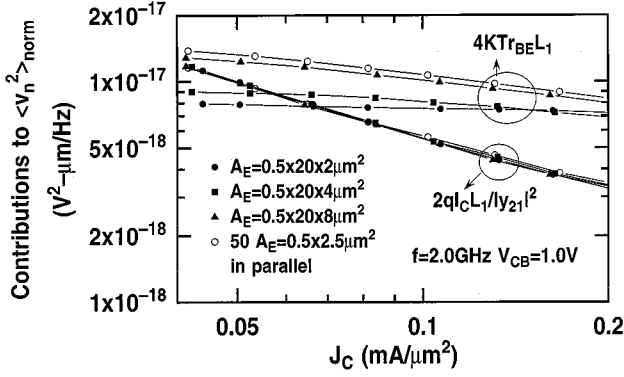


Fig. 12.  $4KT_{BE}L_1$  and  $2qI_C L_1/|y_{21}|^2$  contributions for  $\langle v_n^2 \rangle_{\text{norm}}$  versus collector current density at  $f = 2$  GHz for four different devices.

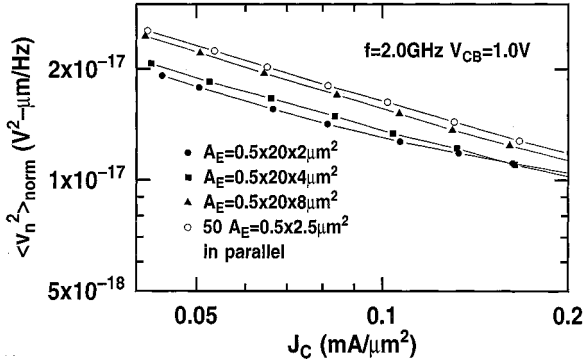


Fig. 13.  $\langle v_n^2 \rangle_{\text{norm}}$  versus collector current density at  $f = 2$  GHz for four different devices.

indicating significant improvement of noise performance can be expected by increasing the base doping [5]. From this analysis, the higher  $\text{NF}_{\min}$  of device B is due to the larger  $\langle v_n^2 \rangle_{\text{norm}}$  and  $\langle i_n^2 \rangle_{\text{norm}}$  compared to those of the other three devices. Therefore, the current gain, the cutoff frequency and the total base and emitter resistance need to be improved to reduce the minimum noise figure.

For low noise applications, not only  $\text{NF}_{\min}$  is important, but also  $\Delta f$ , which is the difference between  $\text{NF}_{\min}$  and  $\text{NF}$  for  $50 \Omega$  source impedance and is given by [6]

$$\Delta f = \frac{4r_n |\Gamma_{S,\text{opt}}|^2}{|1 + \Gamma_{S,\text{opt}}|^2} \quad (7)$$

where  $r_n = R_n/50$ ,  $\Gamma_{S,\text{opt}}$  is the optimum source reflection coefficient, and  $R_n$  is the noise resistance.

Fig. 14 shows  $\Delta f$  versus  $J_C$  for the four different devices. We see that device A and device B have similar  $\Delta f$  at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$ . Therefore, we conclude that a SiGe HBT with  $A_E = 0.5 \times 20 \times 6 \mu\text{m}^2$  is the optimized device at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $f = 2 \text{ GHz}$  for low noise applications.

Using the same method, the optimized transistor sizes at any frequencies and any biases can be found. Table IV summarizes the frequency performance and noise performance of the optimal device sizes at  $f = 2, 4, 6 \text{ GHz}$  for LNA applications. For the device with  $A_E = 0.5 \times 20 \times 2 \mu\text{m}^2$ , even at  $f = 6 \text{ GHz}$  and  $J_C = 0.16 \text{ mA}/\mu\text{m}^2$ , the noise figure is still 2.0 dB and the associate available gain can reach 14 dB.

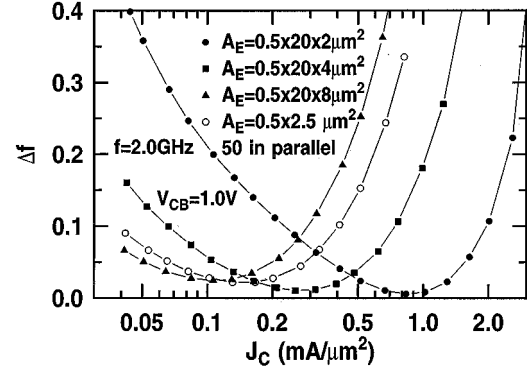


Fig. 14.  $\Delta f$  versus collector current density for four different devices.  $\Delta f$  is the difference between the minimum noise figure and the noise figure for  $50 \Omega$  source impedance.

TABLE IV  
HIGH-FREQUENCY PERFORMANCE OF THE OPTIMAL DEVICES AT  $f = 2, 4$ ,  
AND  $6 \text{ GHz}$  FOR LNA APPLICATIONS

	SiGe HBT	SiGe HBT	SiGe HBT
	2 GHz	4 GHz	6 GHz
$A_E = W \times L \times S (\mu\text{m}^2)$	$0.5 \times 20 \times 6$	$0.5 \times 20 \times 4$	$0.5 \times 20 \times 2$
$J_C (\text{mA}/\mu\text{m}^2)$	0.1	0.13	0.16
and $V_{CB} = 1\text{ V}$			
$f_T (\text{GHz})$	~ 22	27	29.4
$f_{\max} (\text{GHz})$	~ 40	44.3	47.8
$\text{NF}_{\min} (\text{dB})$	~ 0.95	1.33	1.78
$\text{NF}_{50} (\text{dB})$	~ 1.04	1.49	2.01
$R_n (\Omega)$	~ 7	9	17
$G_{A,\text{assoc}} (\text{dB})$	~ 19	15.36	14

## V. SUMMARY

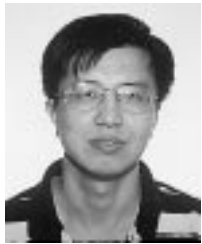
Geometrical scaling issues including width scaling, length scaling and stripe number scaling are investigated from an RF design perspective. Since the optimization of the size of the transistors in Si RF circuit designs is crucial, we use a method that can optimize the emitter geometry in order to minimize the matching circuit losses and overall noise figure. This method not only can choose a device, which can match  $50 \Omega$  very well, it can also select a device with smaller minimum noise figure, which will improve the noise performance. In real LNA design (assuming  $50 \Omega$  system), after choosing this optimized transistor, both base inductance and emitter inductance are also needed. In general, base inductance is mainly used to offset the imaginary part of  $Z_{\text{opt}}$ , while the emitter inductance is mainly designed to make the real part of the input impedance  $\text{Re}(Z_{\text{in}}) = 50 \Omega$  (assuming  $50 \Omega$  system). If both base inductance and emitter inductance are more carefully designed, close to simultaneously noise matching and power matching can be realized. Using this method, we conclude that a SiGe HBT with emitter area  $A_E = 0.5 \times 20 \times 6 \mu\text{m}^2$  is optimum device geometry for low noise applications at  $J_C = 0.1 \text{ mA}/\mu\text{m}^2$  and  $2 \text{ GHz}$ , while  $A_E = 0.5 \times 20 \times 4 \mu\text{m}^2$  and  $A_E = 0.5 \times 20 \times 2 \mu\text{m}^2$  are the optimal device sizes at  $4 \text{ GHz}$  and  $6 \text{ GHz}$ , respectively.

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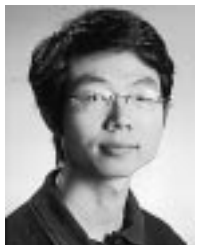
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