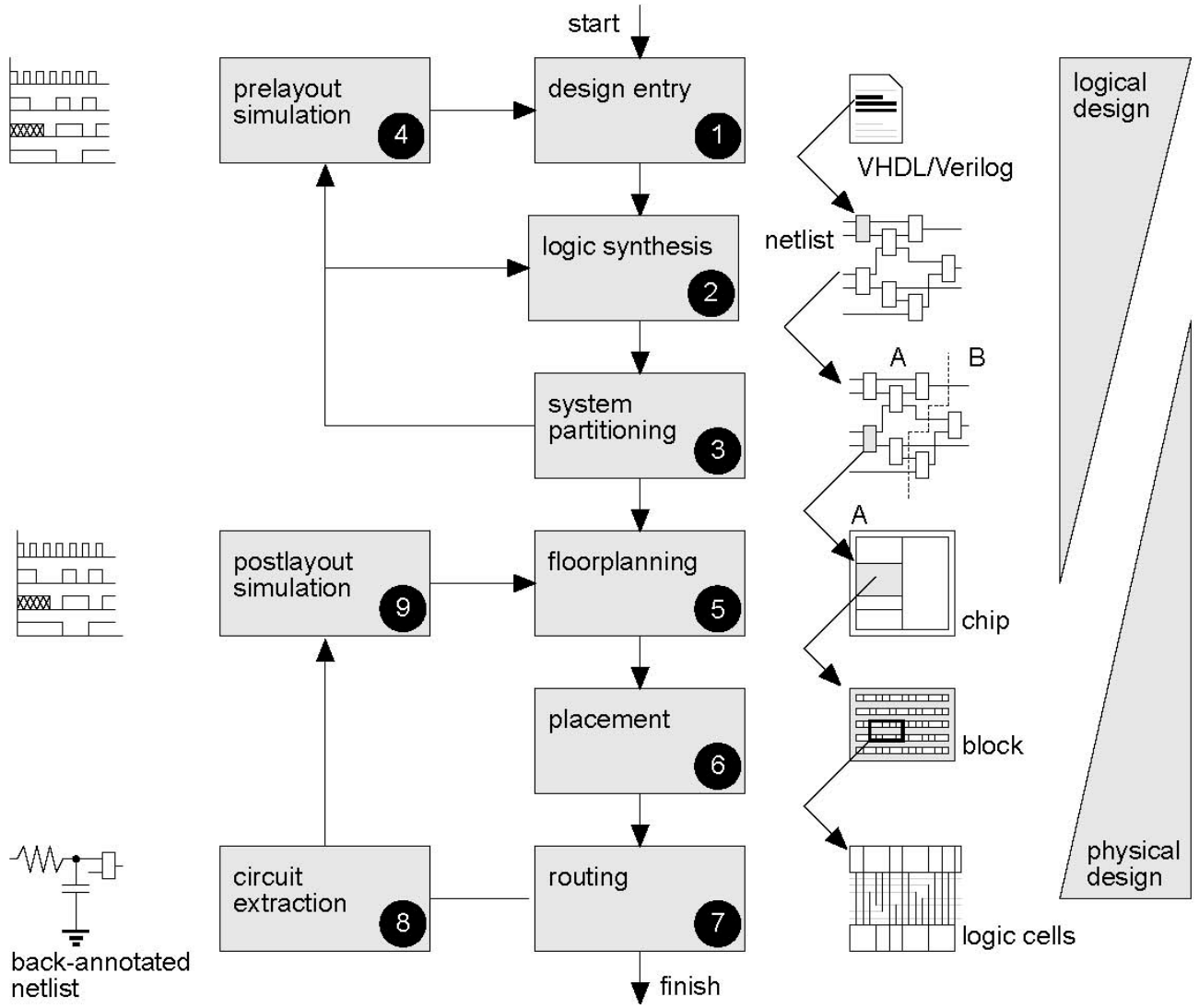
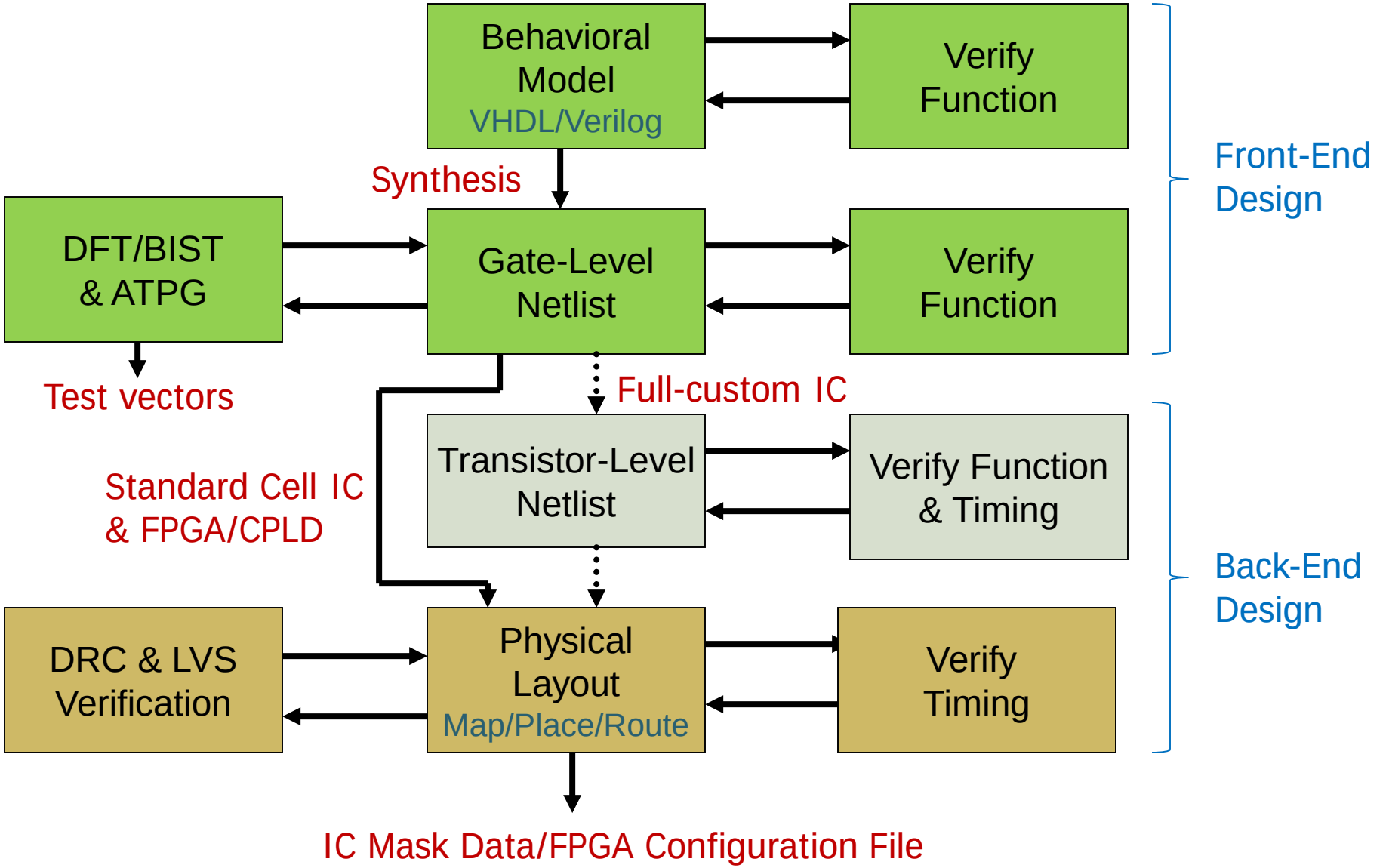
ASIC Computer-Aided Design Flow

ELEC 5250/6250

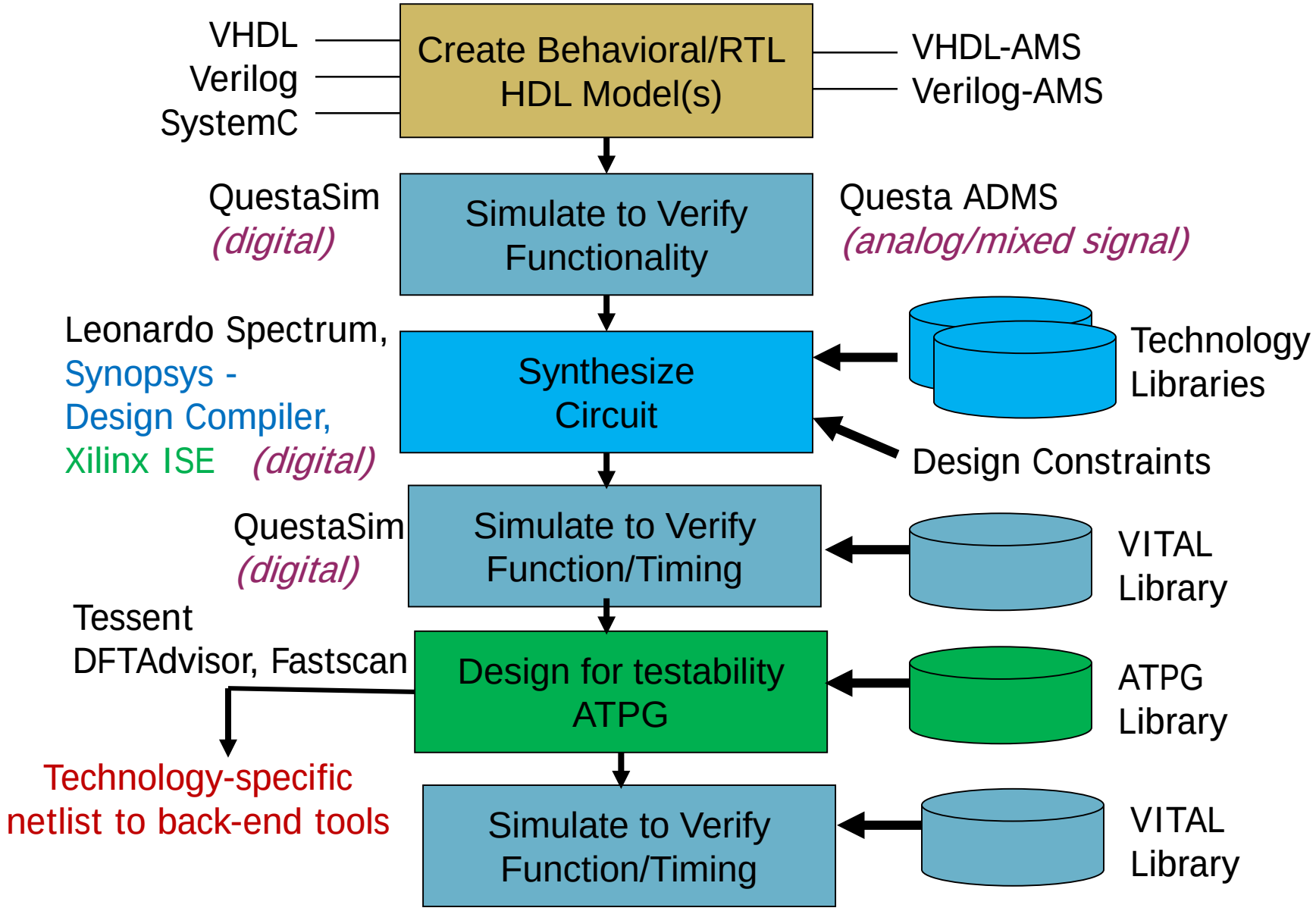
ASIC Design Flow



ASIC Design Flow



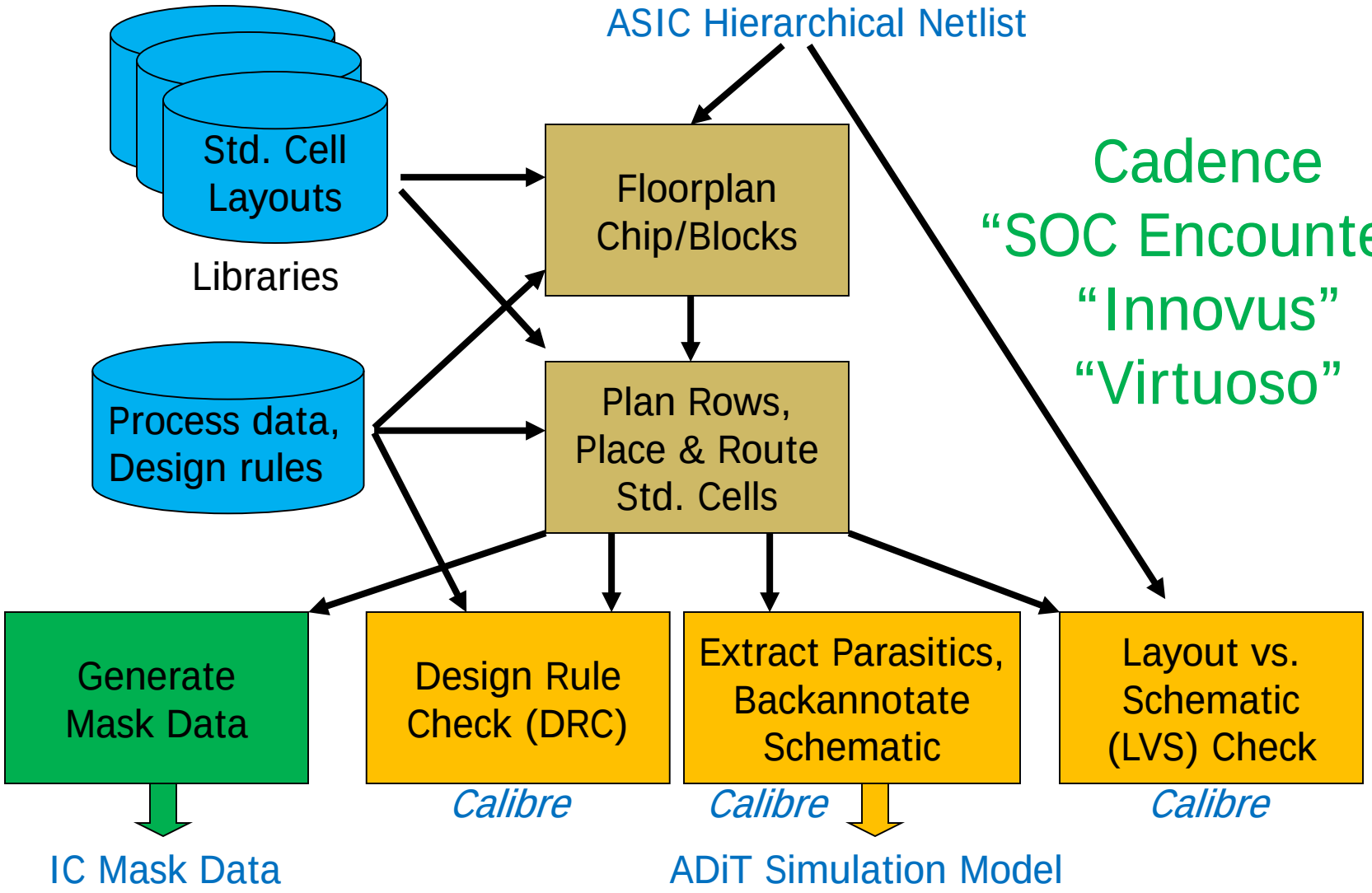
“Front-End” Design & Verification



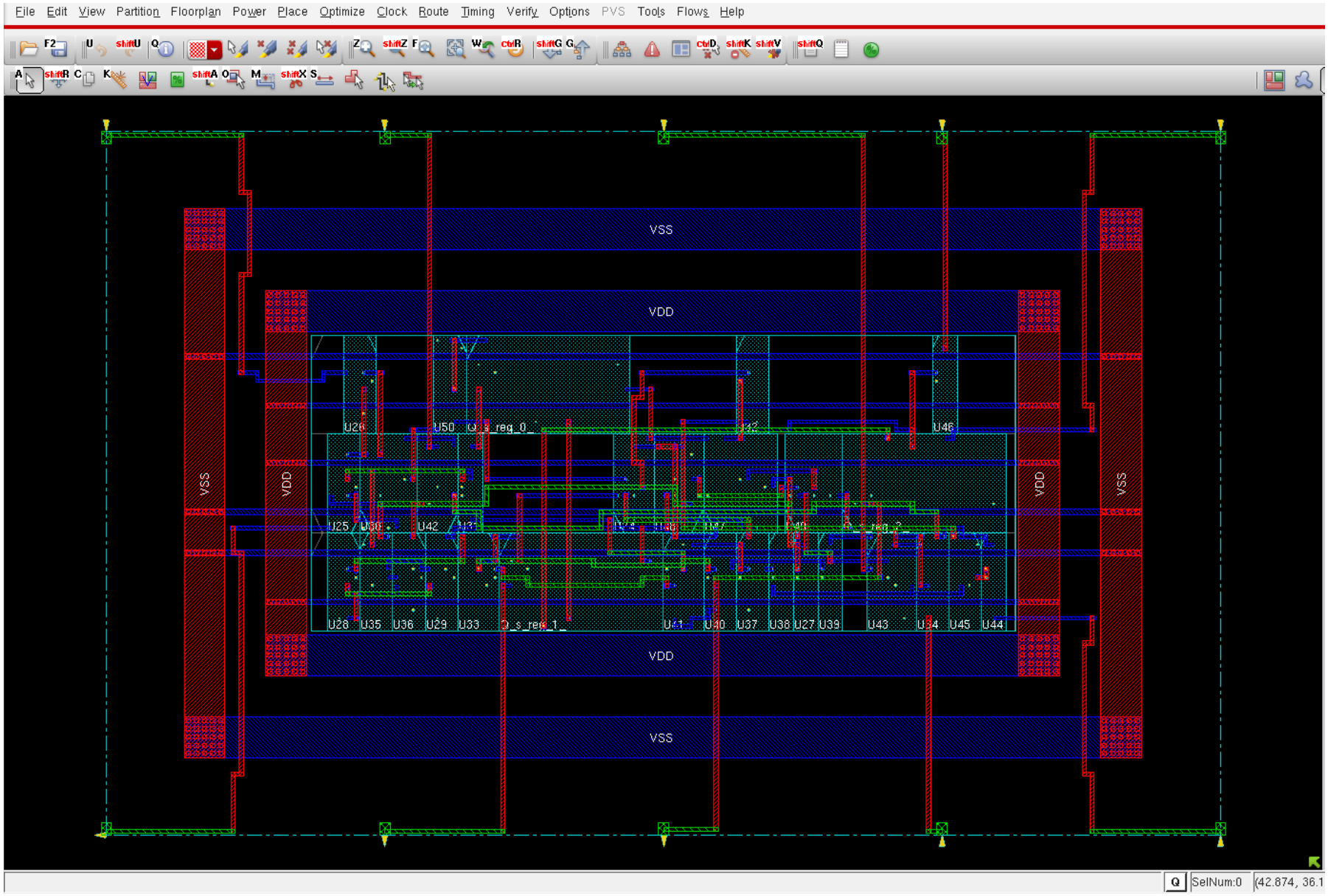
ASIC “back end” (physical) design

Assume digital blocks/standard cells

(can also do full custom layout, IP blocks, mixed-signal blocks, etc.)



Cadence SOC Encounter – Mod7 Counter Layout



Cadence Virtuoso - Chip layout

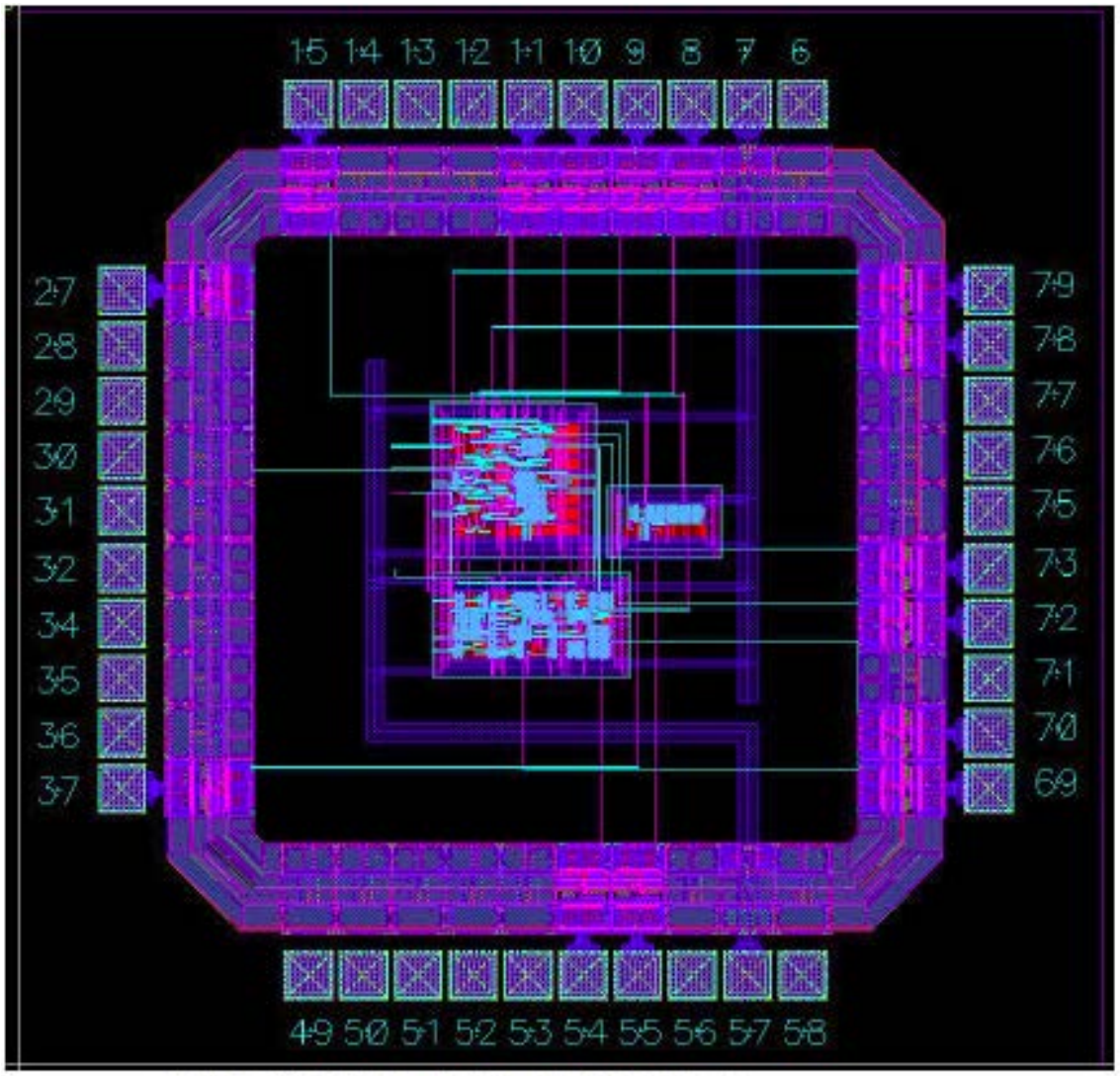


Figure 12.22: Frame and core after routing in *Virtuoso*

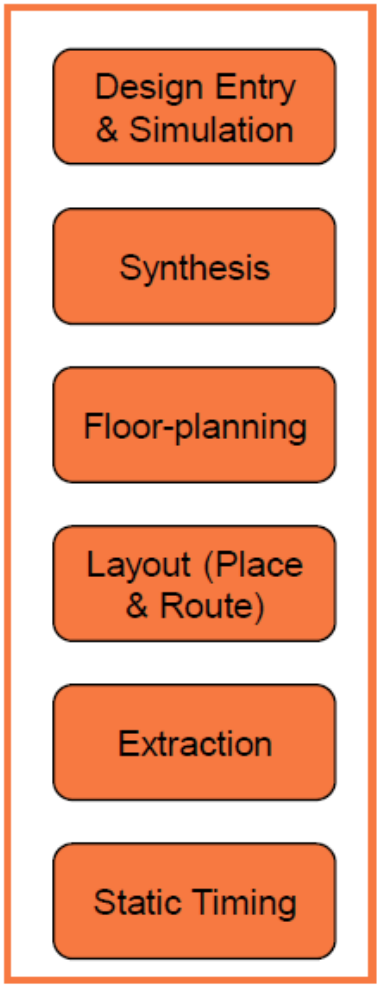
From
E. Brunvand
Book

ASIC CAD tools available in ECE

- **Modeling and Simulation**
  - Modelsim, Questa-ADMS, Eldo, ADiT (Mentor Graphics)
  - Verilog-XL, NC_Verilog, Spectre (Cadence)
  - Active-HDL (Aldec)
- **Design Synthesis (digital)**
  - Leonardo Spectrum (Mentor Graphics)
  - Design Compiler (Synopsys), RTL Compiler (Cadence)
- **Design for Test and Automatic Test Pattern Generation**
  - Tessent DFT Advisor, Fastscan, SoCScan (Mentor Graphics)
- **Schematic Capture & Design Integration**
  - Pyxis Design Architect-IC (Mentor Graphics)
  - Design Framework II (DFII) - Composer (Cadence)
- **Physical Layout**
  - Pyxis IC Station (Mentor Graphics)
  - SOC Encounter, Virtuoso (Cadence)
- **Design Verification**
  - Calibre DRC, LVS, PEX (Mentor Graphics)
  - Diva, Assura (Cadence)

IC Process Design Kits (PDKs)

- **Foundry-specific** data and models for a specific IC technology
  - Used by the design tools
- **Design components** for both front-end & back-end design
  - Design entry/modeling
  - Technology/process data
    - Layer definitions/parameters (Trans, R,C,…)
    - Design rules
  - Standard Cell Library
    - Synthesis library
    - Simulation models (Verilog, transistor)
    - Physical designs (LEF models)
    - Timing models (fast, typical, slow)
  - Verification (DRC,LVS,PEX)
  - DFT/test generation
  - IP and device generators (RAM, etc.)



Global Foundries BiCMOS8HP 130nm PDK

Standard Cell Library Directory Structure

./cdl	**CDL netlist for LVS checking**
./doc	**SC datasheets, test spec and change log**
./gds2	**GDS2 for Standard cell library**
./layermap	**Local copy of the PDK bicmos8hp.layermap**
	(prBoundary layer has been added)
./lef	**LEF for Standard cell library**
./sch_netlist	**Schematic netlists for simulation**
./symbol_61	**CADENCE OA symbol views**
./synopsys	**Standard Synthesis Timing Models**
./verilog	**Verilog behavioral models**
.README	

Global Foundries BiCMOS8HP 130nm PDK

Standard Cell Library: Basic Standard Cells

- **Primitive Logic**
  - NAND, NOR, INVERT, etc.
- **Unique Logic**
  - ADDF – Full Adder
  - CLK – Clock Driver
  - COMP2 – 2-Bit Comparator
  - MUX21 – 2:1 Multiplexer
  - DECAP – Decoupling Cap
- **Physical Design Cells**
  - FILLx (row fill cells, x=1,2,4,8,...,128)
  - FGTIE (floating-gate tie-down)
  - NWSX (substrate and n-well taps)
- **Complex Logic**
  - AO21, OA21, etc.
- **Sequential Logic**
  - DFF – D Flip-Flop
  - LATSR – Latch Set/Reset
  - SDFF – Scanable D Flip-Flop
- **Types of I/O cells available**
  - Wirebond Standard Basic IO Cells
  - C4 Standard Basic IO Cells

I/O

Global Foundries PDK Directory Structure

IBM_PDK/bicmos8hp/<version>/

Subdirectory	Contents
doc/	Technology Design Manual Model Reference Guide Layer Mapping File
cdslib/bicmos8hp	Cadence BiCMOS8HP Device Library (IC61)
/esd8hp	Cadence BiCMOS8HP ESD Library
/Skill	Context Files (Skill Utilities)
/examples	Example Setup Files
/doc	Cadence Library Documentation
Assura/DRC	DRC Files
/LVS	LVS Files
/doc	Assura Release Notes
EM/	Electromagnetic Enablement
/doc	E-M File Release Notes and Guide
/EMX	EMX Proc Files
/Momentum	Momentum Layer and Substrate Files
HSPICE/models	HSPICE Device Model Files
/doc	HSPICE Release Notes
Spectre/models	Spectre (Direct) Device Model Files
/doc	Spectre Release Notes
utils/	Kit Utility Programs

NCSU Cadence Design Kit (CDK)

https://www.eda.ncsu.edu/wiki/NCSU_CDK

- For analog/digital CMOS IC design via the MOSIS IC fabrication service (www.mosis.org)
  - Version ncsu-cdk-1.6.0.beta for Cadence Virtuoso 6.1 and later
- Supports all MOSIS processes based on SCMOS rules
  - **ami_06**/16, hp_04/06, tsmc_02/03/04
  - GDSII layer maps
  - Diva DRC, LVS support (no PEX)
  - Composer interfaces to HSPICE/Spectre, Verilog
  - Technology-independent libraries for analog & digital parts
    - Transistor models, layouts, etc.
    - But – does not include standard cell layout library
  - MOSIS wirebond pads (AMI 0.6µm, TSMC 0.4 µm, HP 0.6µm)

Installed in /class/ELEC6250/ncsu-cdk-1.6.0.beta

U. of Utah CDK (used in Dr. Brunvand's book)

/class/ELEC6250/UofUtah/

- **UofU_TechLib_ami06** UofU-modified tech library for AMI C5N 0.5 micron CMOS process, in the NCSU CDK framework

  (AMI acquired by ON Semiconductor for $915M in 2008)

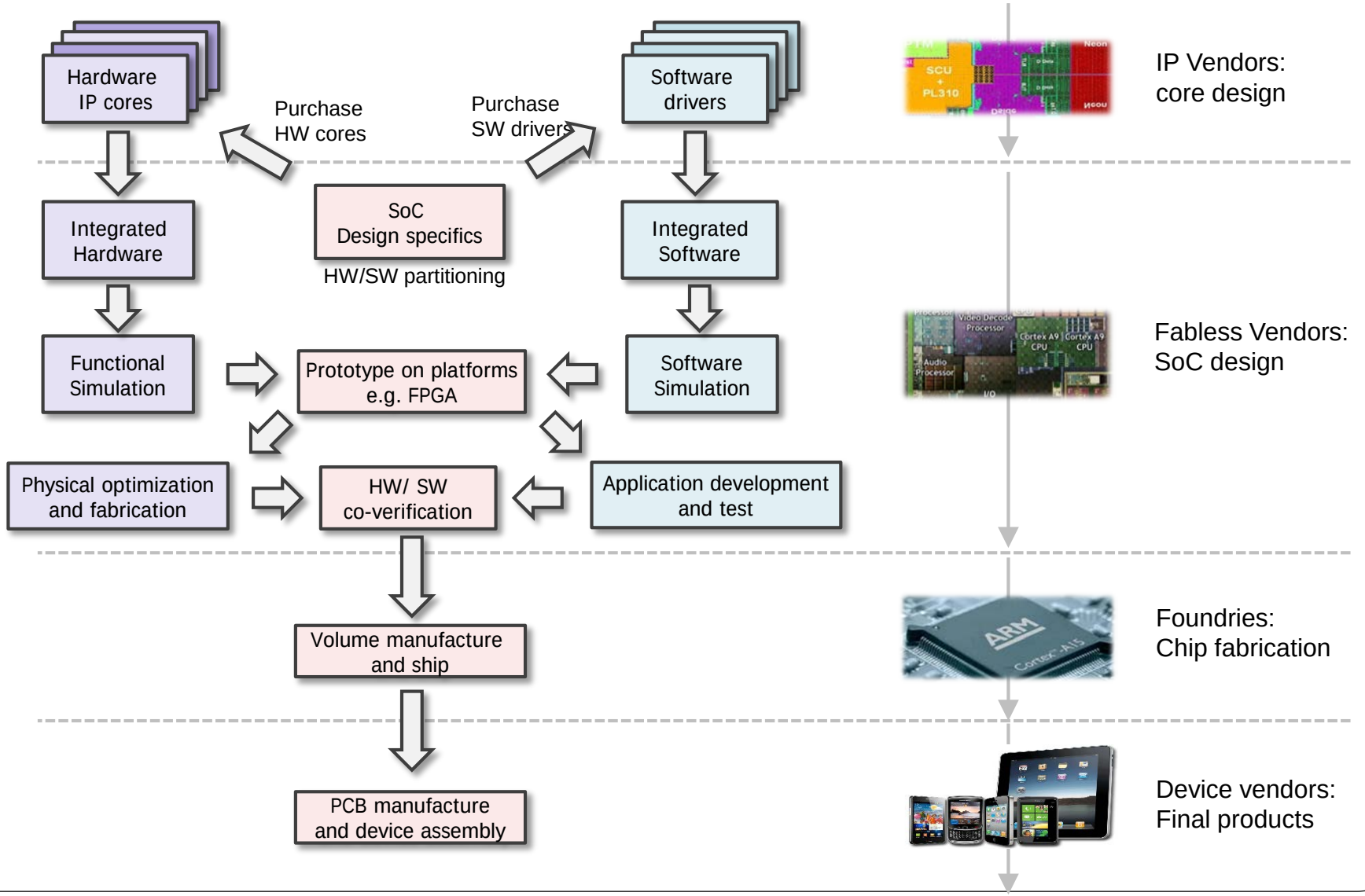
- **UofU_Digital_v1_2** Std. Cell library (37 cells, use M1 & M2)
  - UofU_Digital_v1_2.db: compiled library file for Synopsys Design Compiler
  - UofU_Digital_v1_2.lef: abstract layout information file for place and route tools
  - UofU_Digital_v1_2.lib: library characterization file
  - UofU_Digital_v1_2.v: Verilog interface and simulation behavior file
  - UofU_Digital_v1_2_behv.v: Verilog models with timing "specify" blocks
- **UofU_Pads** Pad cells and frames based on the MOSIS-supplied .5µm pads from Tanner, but UofU-modified to pass DRC and LVS
- **UofU_AnalogParts** UofU-modified transistor models that add delay to the switch-level simulation of those devices

UofU_Digital_v1_2 CMOS cell library

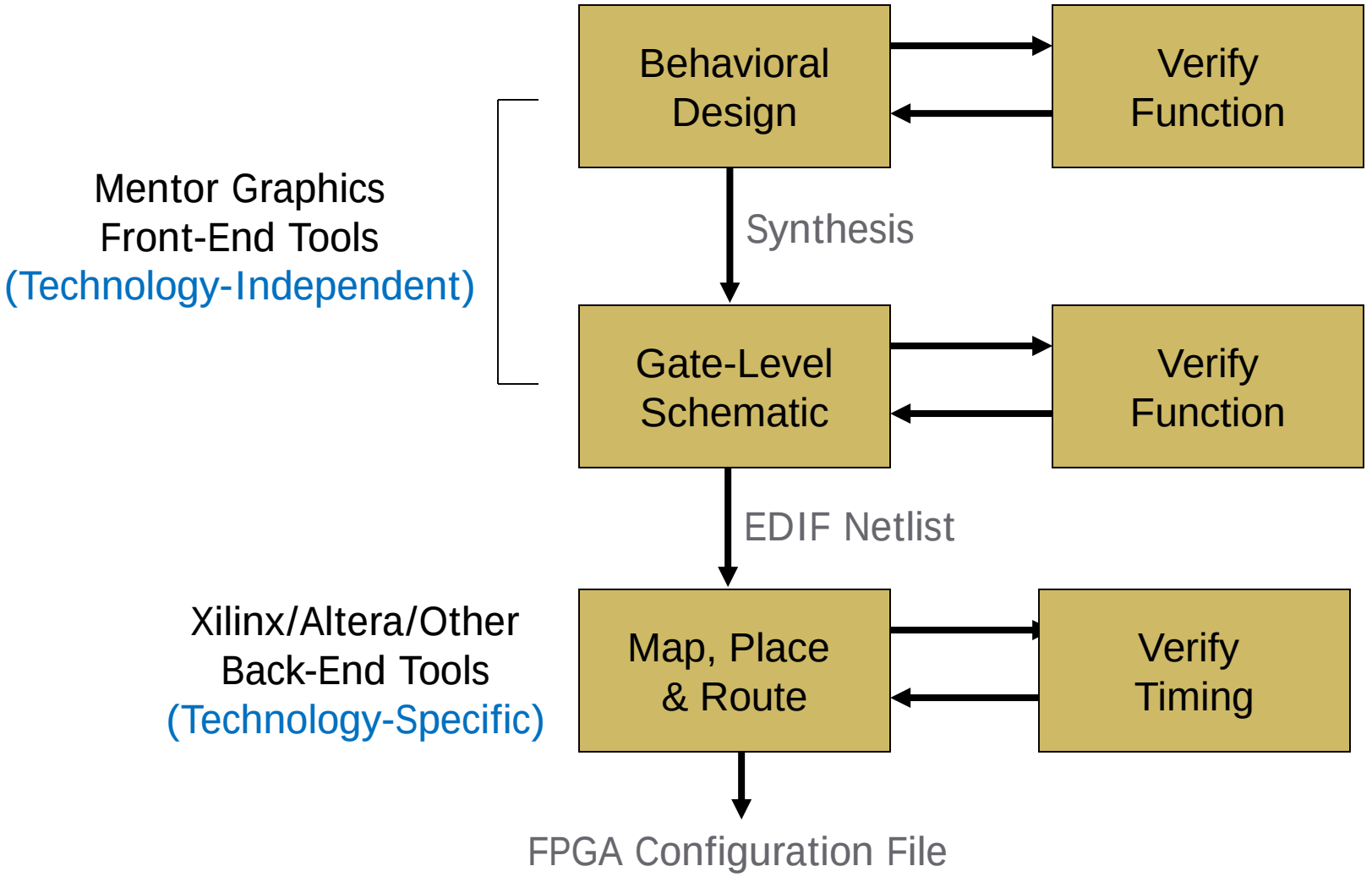
- AND3X1: 3-input AND
- AOI21X1, AOI22X1: AND-OR-Invert gates
- BUFX2, BUFX4, BUFX8: non-inverting buffers
- DCBNX1, DCBX1, DCNX1, DCX1: D-type flip flops with active-low clear.
  B means that the device includes both Q and QB outputs.
  N means active-low clock.
- ENINVX1, ENINVX2: enabled (tri-state) inverters
- FILL, FILL2, FILL4, FILL8: filler cells of different widths for filling in std cell rows
- INVX1, INVX16, INVX2, INVX4, INVX8: inverters
- LCNX1, LCX1: level-sensitive (gated) latches with active-low clear.
  N means active-low gate
- MUX2NX1, MUX2X2: 2-way muxes. N means an inverting mux
- NAND2X1, NAND2X2, NAND3X1: NAND gates with 2 and 3 inputs
- NOR2X1, NOR2X2, NOR3X1: NOR gates with 2 and 3 inputs
- OAI21X1 OAI22X1: OR-AND-Invert gates
- TIEHI, TIELO: Cells used to tie inputs high or low
- XNOR2X1: 2-input XNOR
- XOR2X1: 2-input XOR

Xn = drive strength

SoC Design Flow (Using IP cores)



FPGA Design Flow



Xilinx/Altera FPGA/CPLD Design Tools

- Simulate designs in ***Modelsim*** *(or other simulation tools)*
  - Behavioral/RTL models (VHDL, Verilog)
  - Synthesized netlists (VHDL, Verilog)
    - Requires "primitives" library for the target technology
- Synthesize netlist from behavioral/RTL model
  - Vendor-provided: ***Xilinx Vivado*** *(previously ISE),* ***Altera Quartus II***
  - ***Leonardo*** *(Levels 1,2,3)* has FPGA & ASIC libraries (ASIC-only version installed at AU)
- Vendor tools for back-end design
  - Map, place, route, configure device, timing analysis, generate timing models
  - **Xilinx** ***Vivado*** (*previously ISE - Integrated Software Environment*)
  - **Altera** ***Quartus II***
- Higher level tools for system design & management
  - *Xilinx Platform Studio :* SoC design, IP management, HW/SW codesign
  - Mentor Graphics *FPGA Advantage*