ASIC Project Cost

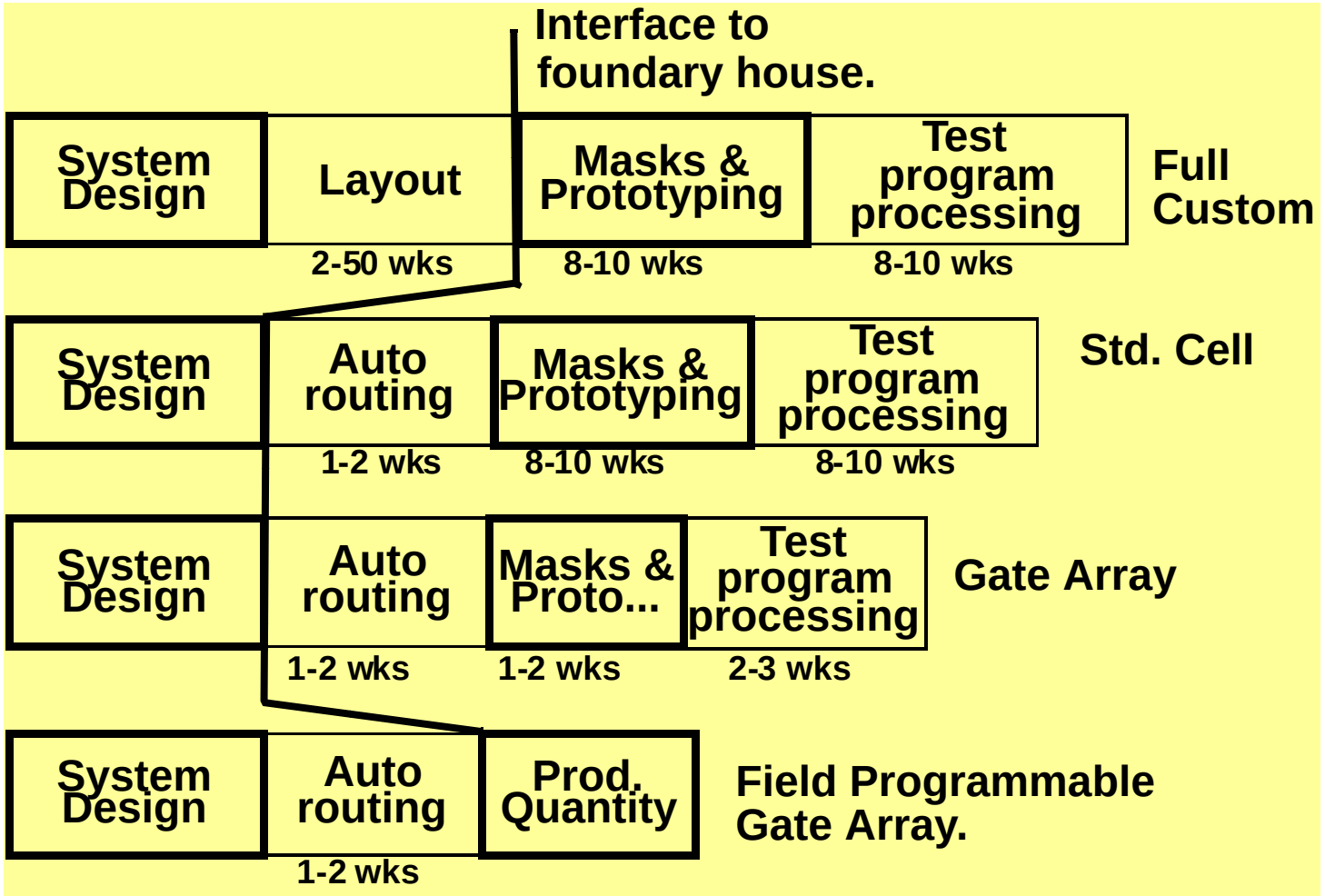
Smith Text – Chapter 1

VLSI Implementations

	Custom	Standard cell	Gate array	FPGA
Density	Highest	Medium	Low	Lowest
Performance	Highest	Medium	Low	Lowest
Design time	Long	Medium	Short	Shortest
Chip Dev cost	High	Medium	Low	Lowest
Testability	Difficult	Less difficult	Easy	Easy
High Volume?	High	Medium	Low	Lowest

Other Considerations?

Comparing Implementation Styles



ASIC Cost

Total Product Cost = NRE + (P x RE)

NRE = fixed, non-recurring engineering cost

RE = variable, recurring cost per part

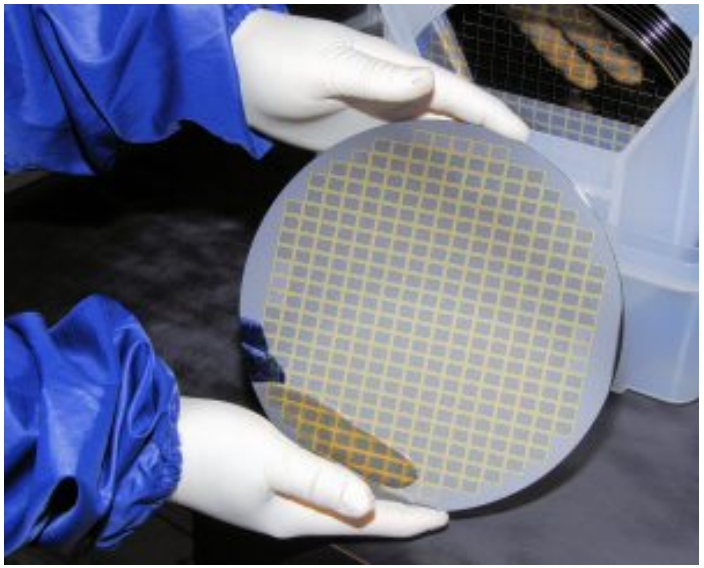
P = #parts produced

ASIC Cost: Fixed (NRE)

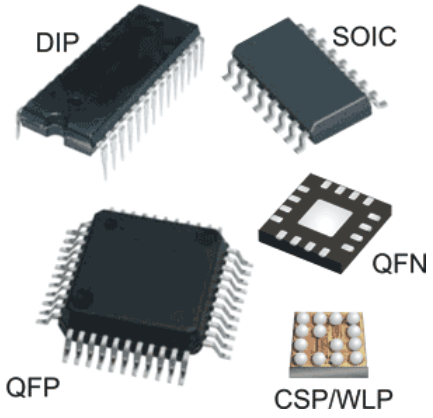
- Fixed Costs
  - EDA tools and training
  - Design cost = f(#gates, designer productivity)
    - Hardware, software, integration
  - Design for test
  - Simulation
  - Test program development
  - ASIC vendor costs (masks, etc.)

ASIC Cost: Variable (RE)

- Variable costs (cost per part)
  - Wafer cost
  - Wafer processing
  - Die size (# die per wafer)
    - Size of design (# gates)
    - Technology (# gates per sq. inch)
    - % utilization of die
  - Production yield = f(defect density,die size)
  - Packaging



http://www.waferpro.com/what-is-a-semiconductor-wafer/



http://electroiq.com/blog/2005/08/materials-and-methods-for-ic-package-assemblies/

ASIC Fixed Costs Example

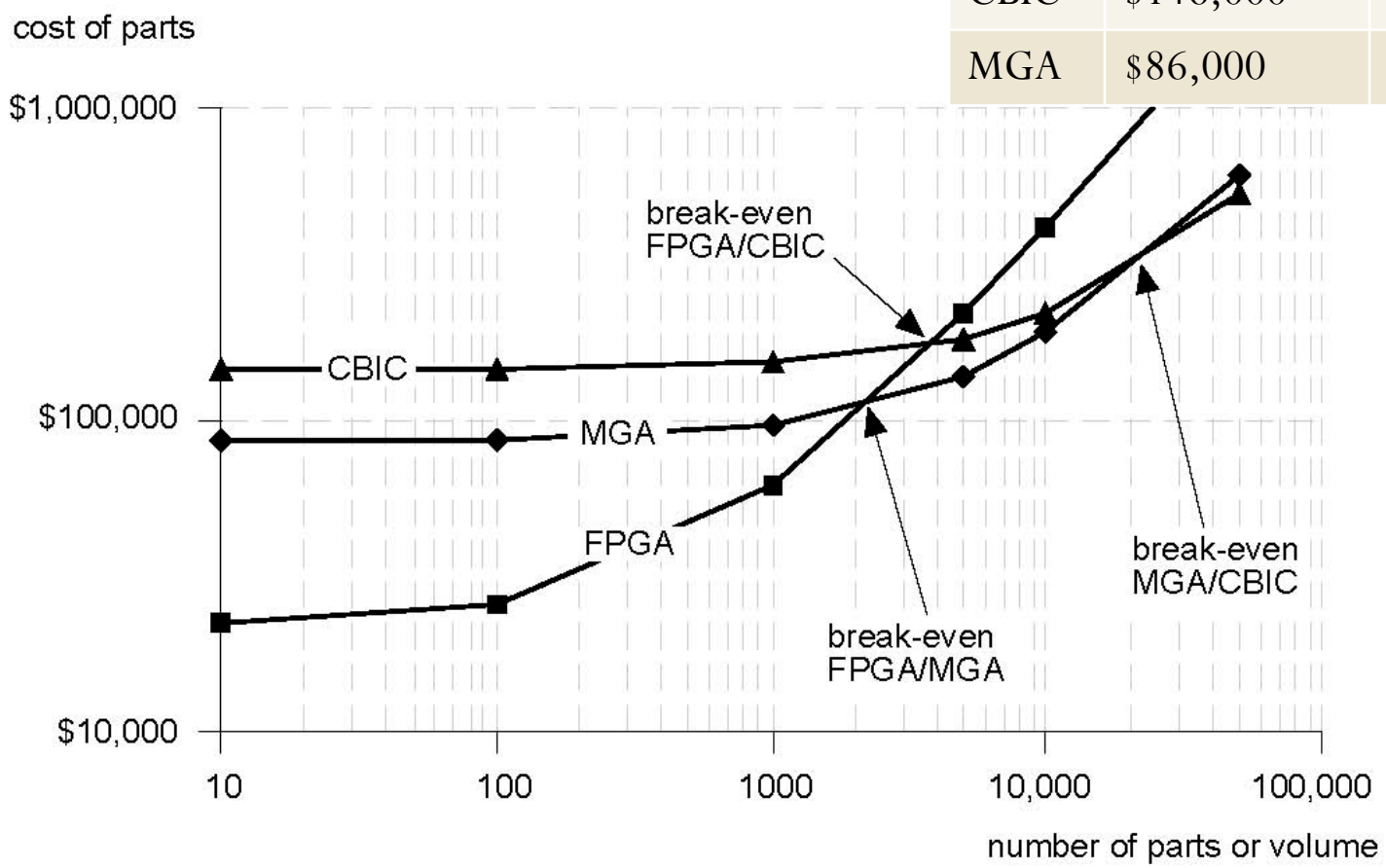
	FPGA		MGA		CBIC	
Training:	$800		$2,000		$2,000	
Days		2		5		5
Cost/day		$400		$400		$400
Hardware	$10,000		$10,000		$10,000	
Software	$1,000		$20,000		$40,000	
Design:	$8,000		$20,000		$20,000	
Size (gates)		10,000		10,000		10,000
Gates/day		500		200		200
Days		20		50		50
Cost/day		$400		$400		$400
Design for test:			$2,000		$2,000	
Days				5		5
Cost/day				$400		$400
NRE:			$30,000		$70,000	
Masks				$10,000		$50,000
				$10,000		$10,000
Test program				$10,000		$10,000
Second source:	$2,000		$2,000		$2,000	
Days		5		5		5
Cost/day		$400		$400		$400
Total fixed costs	$21,800		$86,000		$146,000	

ASIC Variable Costs Example

	FPGA	MGA	CBIC	Units
Wafer size	6	6	6	inches
Wafer cost	1,400	1,300	1,500	$
Design	10,000	10,000	10,000	gates
Density	10,000	20,000	25,000	gates/sq.cm
Utilization	60	85	100	%
Die size	1.67	0.59	0.40	sq.cm
Die/wafer	88	248	365	
Defect density	1.10	0.90	1.00	defects/sq.cm
Yield	65	72	80	%
Die cost	25	7	5	$
Profit margin	60	45	50	%
Price/gate	0.39	0.10	0.08	cents
Part cost	$39	$10	$8	

Break-Even Analysis

	Fixed Cost	Cost/Part
FPGA	$21,800	$39
CBIC	$146,000	$8
MGA	$86,000	$10



ASIC Profit Model

On-time: total sales = $60M
3 months late: total sales = $25M