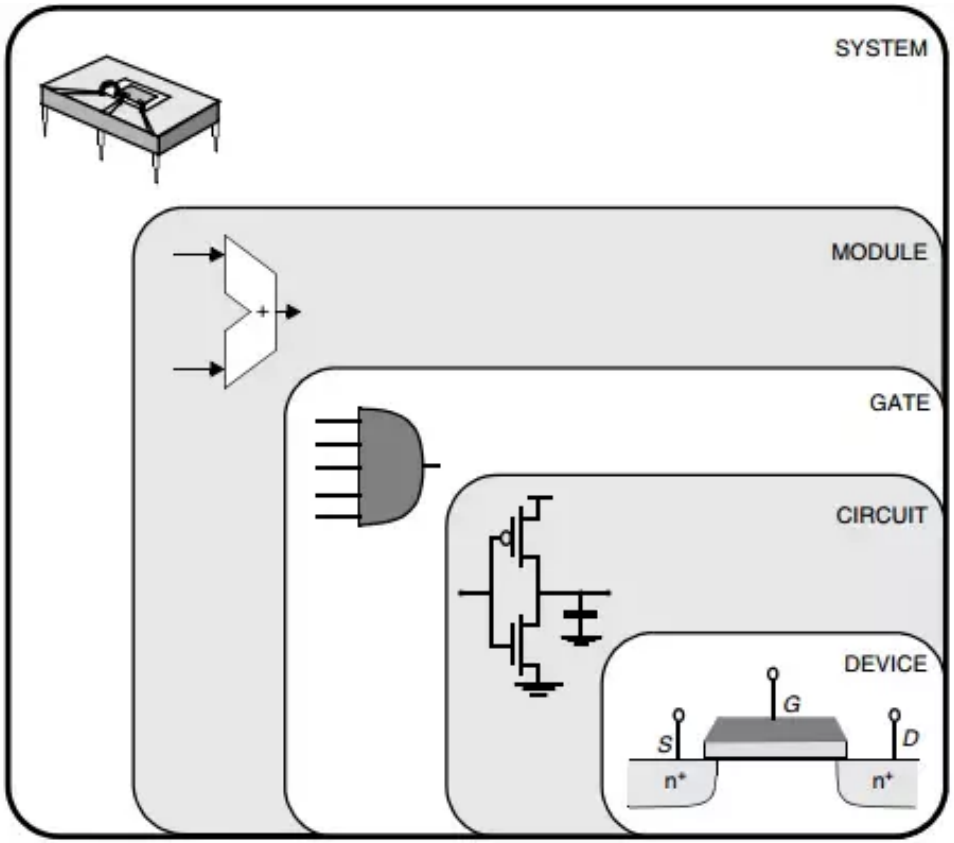
ASIC Technologies

Hierarchical Design and Abstraction

ASIC/SoC Technologies and Implementation

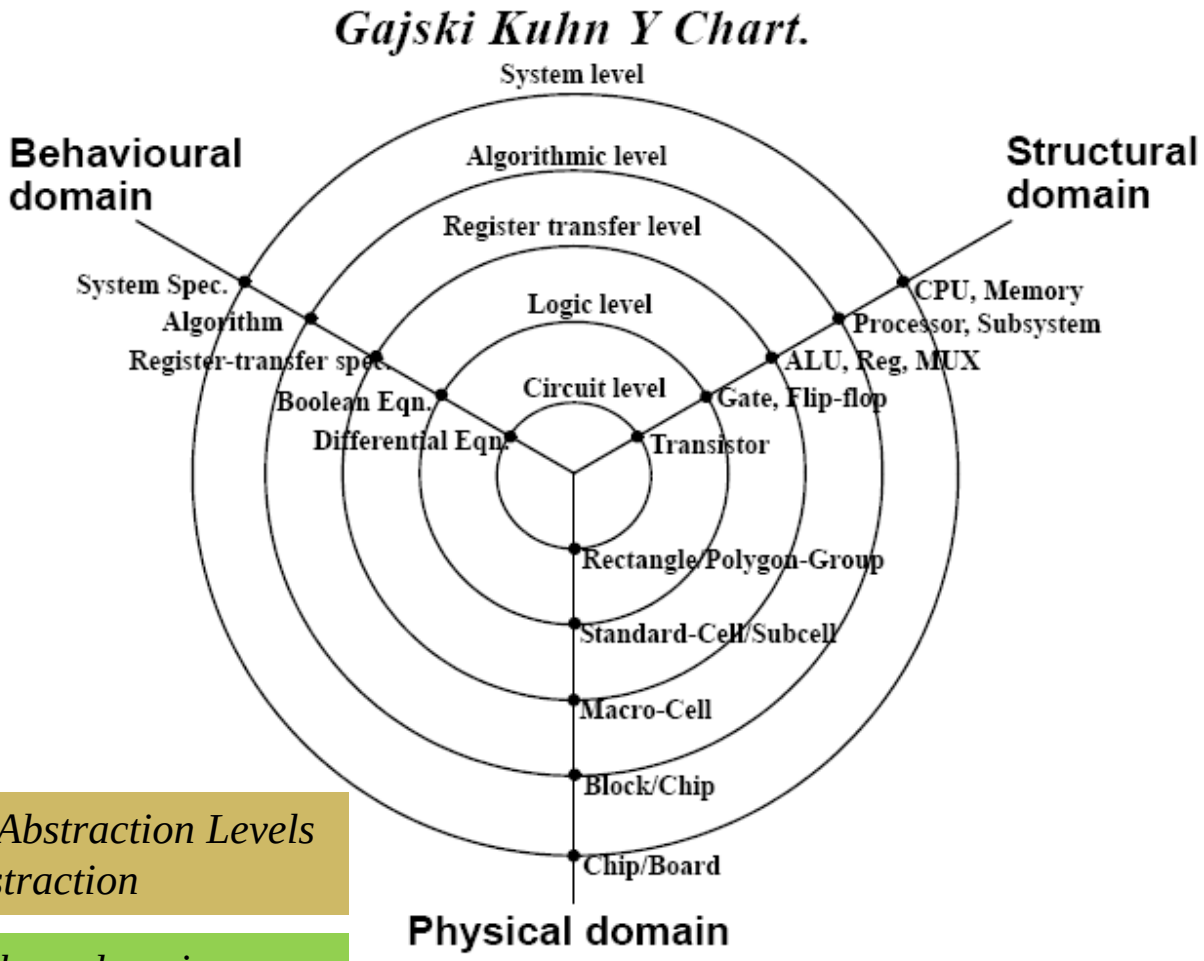
Design abstraction in digital circuits



https://www.quora.com/What-should-be-the-best-way-to-learn-VLSI-design

The taxonomy of VLSI design space

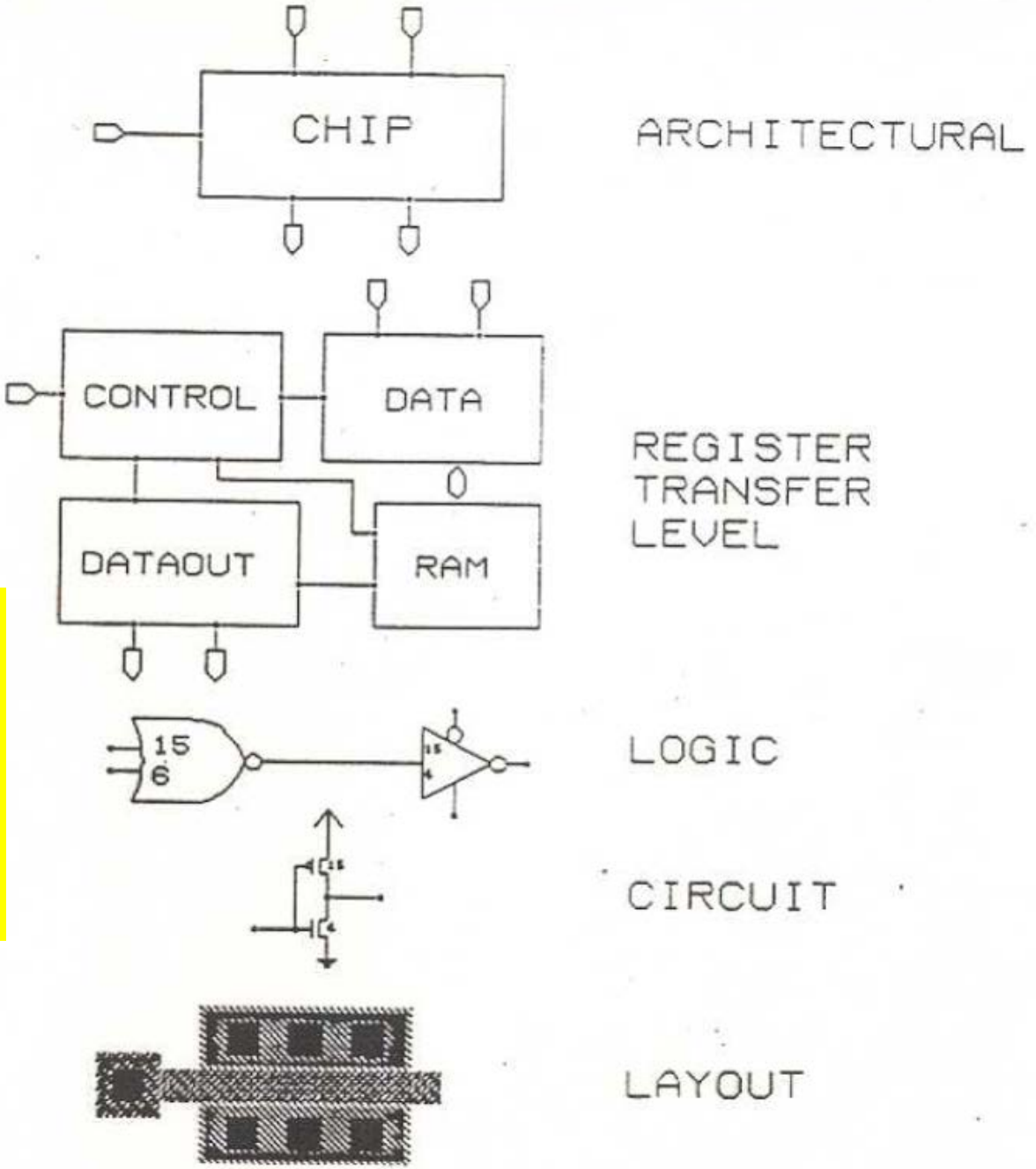
We model and simulate at each level of abstraction and/or mixtures of elements at different abstraction.



Concentric Circles Represent Abstraction Levels
Larger Circles → Greater Abstraction

The three axes represents the three domains

Design Hierarchy/ Abstraction

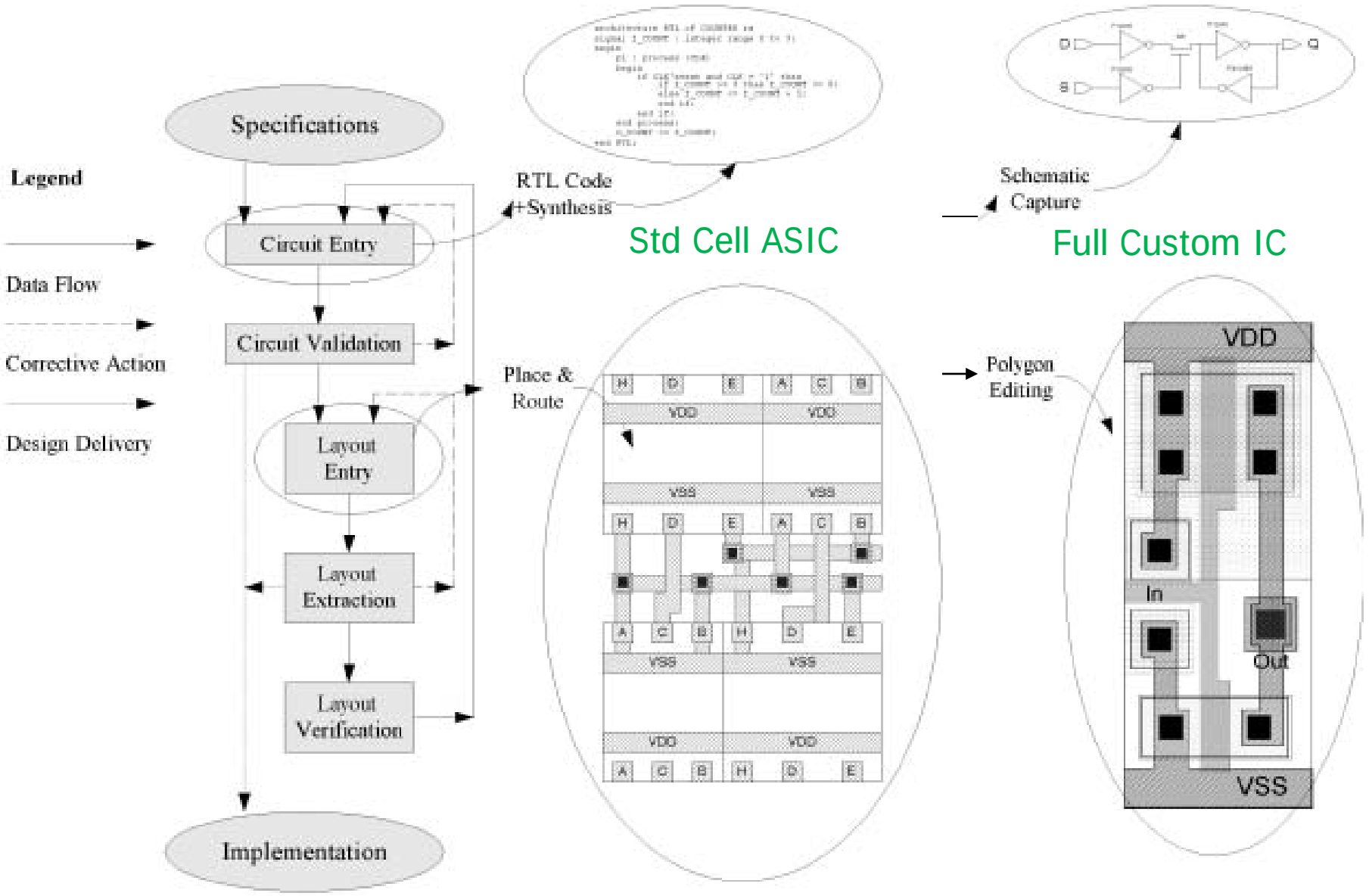


Design abstraction:

- *System (CPUs, I/O, memory)*
- *Behavior/algorithm (HDL)*
- *Register transfer*
- *Logic Gate (net list)*
- *Circuit (transistor)*
- *Mask/layout (physical design)*

ASIC Design Flow

Source: CMOS IC Layout, Dan Clein

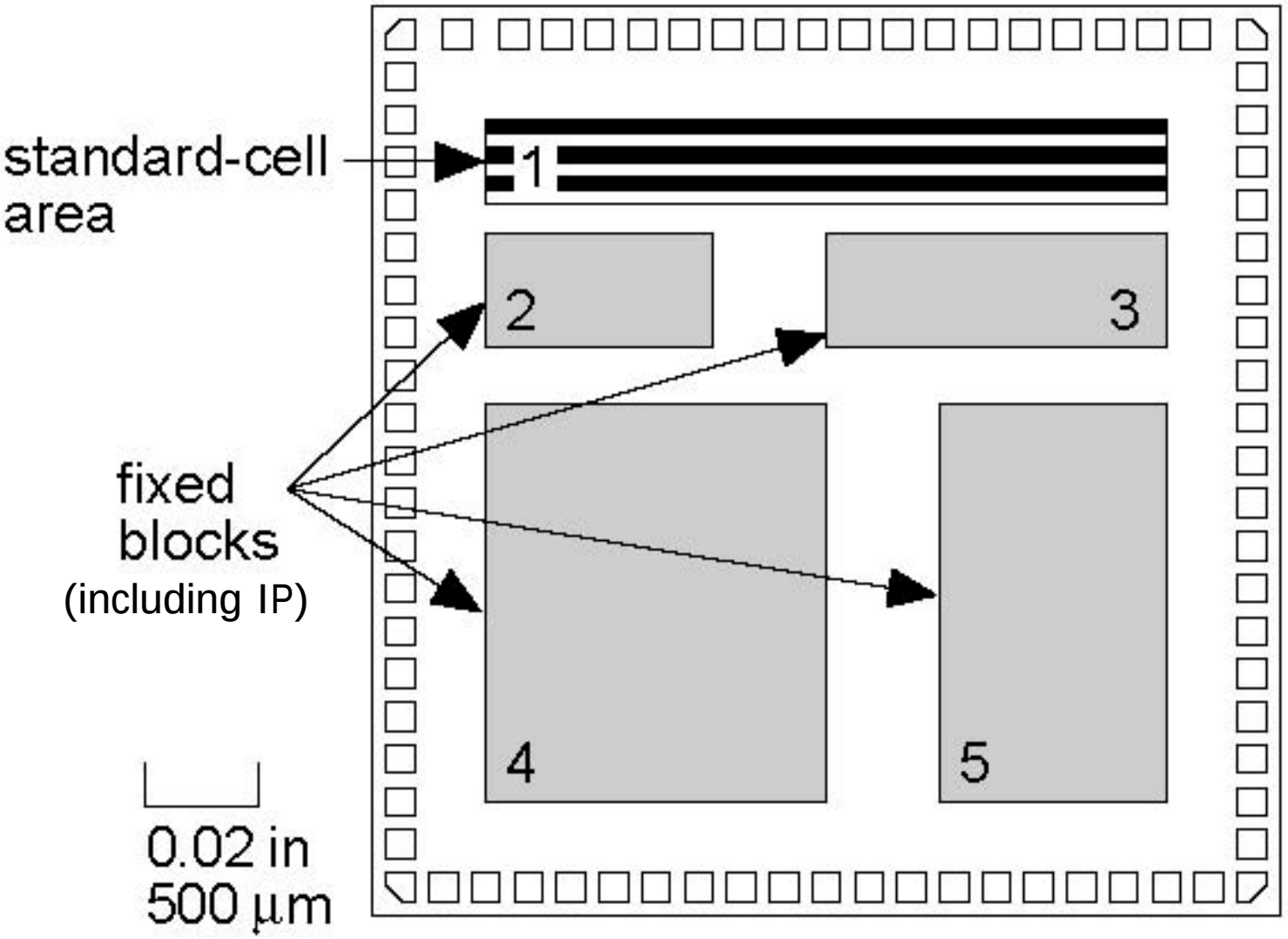


ASIC/SoC Technologies

- Full custom IC design
- ***Cell-based IC (our course)***
- Mask-programmable gate array
- Platform/structured ASIC
- Field-programmable gate array (FPGA)
- Complex programmable logic device (CPLD)
- Software-programmable device
- Commercial off the shelf (COTS) device

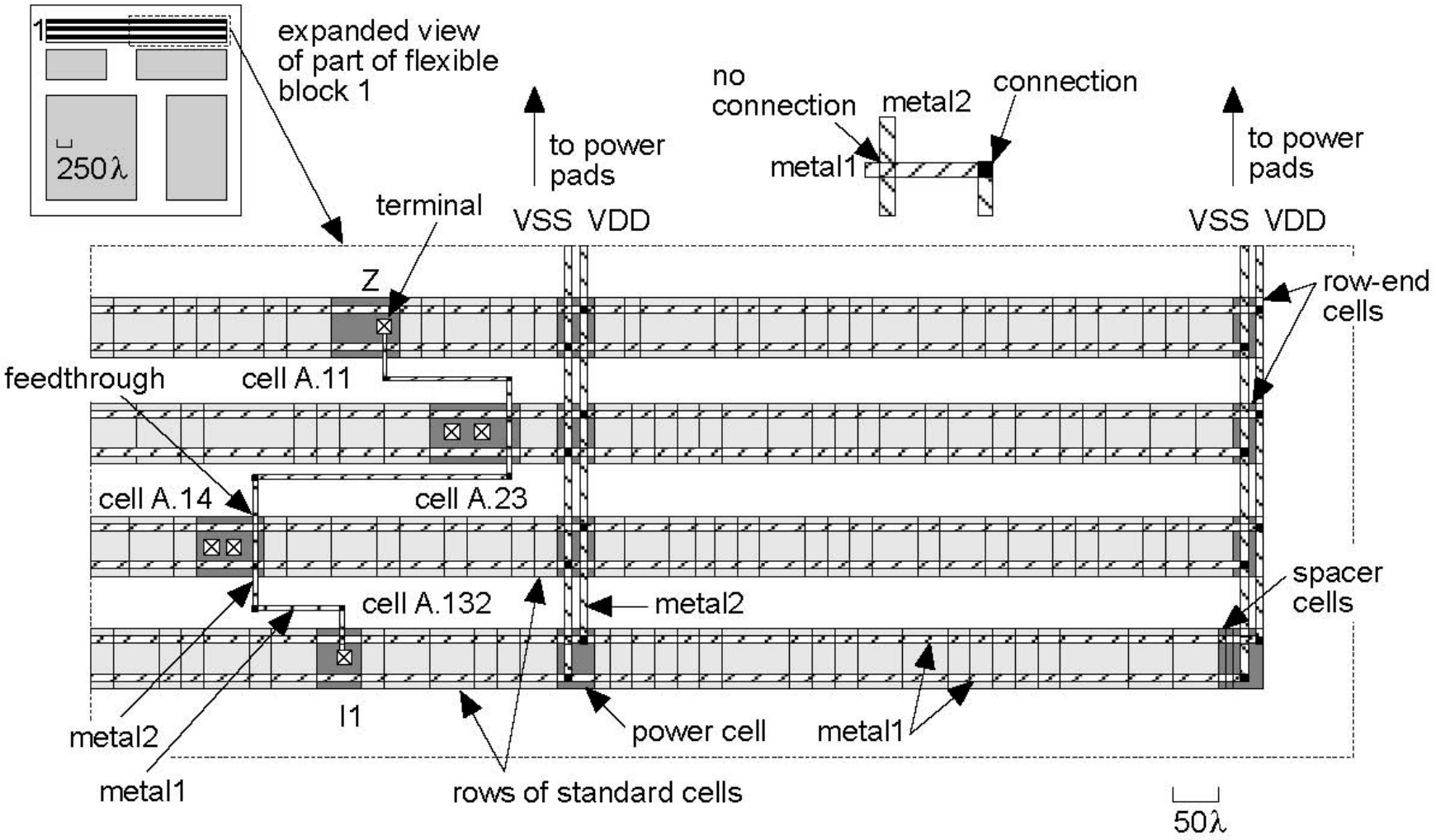
Cell-Based IC

8-week lead time
(must fabricate all layers)

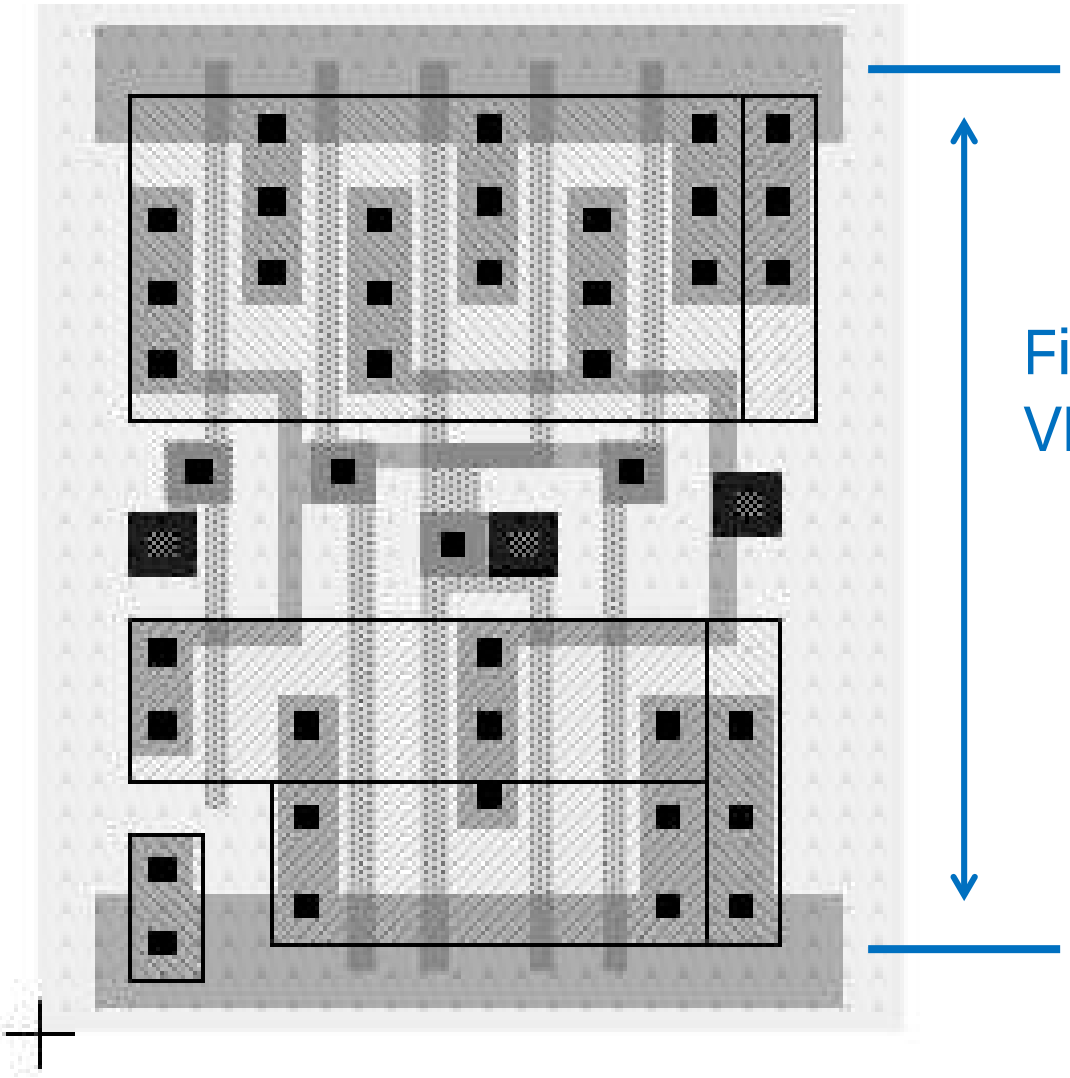


Cell-Based Block

- Build design with predesigned & characterized "cells"
- Customize placement and interconnect (cells placed into fixed-height rows)



Standard Cell

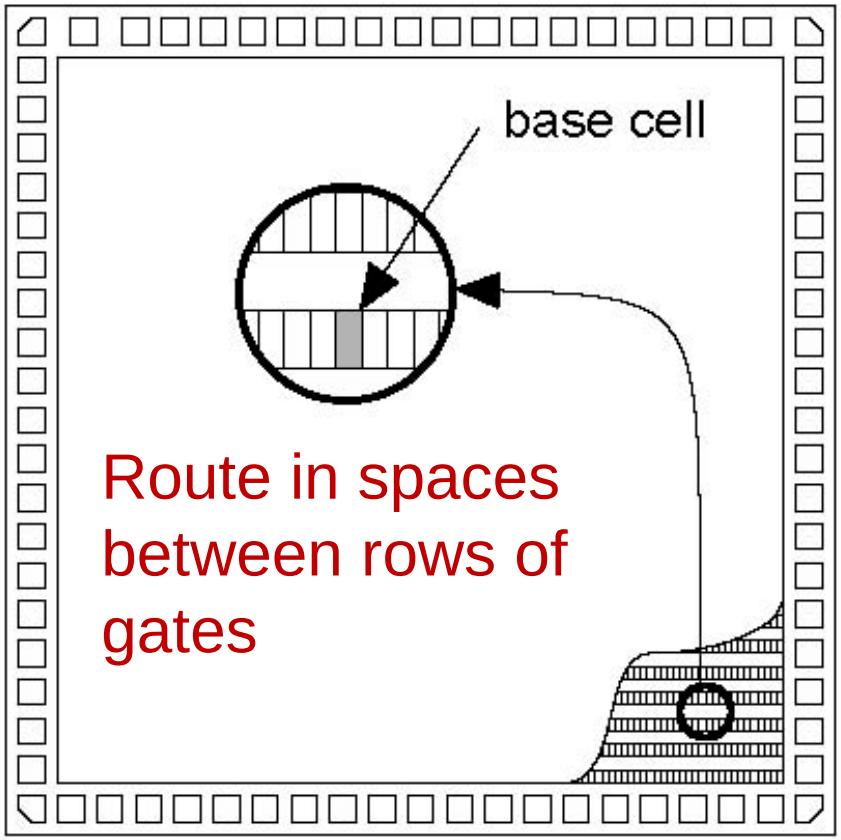


Masked Gate Array

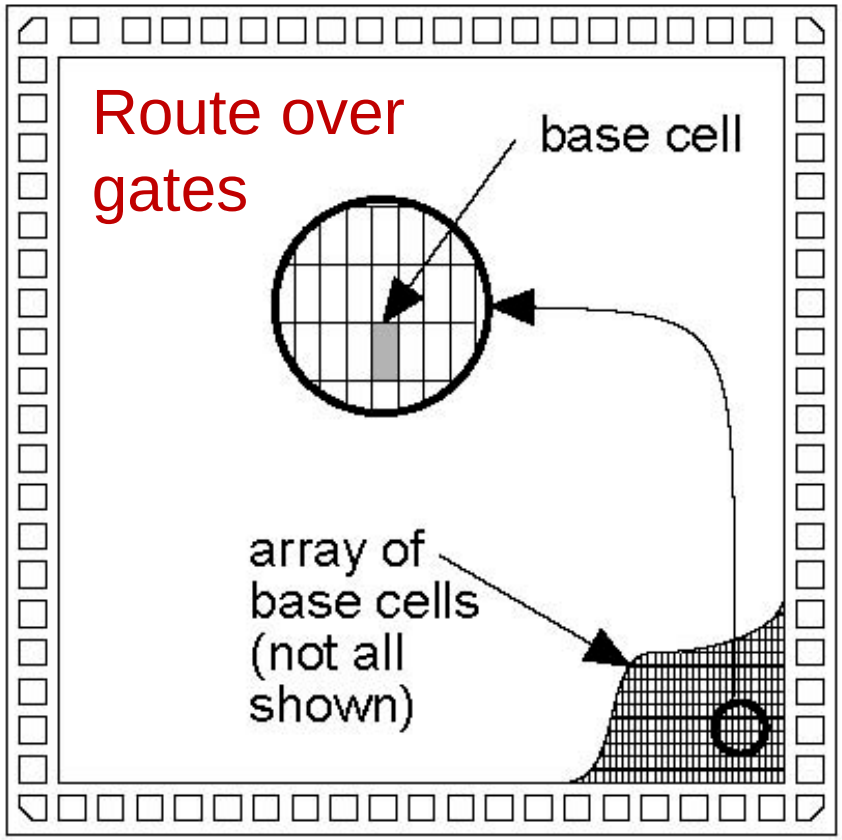
- Map design onto gates in the array
  - Gates designed, characterized, pre-fabricated
  - Customize placement and interconnect
  - Fabricate only top-most interconnects
- Cell library may contain "macros"/IP
  - Patterns of gates/functions
  - Soft vs. hard macros
- Lead time = few days to 2 weeks

Gate array structures

Channeled gate array

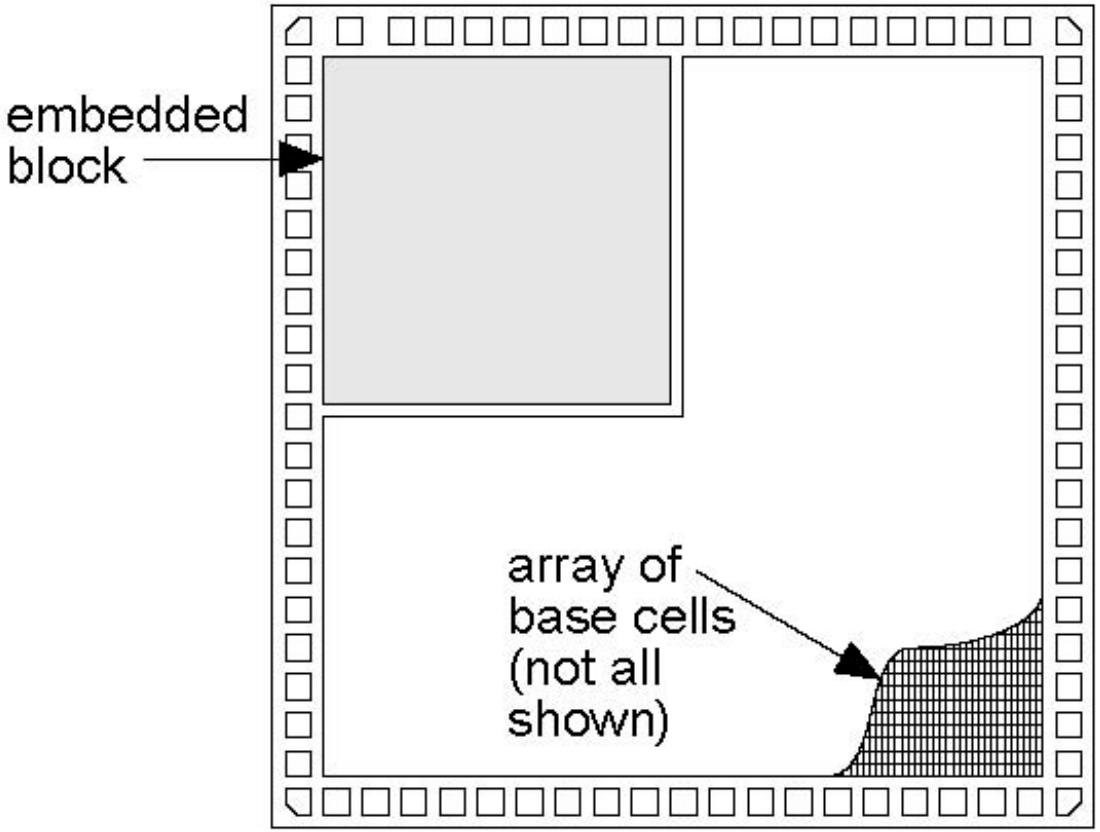


Sea of gates (channel-less)



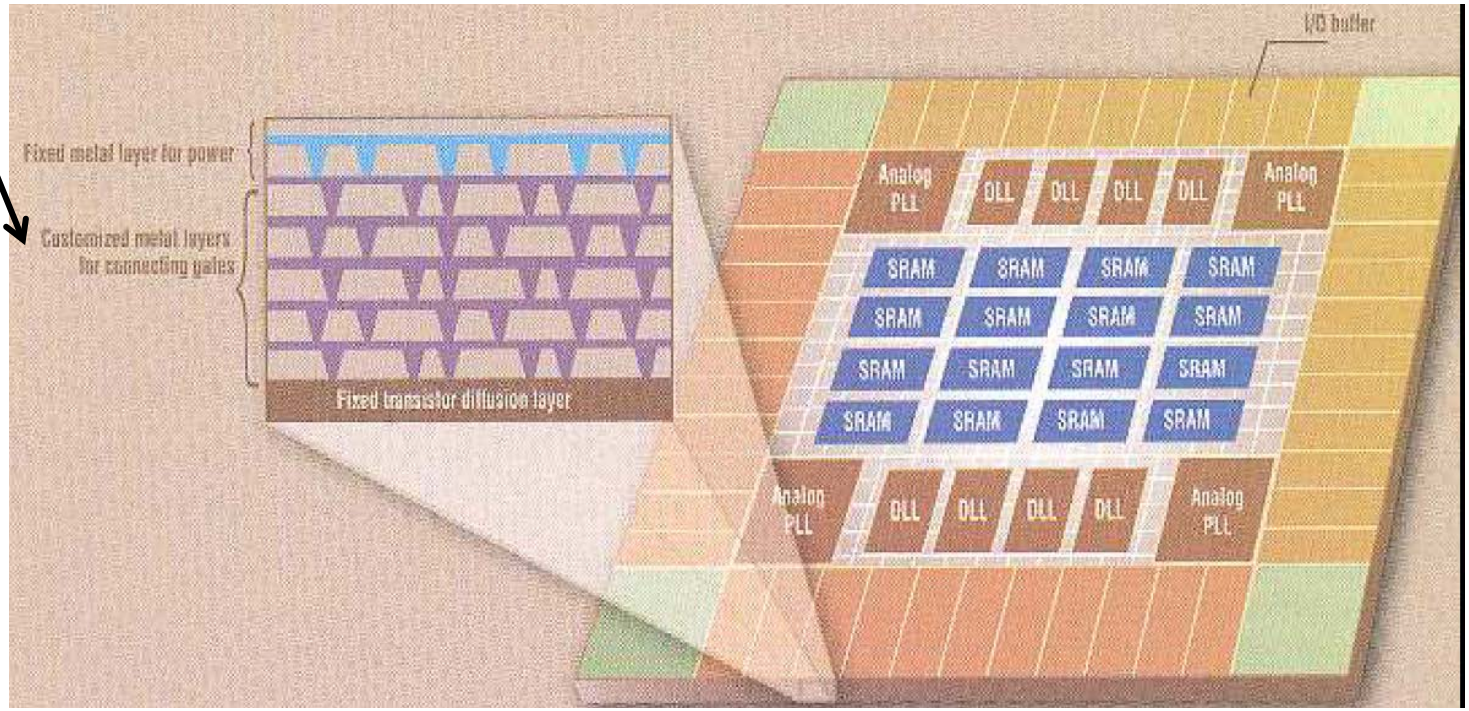
Structured/Embedded Gate Array

- Market position between gate array and cell-based ASIC
- Embedded blocks (CPU, memory) + programmable gate arrays
- Fab creates masks for top metal layers only



Structured ASIC Approach
(NEC Electronics America)

Metal layers customized for the design



(*Electronic Design* Supplement – July 20, 2006)

Faraday TEMPLATE platform ASIC

www.faraday-tech.com

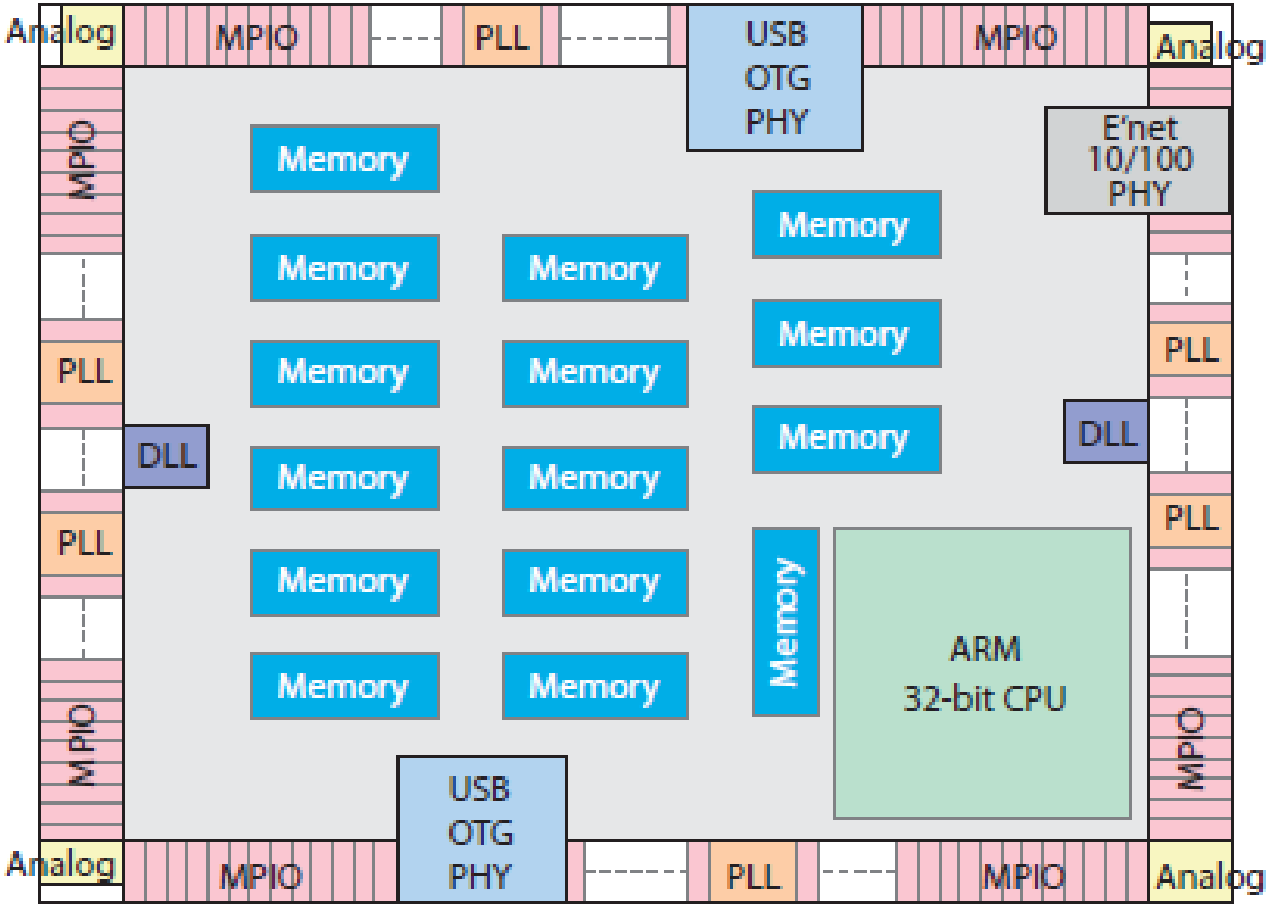
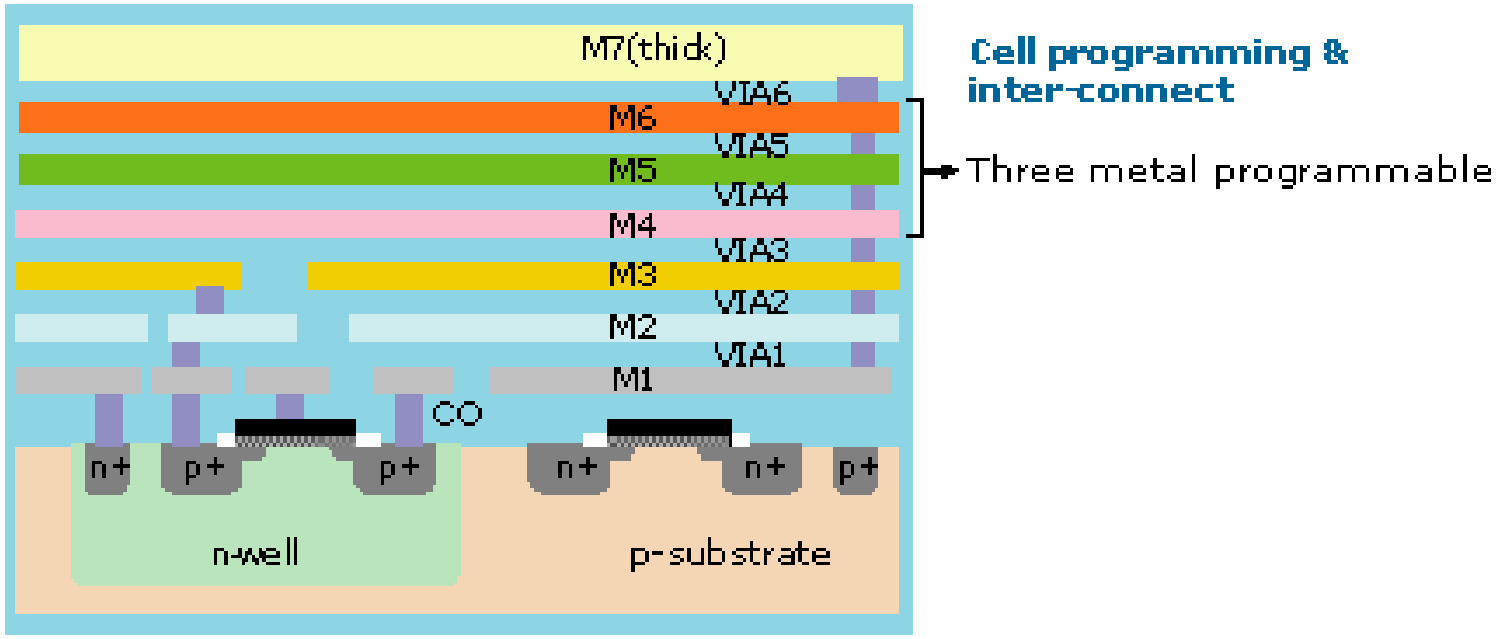


Figure 4: A TEMPLATE master-slice

Faraday - Profile of 1P7M Structured ASIC (www.faraday-tech.com)



Programming layers for 1P7M Process

Faraday platform ASIC examples

www.faraday-tech.com

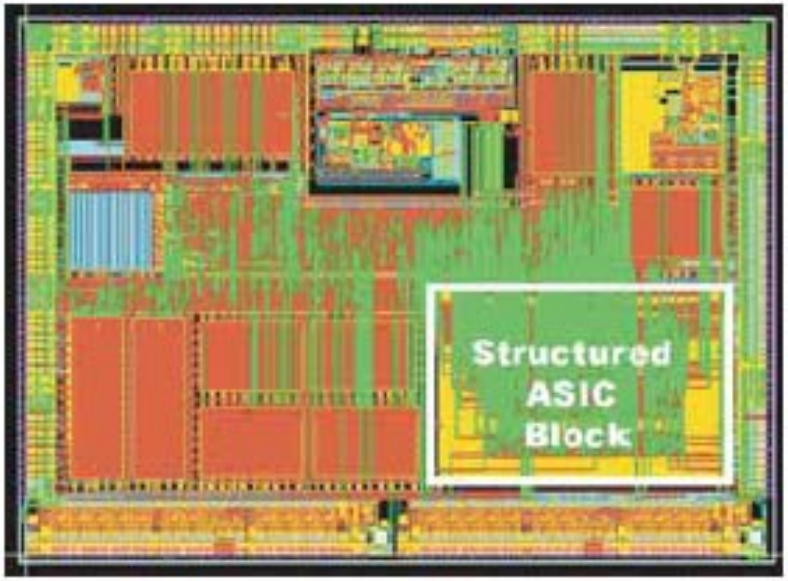


Figure 5: (a) A DisplayComposer Chip

(b) A NetComposer Chip

Faraday TEMPLATE structured ASICs

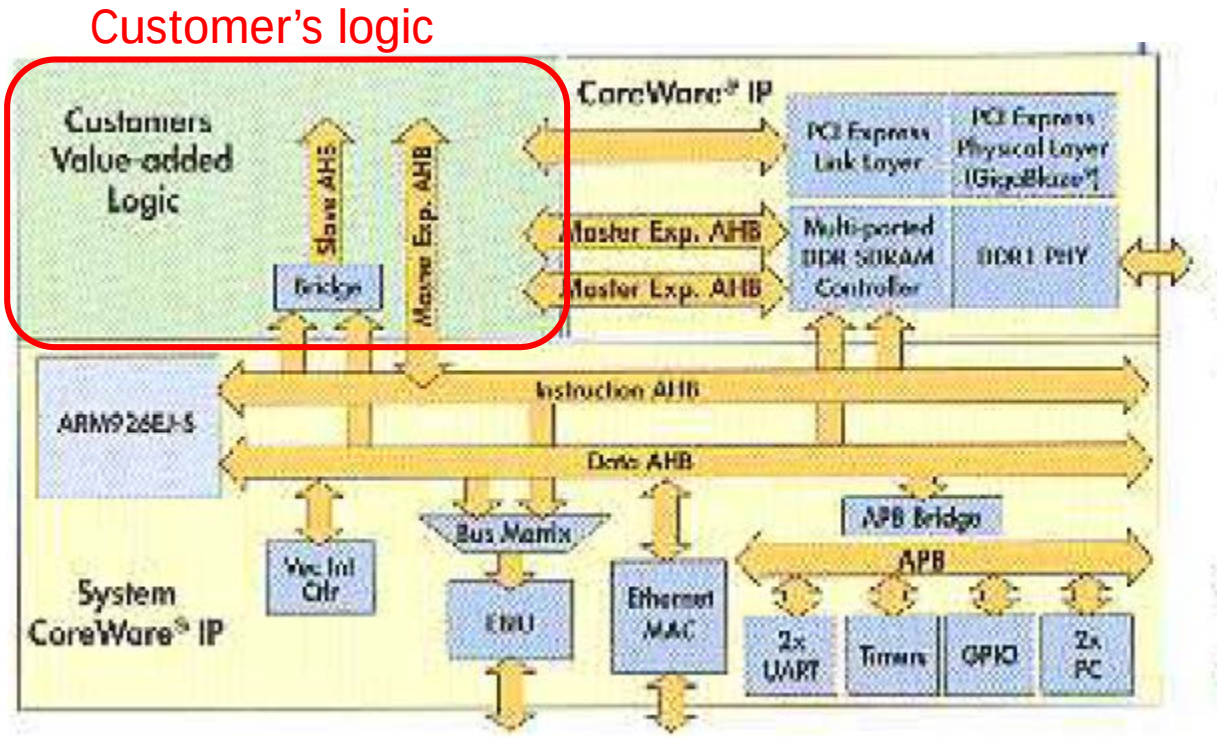
www.faraday-tech.com

Masterslice	FT2000	FT3000	FT4000	FT5000	FT6000	FT7000	FT8000
Usable ASIC Gates	256K	1024K	1024K	2236K	2048K	4352K	6400K
Total RAM bits	512K	1024K	768K	1536K	1664K	2560K	4224K
Number of PLL	4	4	4	4	6	8	12
Number of DLL	-	2	2	2	2	4	4
32bit CPU	-	-	-	-	1	-	-
USB OTG	-	-	1	1	2	2	2
E'net 10/100	-	-	-	-	1	-	1
OSC/POR/VDT	*	*	*	-	*	-	-
System clock Speed	500MHz+	500MHz+	500MHz+	500MHz+	500MHz+	500MHz+	500MHz+
Max. IO available	208	292	292	388	388	484	580
Package							
QFP128	*	*	*				
QFP208	*	*	*	*	*	*	
BGA256		*	*	*	*	*	*
BGA292		*	*	*	*	*	*
BGA352				*	*	*	*
BGA388				*	*	*	*
BGA484							*
BGA580							

Table 2: Template Family

LSI Logic "CoreWare" IP Solution (www.RapidChip.com)

Designing with pre-integrated systems of IP
(*Electronic Design* Supplement – Sep. 6, 2004)



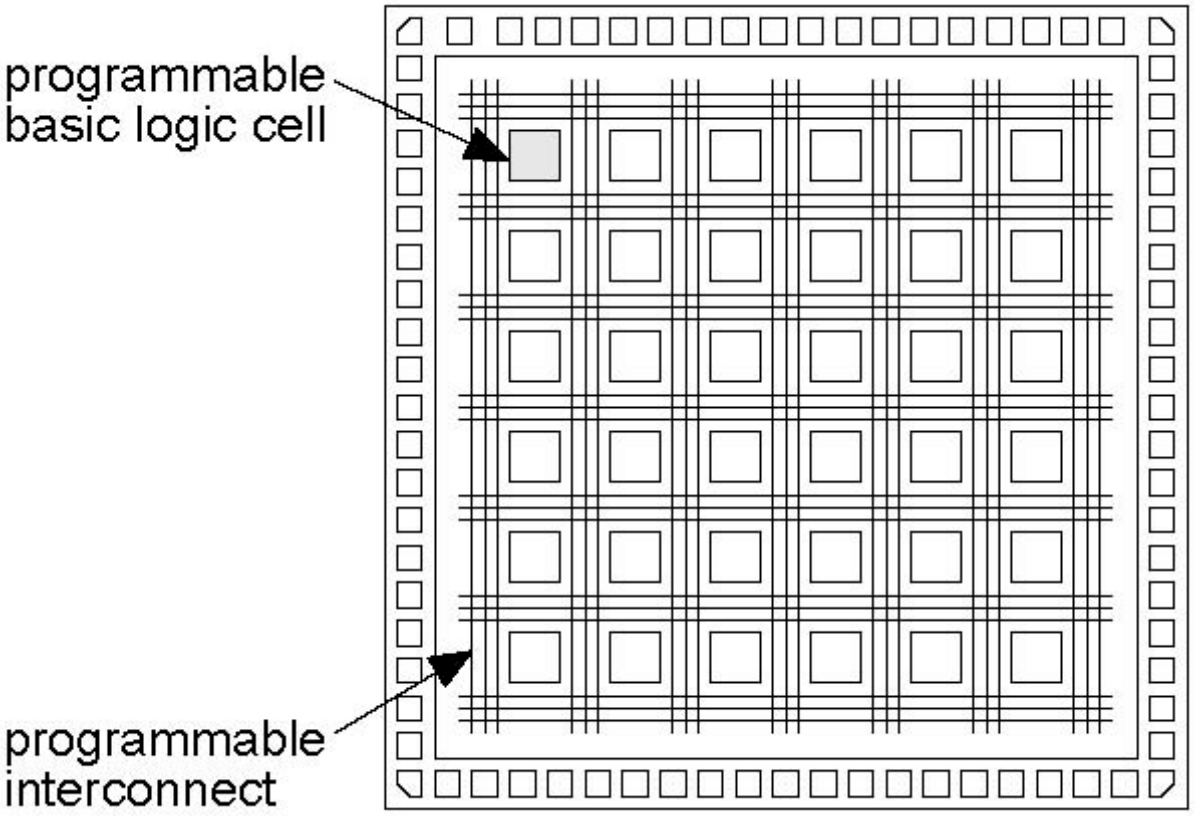
Programmable Logic Devices

- **FPGA**: array of gates & interconnects
- **CPLD**: based on AND/OR array

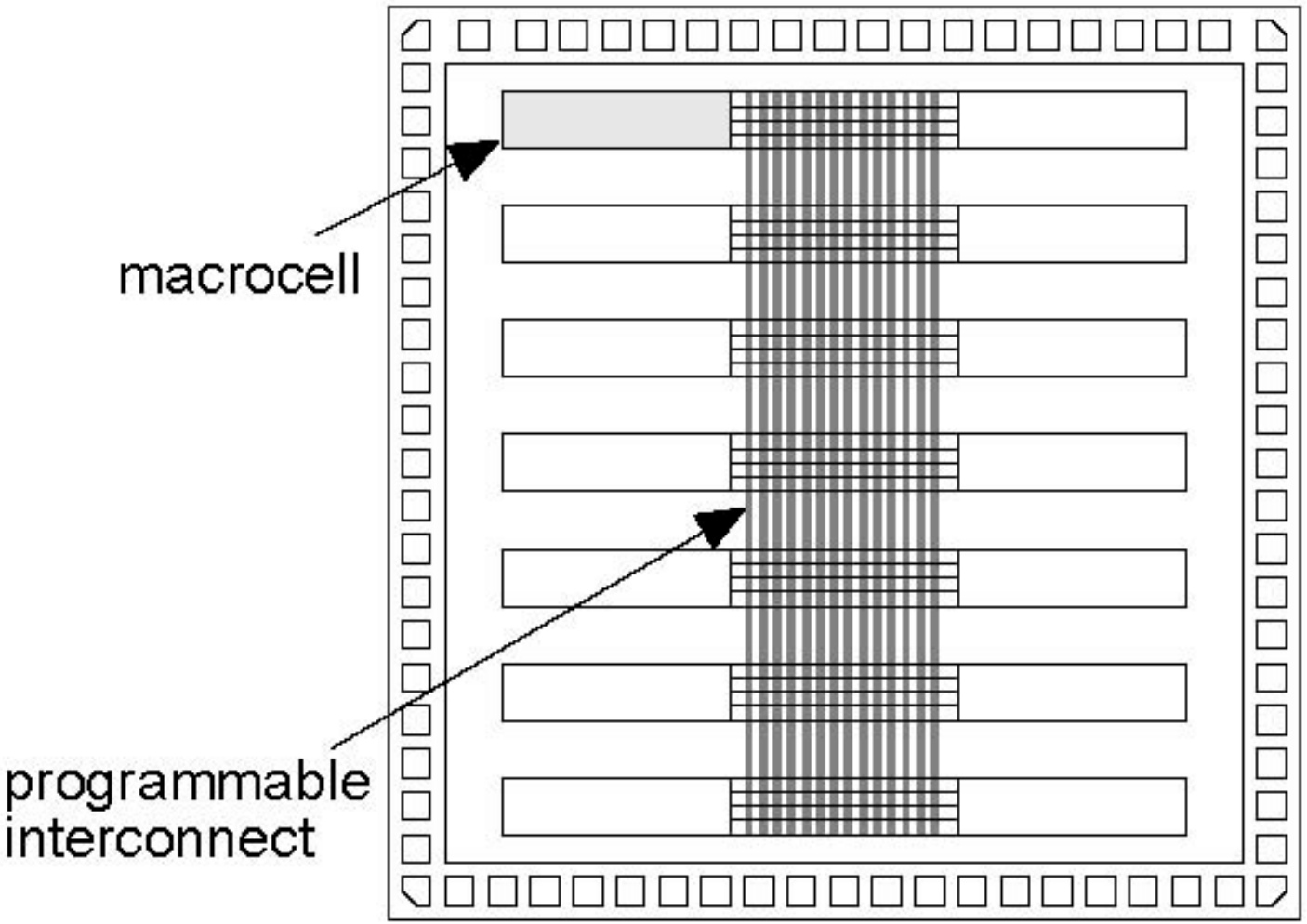
- No custom circuitry to be fabricated
- **User** programs logic/interconnects
- ROM-EPROM-EEROM-RAM based
- Design turnaround time in hours

Field-Programmable Gate Array

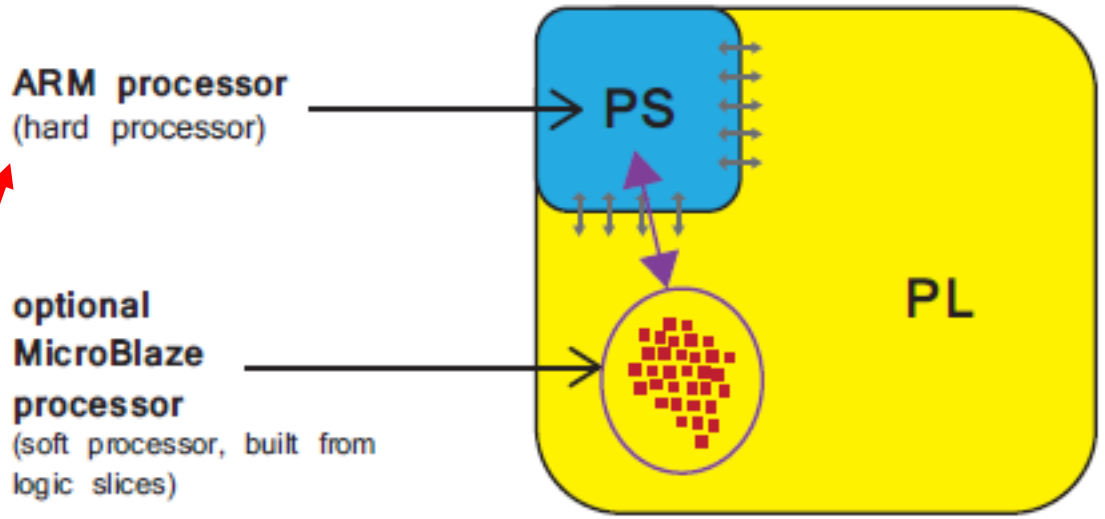
Program logic cells, I/O pads & interconnects



Programmable Logic Device Die



Xilinx Zynq SoC devices



PL = Programmable Logic

Zynq-7000 SoC: Dual-core ARM Cortex-A9 MPCore (up to 1GHz)

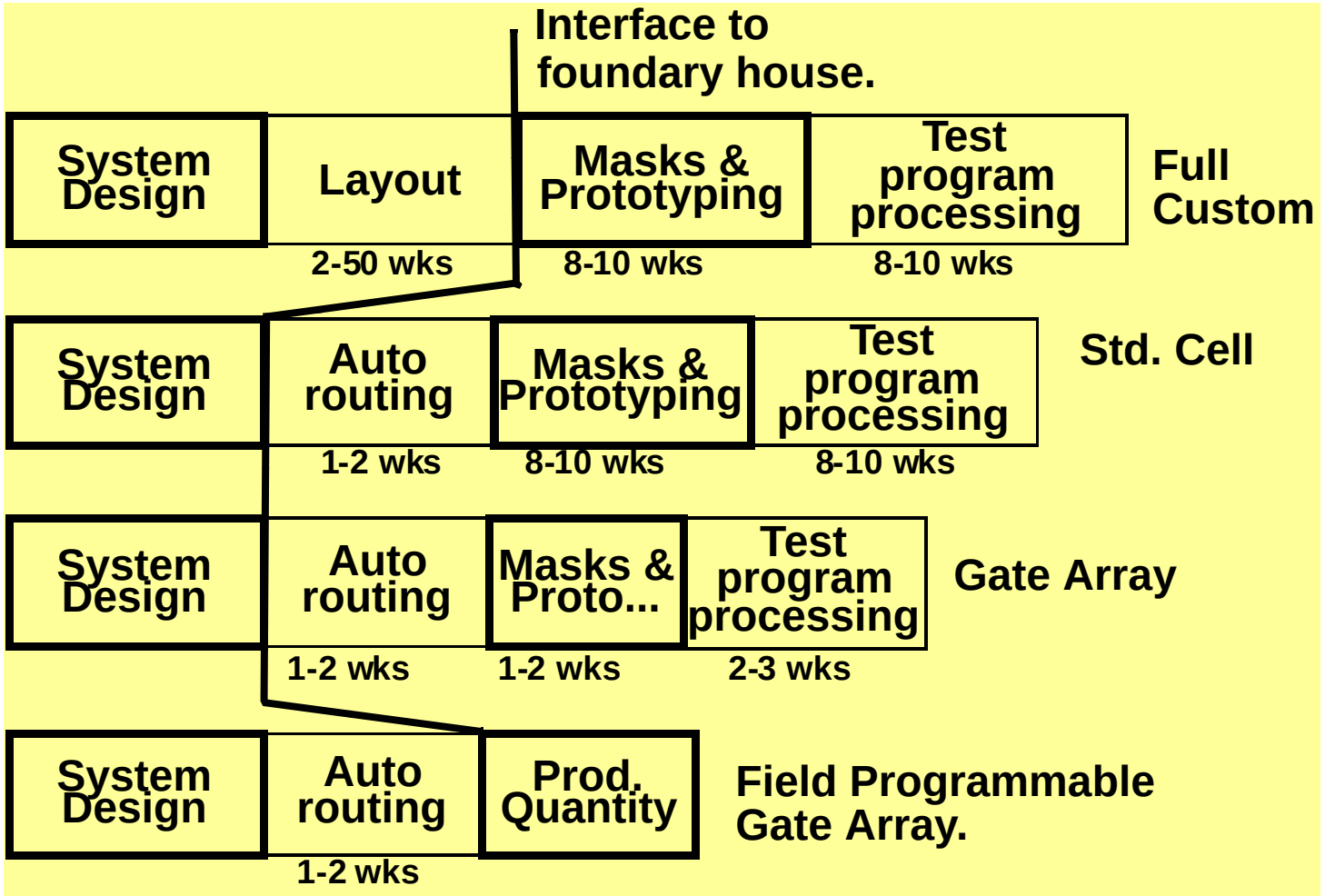
Zynq UltraScale+ MPSoC:

- Quad-core ARM Cortex-A53 MP (up to 1.5 GHz)
- Dual-core ARM Cortex-R5 MPCore (up to 600MHz)
- GPY ARM Mali-400 MP2 (up to 667MHz)

FPGA Evolution

FPGA	Transistor count	Date	Manufacturer
Virtex	~70,000,000	1997	Xilinx
Virtex-E	~200,000,000	1998	Xilinx
Virtex-II	~350,000,000	2000	Xilinx
Virtex-II PRO	~430,000,000	2002	Xilinx
Virtex-4	1,000,000,000	2004	Xilinx
Virtex-5	1,100,000,000	2006	Xilinx
Stratix IV	2,500,000,000	2008	Altera
Virtex-7	6,800,000,000	2012	Xilinx
Virtex-Ultrascale	21,000,000,000	2015	Xilinx

Comparing Implementation Styles



VLSI Implementations

	Custom	Standard cell	Gate array	FPGA
Density	Highest	Medium	Low	Lowest
Performance	Highest	Medium	Low	Lowest
Design time	Long	Medium	Short	Shortest
Chip Dev cost	High	Medium	Low	Lowest
Testability	Difficult	Less difficult	Easy	Easy
High Volume?	High	Medium	Low	Lowest