#### Introduction to ASIC Design

Victor P. Nelson

#### ELEC 5250/6250 – CAD of Digital ICs

#### **Design & implementation of ASICs**



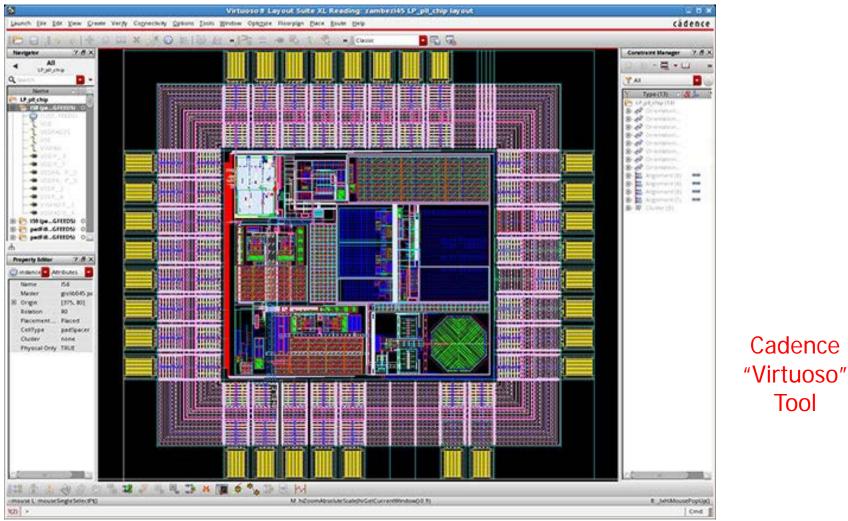




#### Oops – Not these!

#### **Application-Specific Integrated Circuit (ASIC)**

- Developed for a specific application
- Not "general purpose"



Cadence

Tool

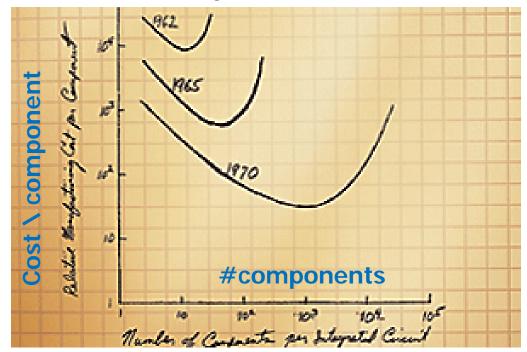
## Progress of State of the Art

Year	Integration Level	# devices	Function	
1938-46	Electromagnetic relays	1		
1943-54	Vacuum tubes	1		
1947-50	Transistor invented	1		
1950-61	Discrete components	1		
1961-66	SSI	10′s	Flip-flop	
1966-71	MSI	100's	Counter	
1971-80	LSI	1,000′s	uP	
1980-85	VLSI	100,000's	uC	
1985-90	ULSI*	1M	uC*	
1990	GSI**	10M	SoC	
2011	Intel Ten-Core <u>Xeon</u>	2.6G	CPU	
2017	Nvidia GV100 Volta	21.1G	GPU	

# Moore's Law (Gordon Moore – 1965)

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year

- ... over the short term this rate can be expected to continue, if not to increase.
- ... over the longer term, the rate of increase is a bit more uncertain
- ... no reason to believe it will not remain nearly constant for at least 10 years
- ... by 1975, #components per integrated circuit for minimum cost will be 65,000
- I believe that such a large circuit can be built on a single wafer."



Moore's original graph

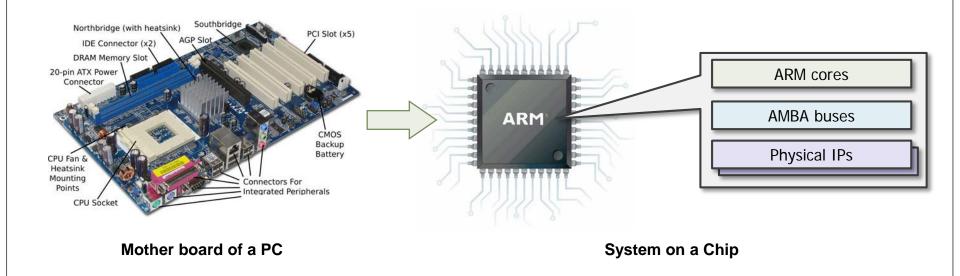
#### Moore's Law Updated 40 Years of Microprocessor Trend Data 10<sup>7</sup> Transistors (thousands) 10<sup>6</sup> Single-Thread 10<sup>5</sup> Performance $(SpecINT \times 10^3)$ $10^{4}$ Frequency (MHz) 10<sup>3</sup> **Typical Power** 10<sup>2</sup> (Watts) Number of $10^{1}$ Logical Cores $10^{0}$ 1970 1980 1990 2000 2010 2020

Year

Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten New plot and data collected for 2010-2015 by K. Rupp

## System-on-Chip (SoC)

- An ASIC that packages basic computing components into a single chip.
- A SoC has most of the components to power a computer.



## Advantages of SoC

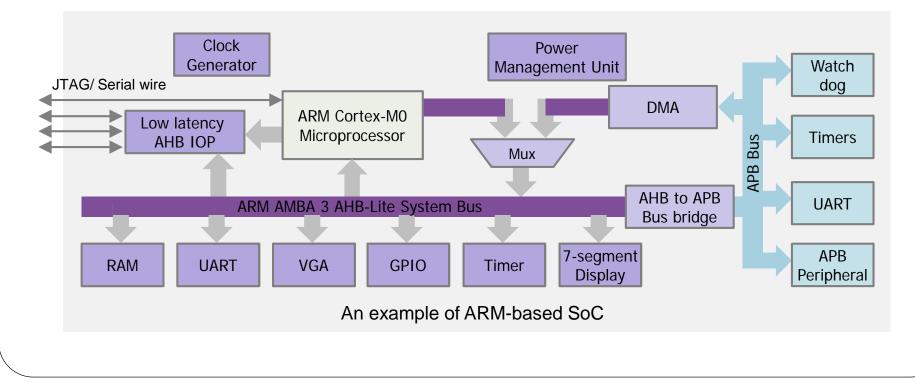
- Higher performance benefiting from:
  - Less propagation delay since internal wires are shorter;
  - Less gate delay as internal transistors have lower electrical impedance;
- Power efficiency benefiting from:
  - Lower voltage required (typically < 2.0 volts) compared with external chip voltage (typically >3.0 volts);
  - Less capacitance;
- Lighter footprint:
  - Device size and weight is reduced;
- Higher reliability:
  - All encapsulated in a single chip package, less interference from the external world;
- Low cost:
  - Cost per unit is reduced since a single chip design can be fabricated in a large volumes.

#### Limitations of SoC

- Less flexibility
  - Unlike a PC or a laptop, which allows you to upgrade a single component, such as RAM or graphic card, a SoC cannot be easily upgraded after manufacture;
- Application Specific
  - Most SoCs are specified to particular applications thus they are not easily adapted to other applications.
- Complexity
  - A SoC design usually requires advanced skills compared with board-level development.

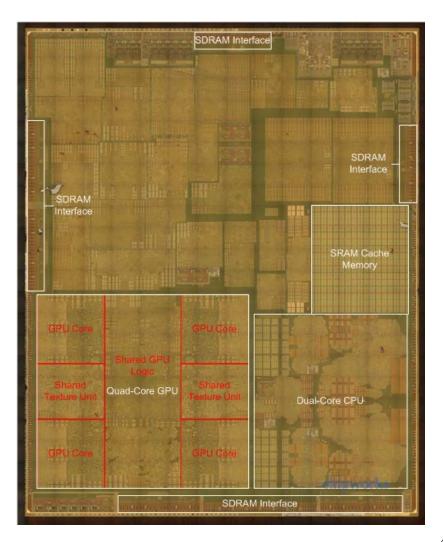
## **ARM-based SoC**

- An basic ARM-based SoC usually consists of
  - An ARM processor, such as Cortex-M0;
  - Advanced Microcontroller Bus Architecture (AMBA), e.g. AMBA3 or AMBA4;
  - Physical IPs (or peripherals) from ARM or third parties;
  - Additionally, some SoCs may have a more advanced architecture, such as multi-bus system with bus bridge, DMA engine, clock and power management, etc...



## Apple "A8" SoC (System on Chip)

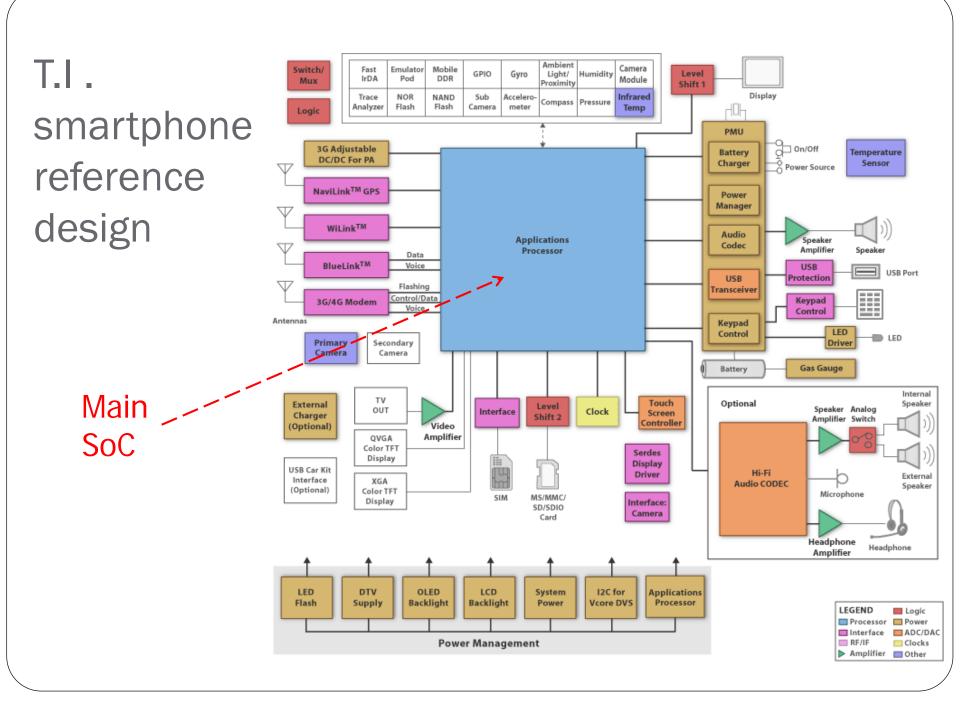
- Used in *iPhone6* & *iPhone6* Plus
- Manufactured by TSMC
  - 20nm, 89mm<sup>2</sup>, 2B transistors
- Elements (unofficial):
  - 2 x ARM Cyclone ARMv8 64-bit cores running at 1.4GHz
  - IMG PowerVR 4-core GX6450 GPU
  - L1/L2/L3 SRAM caches
- Other devices
  - 1 GB LPDDR3 SDRAM
  - 16 to 128GB flash
  - Qualcomm MDM9625M LTE modem
  - M8 motion coprocessor (ARM Cortex M3 uC)
  - iSight camera
  - Near field communications chip (for Apple Pay)
  - User interface and sensors, accelerometers, gyro
  - Wi-Fi and Bluetooth



#### SoC Example: Apple SoC Families

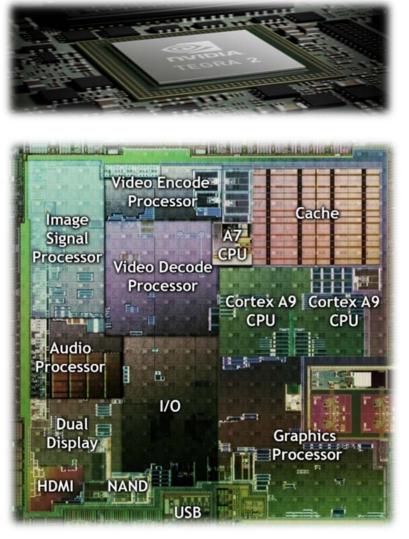
SoC	Model No.	СРИ	CPU ISA	Technology	Die size	Date	Devices
N/A	APL0098	ARM11	ARMv6	90 nm	N/A	6/2007	iPhone iPod Touch (1st gen.)
A4	APL0398	ARM Cortex-A8	ARMv7	45 nm	53.29 mm <sup>2</sup>	3/2010	iPad, iPhone 4, Apple TV (2nd gen.)
A5	APL0498	ARM Cortex-A9	ARMv7	45 nm	122.6 mm <sup>2</sup>	3/2011	iPad 2, iPhone 4S
	APL2498	ARM Cortex-A9	ARMv7	32 nm	71.1 mm <sup>2</sup>	3/2012	Apple TV (3rd gen.)
	APL7498	ARM Cortex-A9	ARMv7	32 nm	$37.8 \text{ mm}^2$	3/2013	AppleTV 3
A5X	APL5498	ARM Cortex-A9	ARMv7	45 nm	$162.94 \text{ mm}^2$	3/2012	iPad (3rd gen.)
A6	APL0598	Swift	ARMv7s	32 nm	96.71 mm <sup>2</sup>	9/2012	iPhone 5
A6X	APL5598	Swift	ARMv7s	32 nm	$123 \text{ mm}^2$	10/2012	iPad (4th gen)
A7	APL0698	Cyclone	ARMv8-A (64-bit)	28 nm	102 mm <sup>2</sup>	9/2013	iPhone 5S, iPad mini (2nd gen)
	APL5698	Cyclone	ARMv8-A	28 nm	$102 \text{ mm}^2$	10/2013	iPad Air
A8	APL1011	Typhoon (dual-core)	ARMv8-A	20 nm	89 mm <sup>2</sup>	9/2014	iPhone 6, iPhone 6 plus
A8X	APL1012	Typhoon (triple-core)	ARMv8-A	20nm	128 mm <sup>2</sup>	10/2014	iPad Air 2
A9	APL0898 APL1022	Twister (dual-core)	ARMv8-A	14nm FinFET 16nm FinFET	96 mm <sup>2</sup> 104.5 mm <sup>2</sup>	9/2015	iPhone 6S, 6S Plus iPad (2017)
A9X	APL1021	Twister (dual-core)	ARMv8-A	16nm FinFET	143.9 mm <sup>2</sup>	11/2015	iPad Pro (12.9". 9.7")
A10	APL1W24	Hurricane (quad-core)	ARMv8-A	16nm FinFET	$125 \text{ mm}^2$	9/2016	iPhone 7, 7 Plus
A10X	APL1071	Hurricane (hex-core)	ARMv8-A	10nm FinFET	$96.4 \text{ mm}^2$	6/2017	iPad Pro (10.5", 12.9")

Source:http://en.wikipedia.org/wiki/Apple\_(system\_on\_chip), as of 6/2017



## SoC Example: NVIDIA Tegra 2

NVIDIA			
2010			
ARM Cortex-A9 (dual-core)			
Up to 1.2 GHz			
1 GB 667 MHz LP-DDR2			
ULP GeForce			
40 nm			
12 x12 mm (Package on Package)			
Acer Iconia Tab A500 Asus Eee Pad Transformer Motorola Xoom Motorola Xoom Family Edition Samsung Galaxy Tab 10.1 Toshiba Thrive			

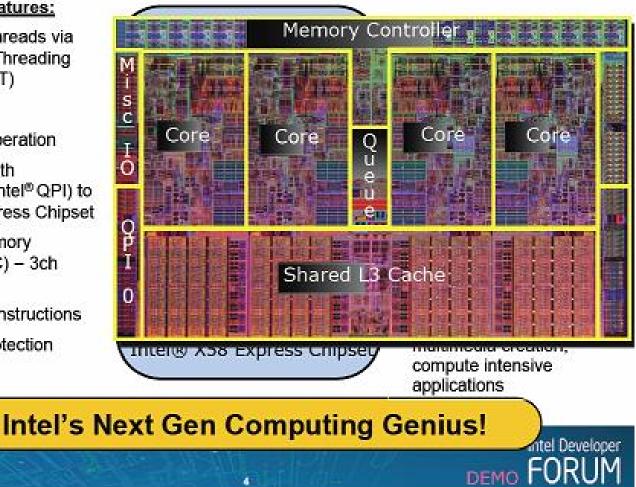


Picture source: http://www.anandtech.com/, http://www.nvidia.com/

#### Intel<sup>®</sup> Core<sup>™</sup> i7 Processor

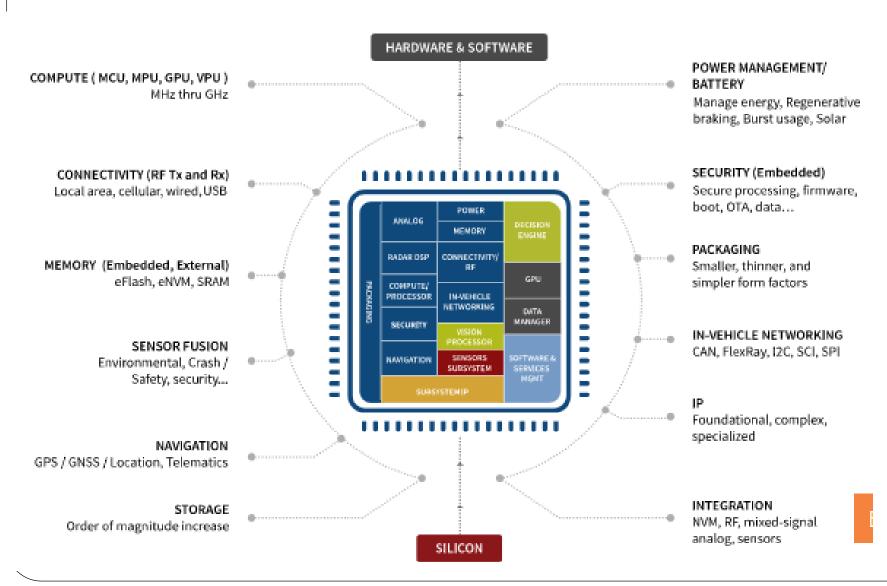
#### Performance/Features:

- 8 processing threads via Intel® Hyper-Threading Technology (HT)
- 4 cores
- Turbo Mode operation
- Intel<sup>®</sup> QuickPath Interconnect (Intel<sup>®</sup> QPI) to Intel<sup>®</sup> X58 Express Chipset
- Integrated Memory Controller (IMC) – 3ch DDR3
- 7 more SSE4 instructions
- Overspeed Protection Removed



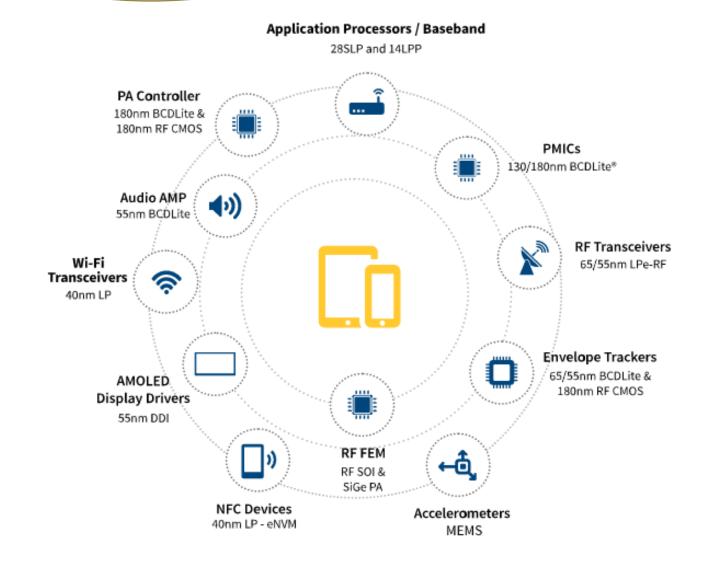




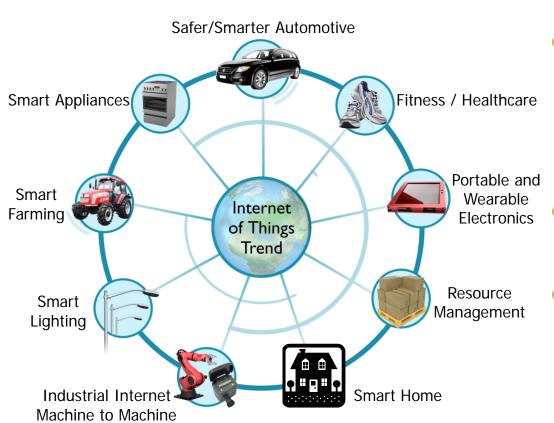








#### SoCs/ASICs for Internet of Things (IoT)



Why Now?

- ASICs are becoming:
  - Cheaper (<50c)
  - Smaller (<1mm<sup>2</sup>)
  - Lower power (µW)
  - Commoditised HW & SW
- Communication is growing faster (broadband)
- Socio-economic benefits
  - Globalisation
  - Automation & control
  - Mobility
  - Smart monitoring
  - Wide range of applications

## "IoT Things" Basic Building Functional Blocks

