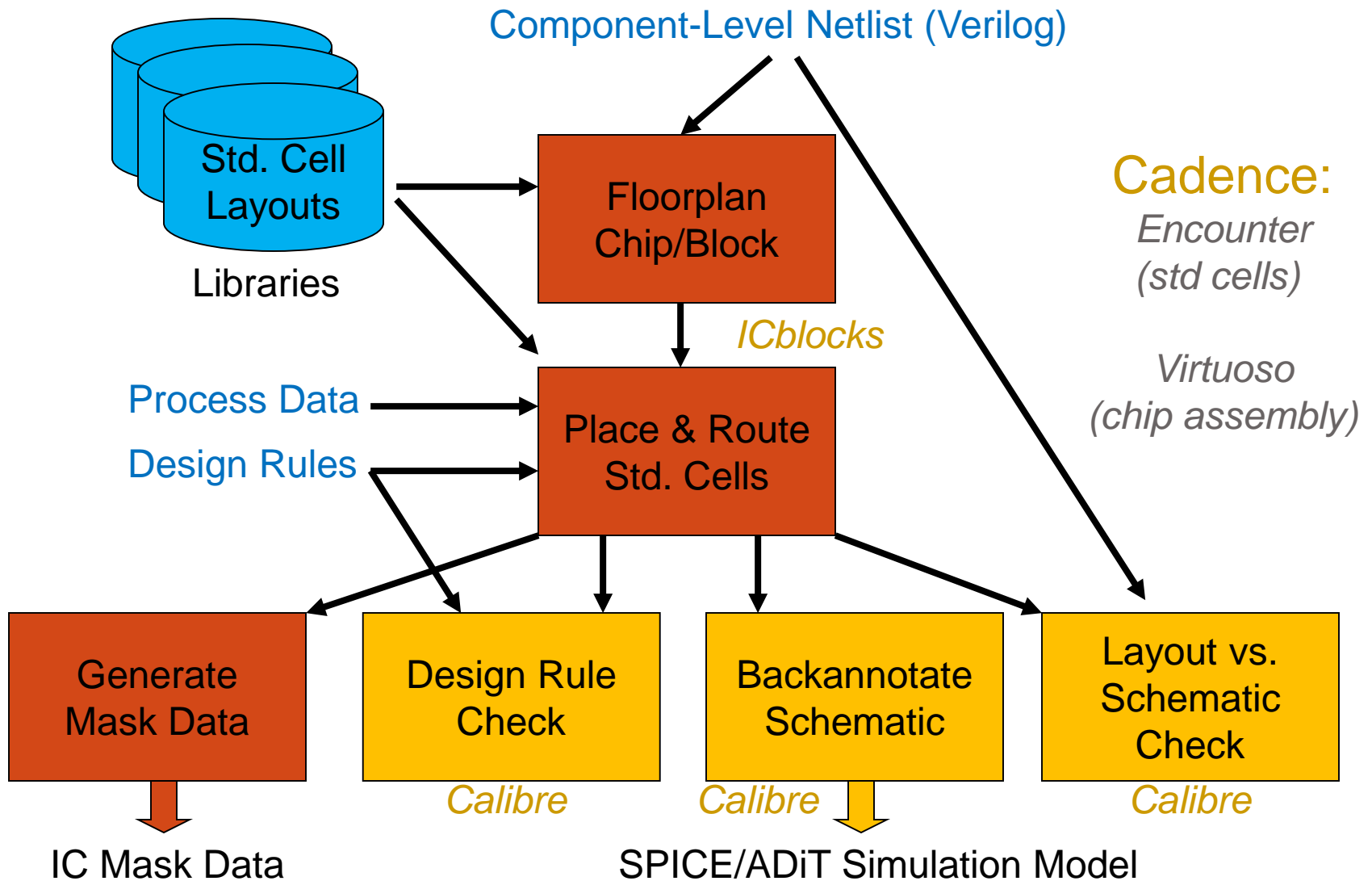


ASIC Physical Design Post-Layout Verification

ASIC Physical Design (Standard Cell)

(can also do full custom layout)



Cadence setup

- Copy files from `/class/ELEC6250/CadenceFiles`

(Replace `dot` with a period. Example: `.cdsenv`)

`dotcdsenv` to your home directory

`dotcdsinit` to your project directory

`cds.lib` to your project directory

`display.drf` to your project directory

`dotsimrc` to your project directory

`addpower.v1.txt` to your project directory

- Edit your `.bashrc` file with the setup information from `/class/ELEC6250/CadenceFiles/dotbasrch`

Import digital block into Virtuoso

- Import GDSII layout information into Virtuoso:
 - Encounter saves: mydesign.gds2
 - Import into a Cadence library
 - File > Import > Stream
 - Results in cell “layout” view
- Import circuit netlist into Virtuoso:
 - Gate-level netlist saved by Encounter: mydesign.v
 - Import netlist into a Cadence Library
 - File > Import > Verilog
 - Results in cell “schematic” and “symbol” views
 - Gates replaced by transistors using “cdslib” components

(Demonstration)

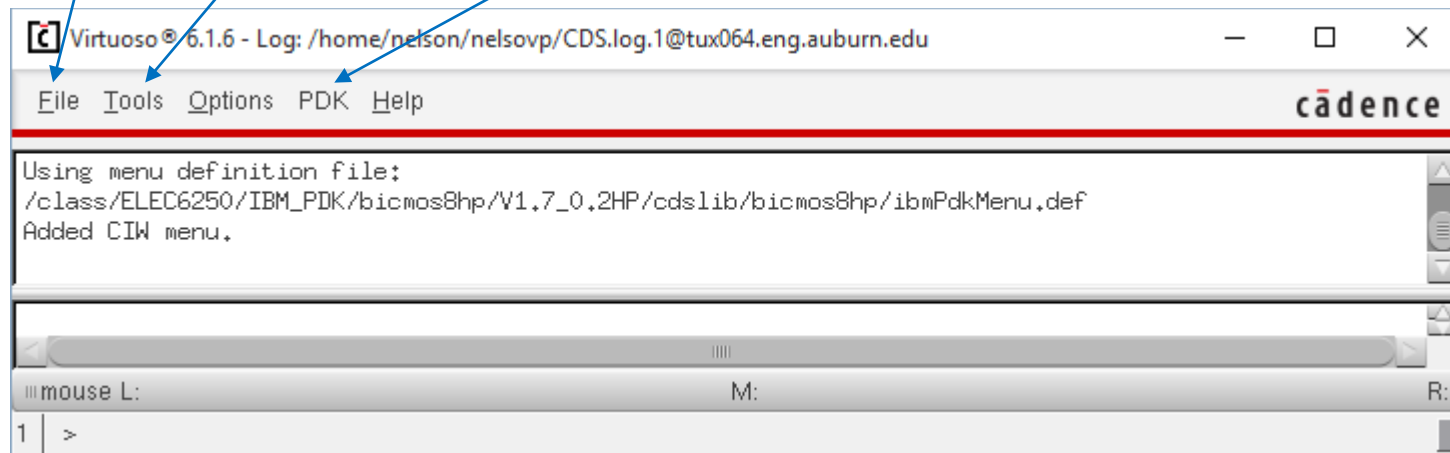
Virtuoso CIW (Command Interpreter Window)

Cadence libraries and tools are accessed from the CIW

Import/Export designs

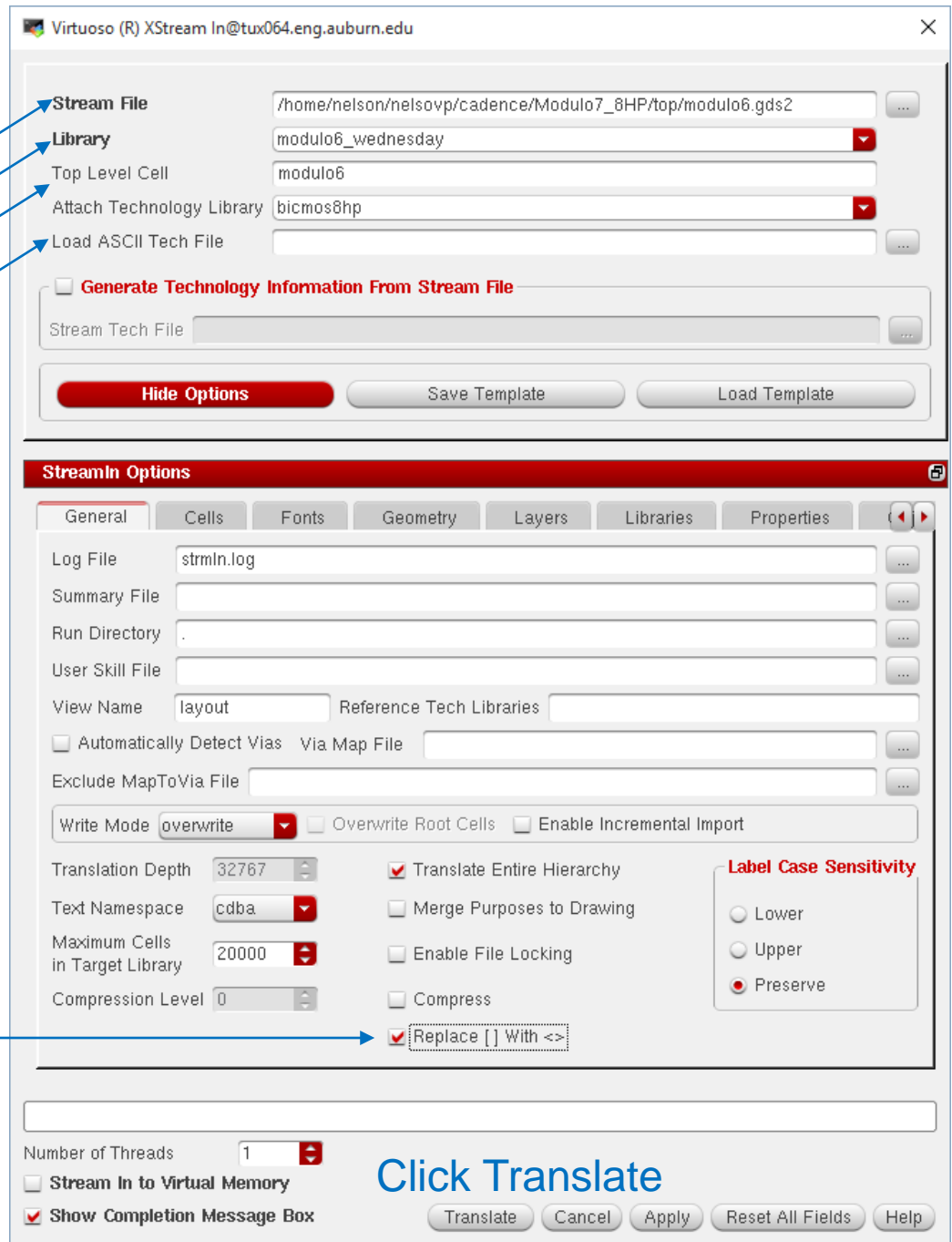
Access libraries

BICMOS8HP PDK Items



File > Import > Stream

GDSII file from Encounter
My library for this cell
Name of top design cell
Technology library



Replace Verilog []
with < >

Click Translate

Translate Cancel Apply Reset All Fields Help

Importing the Verilog netlist

- Verilog netlists saved by Synopsys Design Compiler and Cadence Encounter do not contain ports or definitions of power and ground connections.
- Manually add power/ground connections by executing the following perl script from a linux command line.

```
perl addpowerv1.txt design.v design_vg.v
```

where:

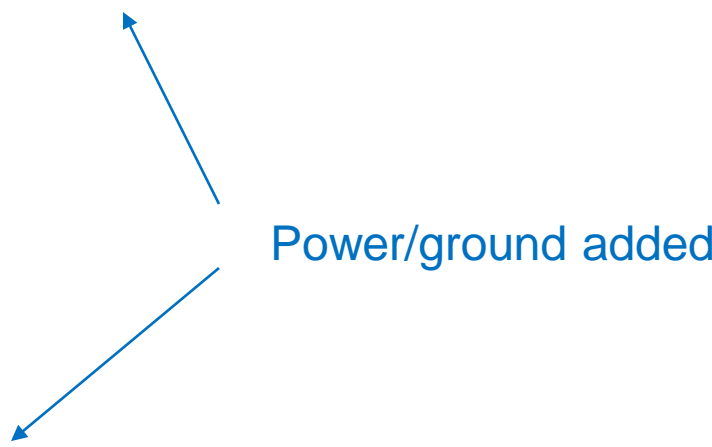
addpowerv1.txt is provided with the setup files

design.v is the netlist generated by Encounter

design_vg.v is the netlist with VDD/GND added

Generated Verilog netlist

```
module modulo6 (VDD, VSS,  
    CLEARbar,  
    L_Cbar,  
    CLK,  
    I,  
    Q);  
inout VDD, VSS;  
input CLEARbar;  
input L_Cbar;  
input CLK;  
input [2:0] I;  
output [2:0] Q;
```



Power/ground added

File > Import > Verilog

My library for this cell
Reference tech library*
Verilog file(s)

* Contains tech file for
"311" bicmos8hp

Creates schematic
and symbol views

Replace Verilog []
with < >

Verilog In@tux064.eng.auburn.edu

Import Options Global Net Options Schematic Generation Options

File Filter Name

./
CDScheck_modulo6_top.log
PEX_runset
PIPO.LOG
PIPO.LOG.modulo6
PIPO.SUM.modulo6
/home/ne1son/ne1sov/cadence/Modulo7_8HP/top

Target Library Name modulo6_wednesday Browse

Reference Libraries cdslib

Verilog Files To Import modulo6_soc_vdvs.v Add

-f Options Add

-v Options Add

-y Options Add

Library Extension

Library Pre-Compilation Options

Pre Compiled Verilog Library

HDL View Name hdl

Target Compile Library Name Browse

Compile Verilog Library Only

Ignore Modules File Add

Import Modules File Add

Import Structural Modules As schematic

Structural View Names

Schematic	schematic	Netlist	netlist
Functional	functional	Symbol	symbol

Log File ./verilogIn.log Work Area /tmp

Name Map Table ./verilogIn.map.table

Overwrite Existing Views

Overwrite Symbol Views Created By VerilogIn

Verilog Cell Modules Create Symbol Only Import Import As Functional

OK Cancel Defaults Apply Load Save Help

Library Manager

The screenshot shows the Cadence Library Manager interface. The title bar reads "Library Manager: Directory ...elsovp/cadence/Modulo7_8HP/top@tux064.eng.auburn.edu". The menu bar includes "File", "Edit", "View", "Design Manager", and "Help". The "cadence" logo is in the top right corner. There are two checkboxes: "Show Categories" and "Show Files".

The interface is divided into three main panes:

- Library:** A list of libraries including "modulo6_wednesday", "8hp_pads", "US_8ths", "analogLib", "avTech", "basic", "bicmos8hp", "cdsDefTechLib", "cdslib", "esd8hp", "esd8hp_legacy", "mod6_monday", "mod6_tuesday", "modulo6_wednesday" (highlighted), "myschematic", "nelson", "new_mod6", "sample", and "sbaLib". A blue arrow points to "modulo6_wednesday" with the text "New library".
- Cell:** A list of cells for the selected library, including "modulo6", "AOI21_A", "AOI22_A", "CLK_H", "DFFS_B", "FILL1", "FILL2", "FILL4", "FILL8", "FILL16", "INVERT_B", "M1_M2_via_1x", "M1_M2_via_1x_h", "M2_M3_via_1x", "M3_MQ_via_1x", "XOR2_A", "iopin", "ipin", "modulo6" (highlighted), and "modulo6_VIA0". A blue arrow points to "modulo6" with the text "New cell".
- View:** A table showing views created by import. The table has columns for "View", "Lock", and "Size".

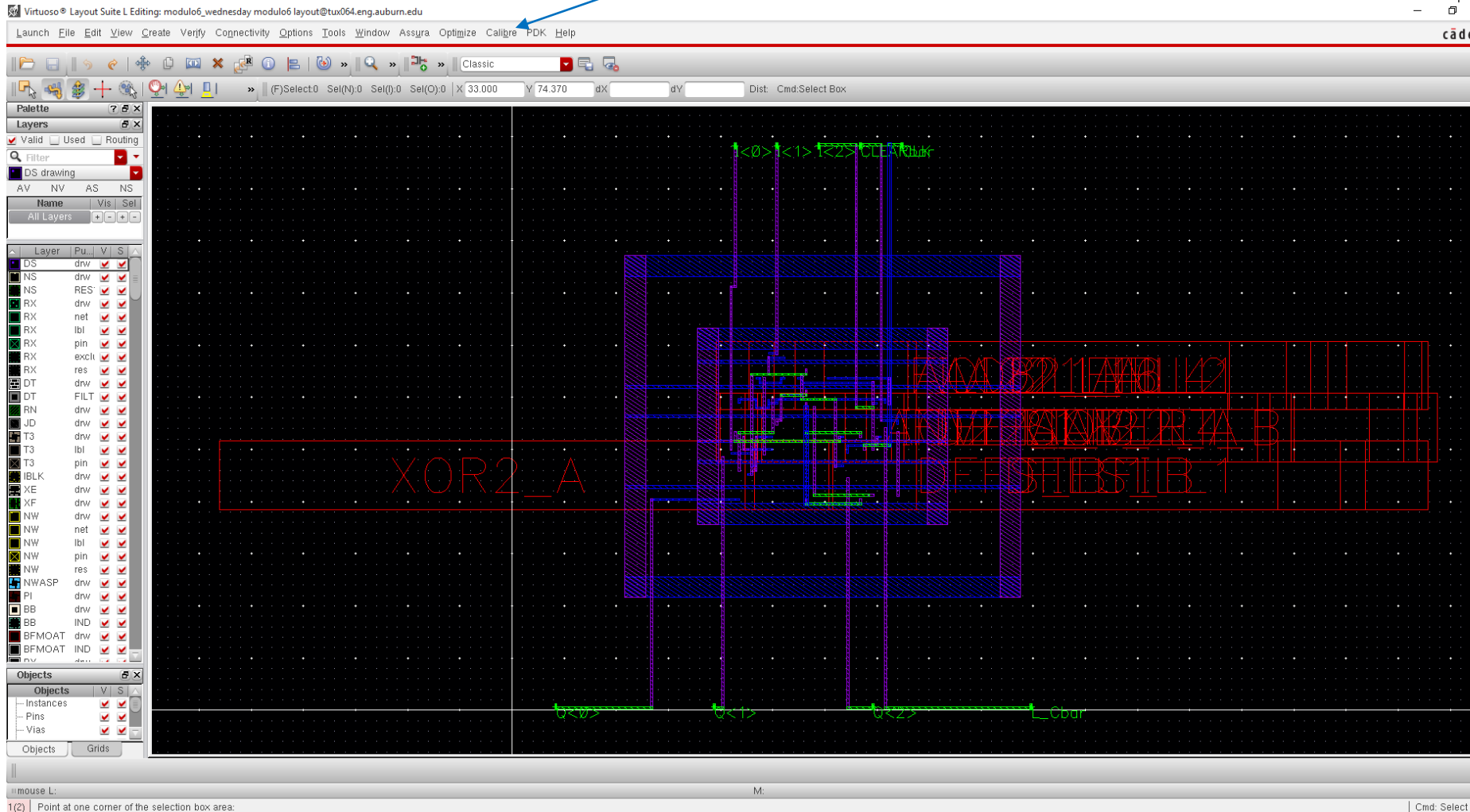
View	Lock	Size
layout		23k
schematic		44k
symbol		27k

A blue arrow points to the "Views created by import" text with the text "Views created by import".

At the bottom, there is a "Messages" pane with the text: "Log file is "/home/nelson/nelsovp/cadence/Modulo7_8HP/top/libManager.log". A blue arrow points from the "Views created by import" text to this message pane with the text "Double-click on view to open it in the appropriate tool." The status bar at the bottom right shows "Lib: modulo6_wednesday | Free: 7.80G".

Layout view of "modulo6"

Calibre LVS/DRC/PEX



1(2) Point at one corner of the selection box area:

Cmd: Select

Schematic view of “modulo6”

The image shows a screenshot of the Cadence Virtuoso Schematic Editor. The title bar reads "Virtuoso® Schematic Editor L Editing: modulo6_wednesday modulo6 schematic@tux064.eng.auburn.edu". The menu bar includes "Launch", "File", "Edit", "View", "Create", "Check", "Options", "Window", "Calibre", "PDK", and "Help". The "cadence" logo is in the top right corner. Below the menu bar is a toolbar with various icons for file operations, editing, and simulation. A secondary toolbar below that shows a "Basic" mode and a search field. On the left side, there are three panels: "Navigator", "Property Editor", and "Search". The "Navigator" panel shows a tree view of the project structure, including a folder named "modulo6" and several components like "CLK_L...CLK_H)", "Q_reg_...FFS_B)", "U14 (AOI21_A)", "U15 (XOR2_A)", "U16 (INVERT_B)", "U17 (INVERT_B)", "U18 (AOI22_A)", "U19 (AOI22_A)", "U20 (AO21_B)", and "U21 (AOI22_A)". The "Property Editor" panel is currently empty. The main workspace displays a schematic diagram of a modulo6 counter circuit. The circuit is implemented on a grid of dots. It features several logic gates (AOI21, XOR2, INVERT, AOI22, AO21) and flip-flops (Q_reg_...FFS_B). The circuit is connected to a clock signal (CLK_L...CLK_H) and a clear signal (CLEAR). The output of the circuit is shown as a series of pulses. The status bar at the bottom indicates "mouse L:", "M:", "R:", and "Cmd: Sel: 0".

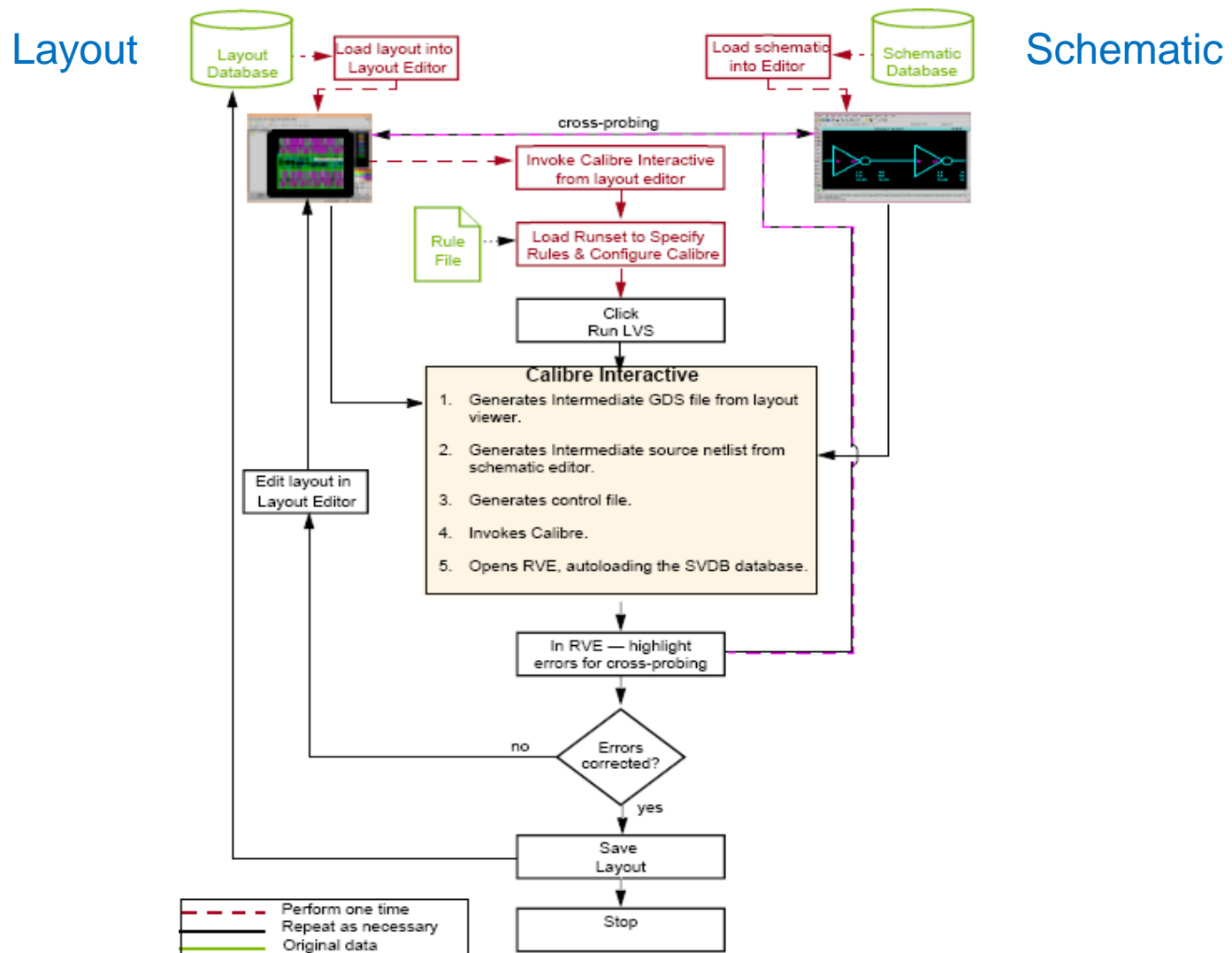
Symbol view of “modulo6”

The screenshot shows the Cadence Virtuoso Symbol Editor interface. The title bar reads "Virtuoso® Symbol Editor L Editing: modulo6_wednesday modulo6 symbol@tux064.eng.auburn.edu". The menu bar includes "Launch", "File", "Edit", "View", "Create", "Check", "Options", "Window", "PDK", and "Help". The "cadence" logo is in the top right corner. The toolbar contains various icons for file operations, navigation, and editing. The "Navigator" pane on the left shows a tree view of the "modulo6" module with sub-elements: CLEARbar, CLK, I<2:0>, L_Cbar, Q<2:0>, VDD!, VSS, CLEARbar: CLEARbar, CLK: CLK, I<2:0>: I, L_Cbar: L_Cbar, Q<2:0>: Q, VDD!: VDD, and VSS: VSS. The "Property Editor" pane is empty. The main workspace displays the symbol view of the "modulo6" module, which is a rectangular block with a green border. The symbol contains the following text: "CLEARbar" (yellow), "L_Cbar" (red), "VDD!" (red), "VSS" (red), "CLK" (red), "modulo6" (green), "Q<2:0>" (red), and "I<2:0>" (red). Red rectangular boxes represent input and output ports on the left and right sides of the symbol.

Verify correctness of layout

- Open layout in Virtuoso
- Verify with Calibre or Assura tools
 1. LVS (layout vs. schematic)
 - Extract netlist from layout
 - Compare extracted netlist to imported netlist
 2. DRC (design rule check)
 - Checks all layout levels
 - Errors should be fixed as appropriate
 3. PEX (parameter extraction)
 - Extract netlist from layout, including R/C parameters
 - Simulate netlist to verify functionality and timing

Calibre Layout-vs-Schematic (LVS) Check



Layout vs schematic check (Calibre Interactive LVS)

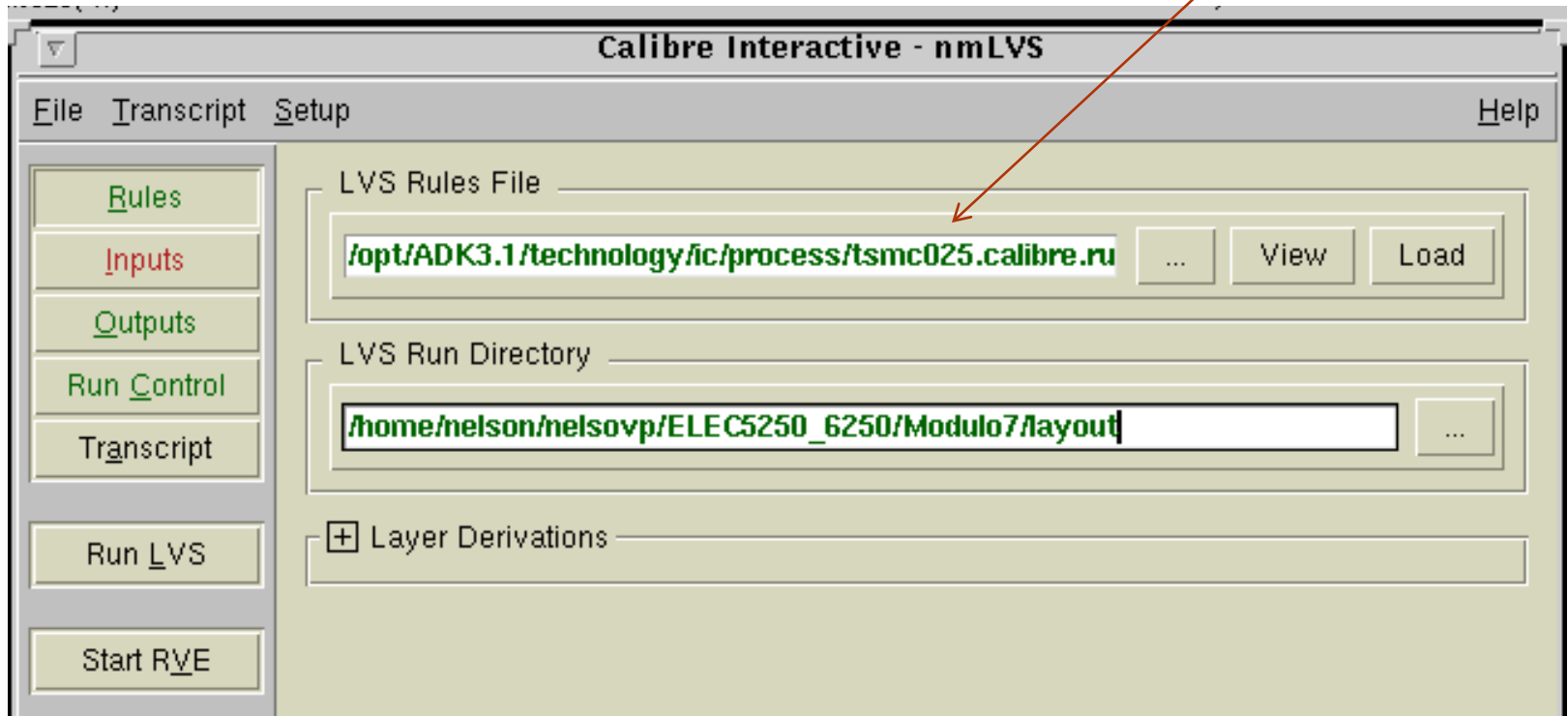
- Compares extracted transistor-level netlist vs. netlist generated from Verilog gate-level netlist
- From Layout GXL menu: *Calibre > Run LVS*
(*Demonstrate*)

Mentor Graphics LVS

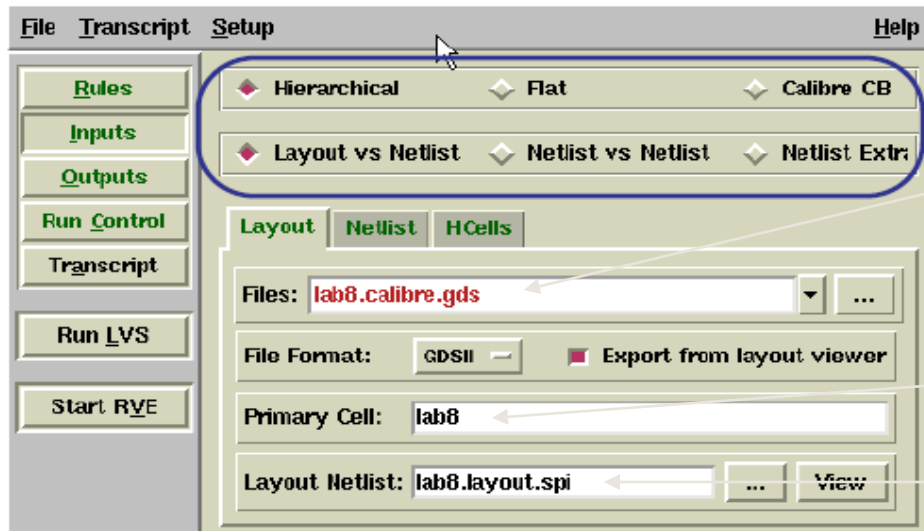
- Rules: *\$ADK/technology/ic/process/tsmc035.calibre.rules*
- Inputs/Layout: *will be generated by Calibre*
- Inputs/Netlist: *count4.src.net* (created in DA-IC)
Top-level cell: *count4* (schematic name)
- Inputs/H-cells (hierarchical cells): *\$ADK/technology/adk.hcell*
- Extracted file: *count4.lay.net*

Load rules file

tsmc035



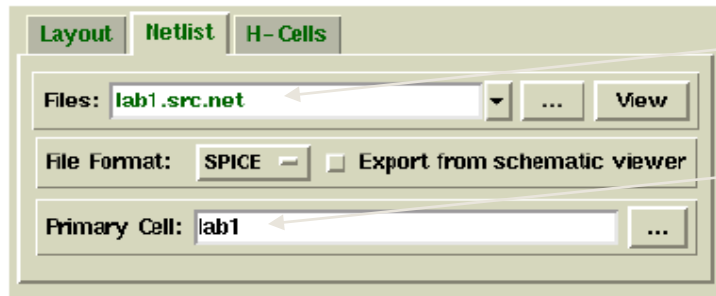
Calibre inputs



Layout to be extracted by Calibre (GDSII format)

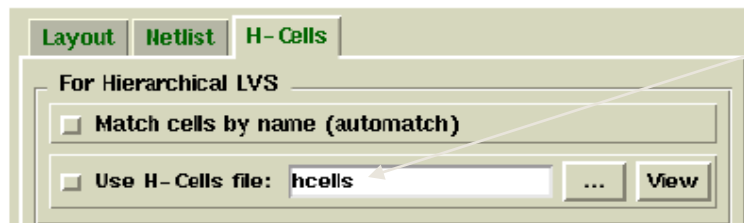
Layout top cell name

Extracted layout netlist



Source netlist created in DA-IC

Schematic name



Hierarchical cells file:

\$ADK/technology/adk.hcell

Calibre RVE to probe LVS results

The screenshot shows the Calibre LVS RVE interface for a design named 'svdb (lab8)'. The interface is divided into several sections:

- Left Panel:** A tree view showing the project structure with folders for 'Input Files' (Rules File, Source Netlist) and 'Output Files' (Layout Netlist, Extraction Report, LVS Report).
- Center Panel:** A tree view of LVS results. The root node is 'LVS Results: Designs Don't Match', which is expanded to show 'a1220 / s1220 - 1 Discrepancy'. This node is further expanded to show 'Incorrect Nets - 1 Discrepancy', which is then expanded to show 'Discrepancy #1'. Below this, several other discrepancy entries are listed with green checkmarks: 'a1230 / s1230', 'a1240 / s1240', 'a1310 / s1310', 'a1620 / s1620', and 'a1720 / s1720'.
- Bottom Panel:** A table titled 'a1220 / s1220: Discrepancy #1 - Incorrect Nets'. It has two columns: 'LAYOUT NAME' and 'SOURCE NAME'. The first row shows 'Net 2' in the layout name column and '2' in the source name column.

Annotations with callout boxes provide instructions:

- 'Expand the results tree to display individual discrepancies.' points to the 'Incorrect Nets' node.
- 'Click a discrepancy to display information.' points to the 'Discrepancy #1' node.
- 'Double-click a net or instance name to highlight in a layout viewer.' points to the 'Net 2' entry in the table.

At the bottom left, the status bar indicates 'Query Cell: lab8'.

The screenshot shows a layout viewer window titled 'Cells'. On the left, a cell hierarchy is listed:

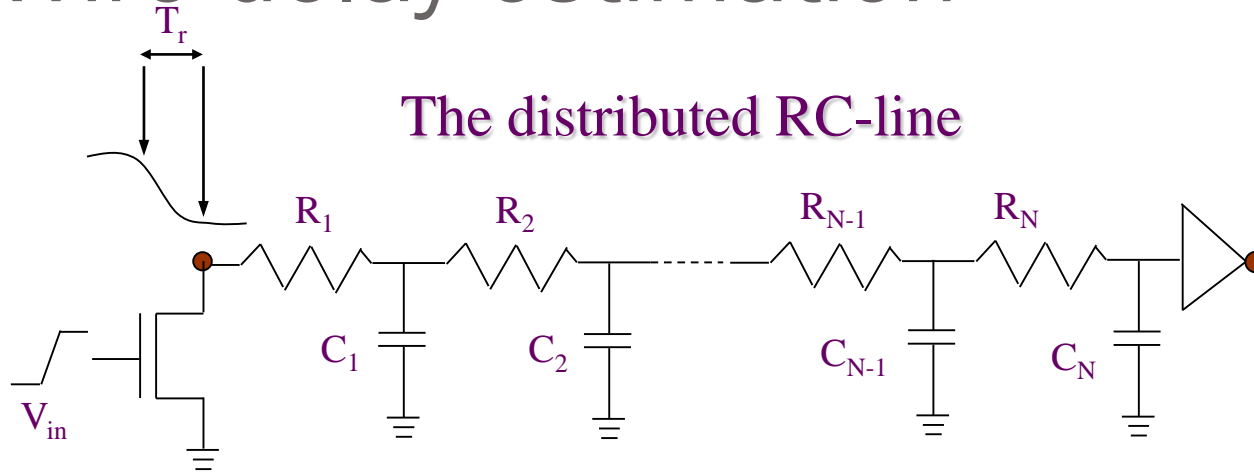
- lab0
- a1220
- s1230
- a1240
- a1310
- s1620
- a1720
- s2311
- s3500

The main area of the window displays a physical layout of the design. The layout is divided into several regions, some of which are highlighted with green hatching. A blue square highlights a specific net in the layout, and a red square highlights another net. A blue arrow points from the 'Net 2' entry in the table above to the highlighted net in the layout.

Post-layout functional/timing verification (Calibre PEX)

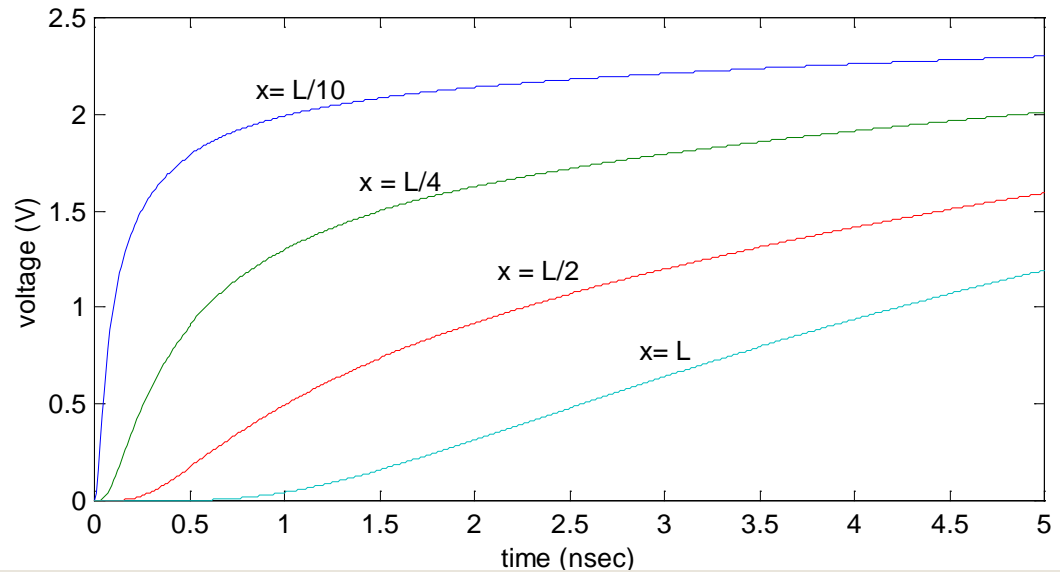
- Purpose: timing analysis & functional verification of the final design
 - analyze netlist extracted from layout
 - parasitic wire capacitance
 - parasitic wire to wire capacitance
 - net and via resistance
 - perform netlist & parameter extraction with *Calibre PEX*
 - simulate in *ADiT, Eldo, Spectre, PSPICE, HSPICE, etc.*

Wire delay estimation

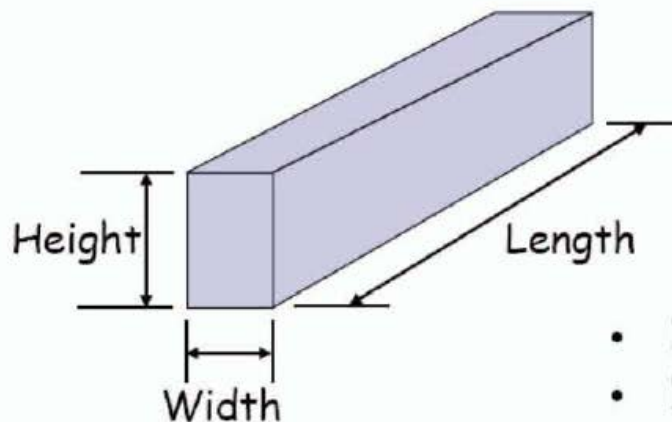


Diffused signal propagation

$$\text{Delay} \sim L^2$$



Wire resistance



$$\text{resistance} = \frac{(\text{length} \times \text{resistivity})}{(\text{height} \times \text{width})}$$

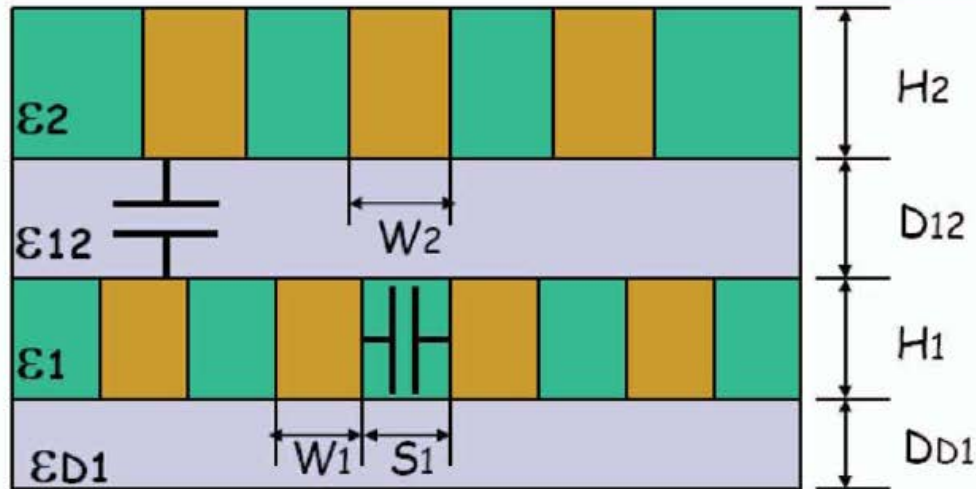
- bulk aluminum $2.8 \times 10^{-8} \Omega\text{-m}$
- bulk copper $1.7 \times 10^{-8} \Omega\text{-m}$
- bulk silver $1.6 \times 10^{-8} \Omega\text{-m}$

- Height (Thickness) fixed in given manufacturing process
- Resistances quoted as Ω/square
- TSMC 0.18 μm 6 Aluminum metal layers
 - M1-5 0.08 Ω/square (0.5 μm \times 1mm wire = 160 Ω)
 - M6 0.03 Ω/square (0.5 μm \times 1mm wire = 60 Ω)

Courtesy of Arvind and Krste Asanovic. Used with permission.

Cite as: Vladimir Stojanovic, course materials for 6.973 Communication System Design, Spring 2006.
MIT OpenCourseWare (<http://ocw.mit.edu/>), Massachusetts Institute of Technology.
Downloaded on [DD Month YYYY].

Wire capacitance



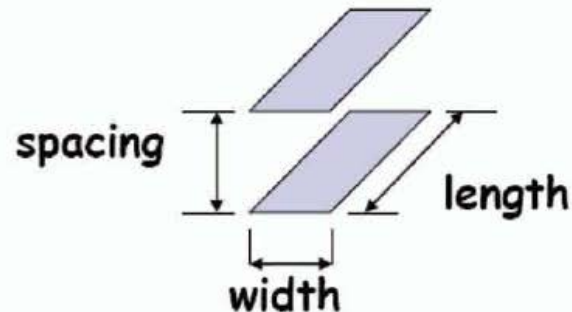
- Capacitance depends on geometry of surrounding wires and relative permittivity, ϵ_r , of insulating dielectric
 - silicon dioxide, SiO_2 $\epsilon_r = 3.9$
 - silicon flouride, SiOF $\epsilon_r = 3.1$
 - SiLK™ polymer, $\epsilon_r = 2.6$
- Can have different materials between wires and between layers, and also different materials on higher layers

Courtesy of Arvind and Krste Asanovic. Used with permission.

Cite as: Vladimir Stojanovic, course materials for 6.973 Communication System Design, Spring 2006.
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Downloaded on [DD Month YYYY].

Capacitance scaling

parallel plate capacitance $\propto \frac{\text{width}}{\text{spacing}} \times \text{length}$

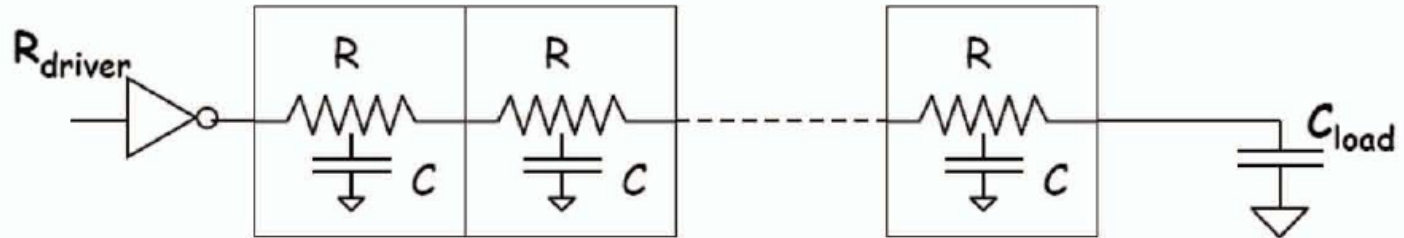


- Capacitance/unit length ~constant with feature size scaling (width and spacing scale together)
 - Isolated wire sees approx. 100 fF/mm
 - With close neighbors about 160 fF/mm
- **Need to use capacitance extractor to get accurate values**

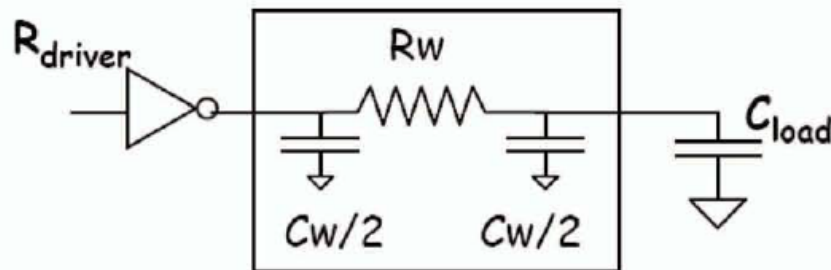
Courtesy of Arvind and Krste Asanovic. Used with permission.

Cite as: Vladimir Stojanovic, course materials for 6.973 Communication System Design, Spring 2006.
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Downloaded on [DD Month YYYY].

Wire delay models



- Wire has distributed R and C per unit length
 - wire delay increases quadratically with length
 - edge rate also degrades quadratically with length
- Simple lumped Π model gives reasonable approximation
 - R_w is lumped resistance of wire
 - C_w is lumped capacitance (put half at each end)



$$\text{Delay} = R_{\text{driver}} \times \frac{C_w}{2} + (R_{\text{driver}} + R_w) \times \left(\frac{C_w}{2} + C_{\text{load}} \right)$$

Courtesy of Arvind and Krste Asanovic. Used with permission.

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Wire delay example

- In 0.18 μm TSMC, 5x minimum inverter with effective resistance of 3 k Ω , driving FO4 load (25fF)
- Delay = $R_{\text{driver}} \times C_{\text{load}} = 75 \text{ ps}$
- Now add 1mm M1 wire, 0.25 μm wide
 - $R_w = 320\Omega$ wire + 22 Ω vias = 344 Ω
 - $C_w = 160\text{fF}$

$$\begin{aligned}\text{Delay} &= R_{\text{driver}} \times \frac{C_w}{2} + (R_{\text{driver}} + R_w) \times \left(\frac{C_w}{2} + C_{\text{load}} \right) \\ &= 3\text{k}\Omega \times 80\text{fF} + (3\text{k}\Omega + 344\Omega) \times (80\text{fF} + 25\text{fF}) \\ &= 591\text{ps}\end{aligned}$$

Courtesy of Arvind and Krste Asanovic. Used with permission.

Cite as: Vladimir Stojanovic, course materials for 6.973 Communication System Design, Spring 2006.
MIT OpenCourseWare (<http://ocw.mit.edu/>), Massachusetts Institute of Technology.
Downloaded on [DD Month YYYY].

Parameter extraction with Calibre PEX

- Extract SPICE netlist, including parasitic RC
 - *Transistor-level*, gate-level, or hierarchical extraction
- With the layout cell open:
 - In the menu bar: *Calibre>Run PEX*
 - Input options: *similar to Calibre LVS*
 - Extraction options (Outputs tab):
 - choose *“Transistor level”*
 - choose one of:
 - *C: lumped C + coupling cap’s*
 - *RC: distributed RC*
 - *RCC: distributed RC + coupling cap’s*
 - Click *“Run PEX”*
 - Output files: *modulo5.sp* - main SPICE model (transistors)
modulo5.sp.pex - extracted R/C (lumped)
modulo5.sp.MODULO5.pxi - extracted C (coupling)

Extracted file – top level

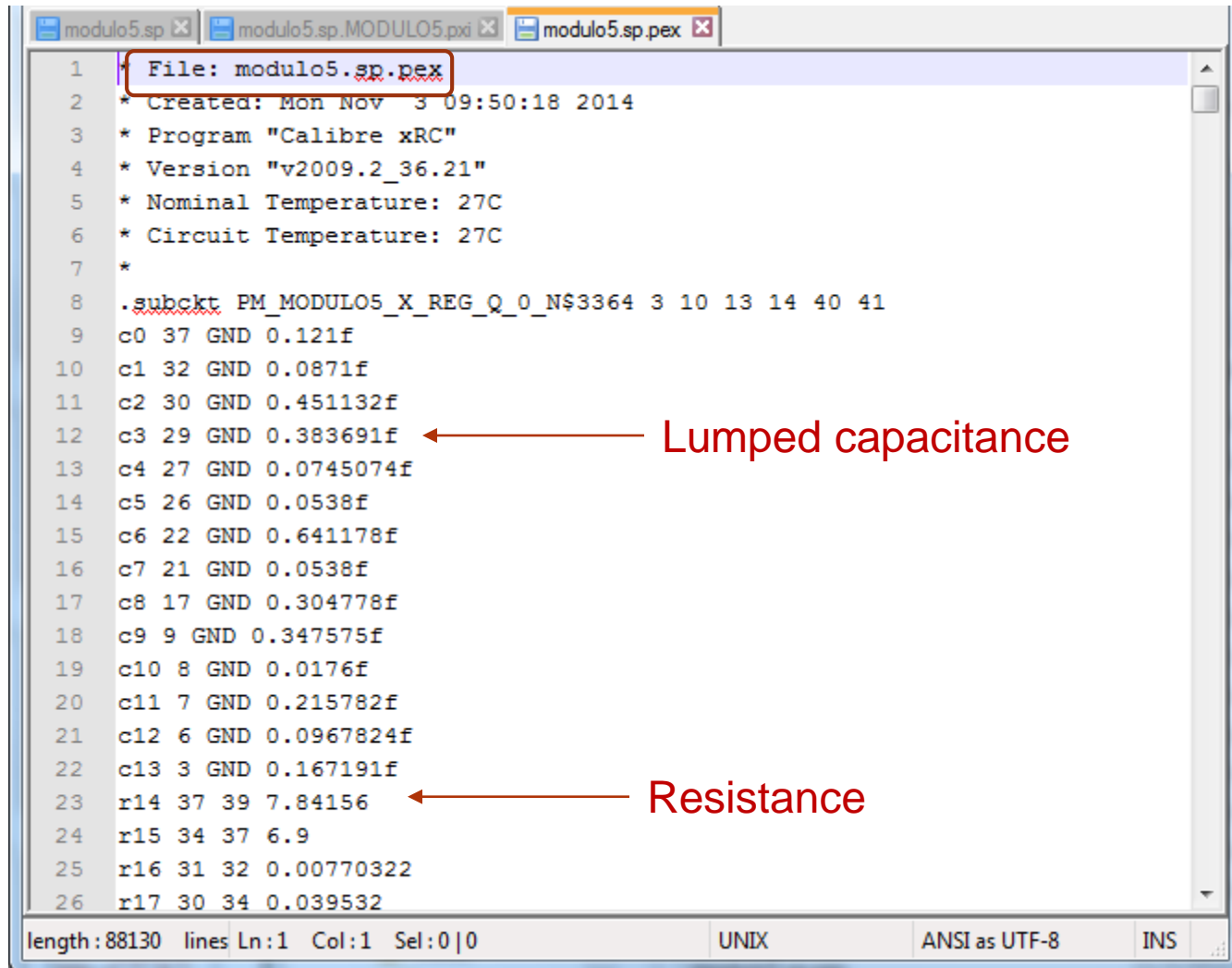
```
1 * File: modulo5.sp
2 * Created: Mon Nov 3 09:50:18 2014
3 * Program "Calibre xRC"
4 * Version "v2009.2_36.21"
5 *
6 .include "modulo5.sp.pex"
7 .global GND VDD
8 .subckt modulo5 I[0] I[1] I[2] Q[0] Q[1] Q[2] L_CBAR CLK CLEARBAR
9 *
10 * VDD VDD
11 * GND GND
12 * L_CBAR L_CBAR
13 * Q[2] Q[2]
14 * CLK CLK
15 * Q[1] Q[1]
16 * CLEARBAR CLEARBAR
17 * I[0] I[0]
18 * Q[0] Q[0]
19 * I[2] I[2]
20 * I[1] I[1]
21 mX IX3 M IS212 N NX2 X ix3 M IS212_d N X IX3 NS5 X ix3 M IS212_g
22 + N_GND X ix3 M IS212_s N_GND X reg_Q_0 M IS1901_b N L=4e-07 W=1e-06
23 mX IX3 M IS211 N NX2 X ix3 M IS211_d N X IX3 NS5 X ix3 M IS211_g
24 + N_VDD X ix3 M IS211_s N_VDD X reg_Q_1 M IS1899_b P L=4e-07 W=1.8e-06
25 mX IX3 M IS5 N X IX3 NS5 X ix3 M IS5_d N Q[0] X ix3 M IS5_g
26 N_GND X ix3 M IS5_s
27 + N_GND X reg_Q_0 M IS1901_b N L=4e-07 W=1e-06
28 mX IX3 M IS4 N X IX3 NS5 X ix3 M IS4_d N Q[1] X ix3 M IS4_g
29 N_GND X ix3 M IS4_s
30 + N_GND X reg_Q_0 M IS1901_b N L=4e-07 W=1e-06
31 mX IX3 M IS3 N X IX3 NS5 X ix3 M IS3_d N Q[1] X ix3 M IS3_g
32 + N X IX3 NS1 X ix3 M IS3_s N_VDD X reg_Q_1 M IS1899_b P L=4e-07 W=2.6e-06
33 mX IX3 M IS2 N X IX3 NS1 X ix3 M IS2_d N Q[0] X ix3 M IS2_g
```

File: modulo5.sp

Include extracted R/C

N transistor
source drain bulk gate

Extracted file – extracted R/C

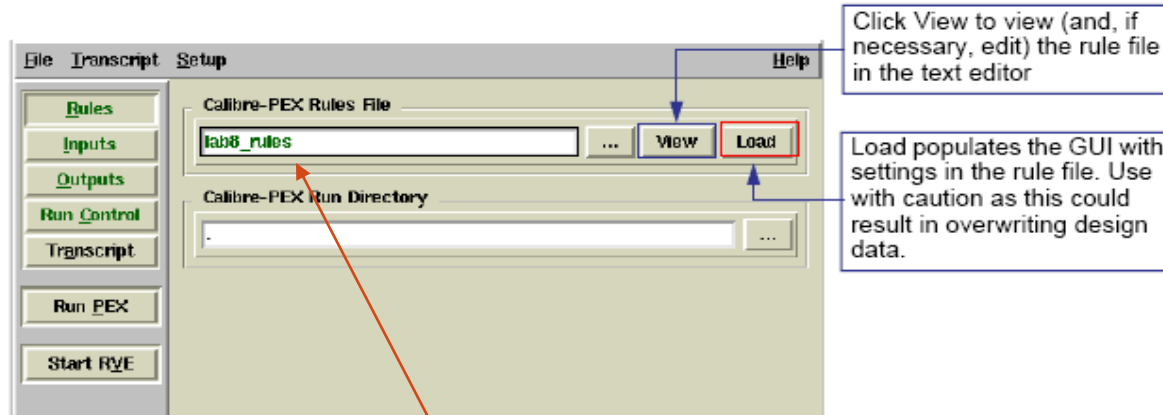


The image shows a screenshot of a text editor window with three tabs: 'modulo5.sp', 'modulo5.sp.MODULO5.pxi', and 'modulo5.sp.pex'. The active tab is 'modulo5.sp.pex', which contains the following text:

```
1 File: modulo5.sp.pex
2 * Created: Mon Nov 3 09:50:18 2014
3 * Program "Calibre xRC"
4 * Version "v2009.2_36.21"
5 * Nominal Temperature: 27C
6 * Circuit Temperature: 27C
7 *
8 .subckt PM_MODULO5_X_REG_Q_0_N$3364 3 10 13 14 40 41
9 c0 37 GND 0.121f
10 c1 32 GND 0.0871f
11 c2 30 GND 0.451132f
12 c3 29 GND 0.383691f ← Lumped capacitance
13 c4 27 GND 0.0745074f
14 c5 26 GND 0.0538f
15 c6 22 GND 0.641178f
16 c7 21 GND 0.0538f
17 c8 17 GND 0.304778f
18 c9 9 GND 0.347575f
19 c10 8 GND 0.0176f
20 c11 7 GND 0.215782f
21 c12 6 GND 0.0967824f
22 c13 3 GND 0.167191f
23 r14 37 39 7.84156 ← Resistance
24 r15 34 37 6.9
25 r16 31 32 0.00770322
26 r17 30 34 0.039532
```

The status bar at the bottom of the editor shows: 'length: 88130 lines Ln: 1 Col: 1 Sel: 0 | 0', 'UNIX', 'ANSI as UTF-8', and 'INS'.

Calibre PEX inputs



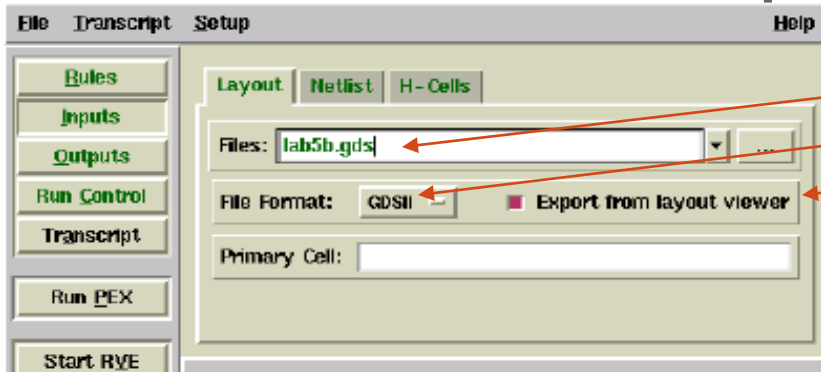
Click View to view (and, if necessary, edit) the rule file in the text editor

Load populates the GUI with settings in the rule file. Use with caution as this could result in overwriting design data.

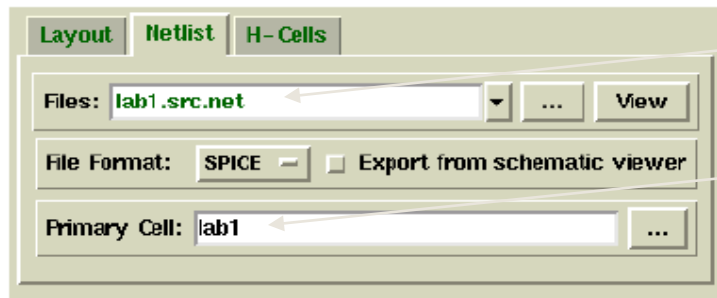
Specify rules file:

`$ADK/technology/ic/process/tsmc035.calibre.rules`

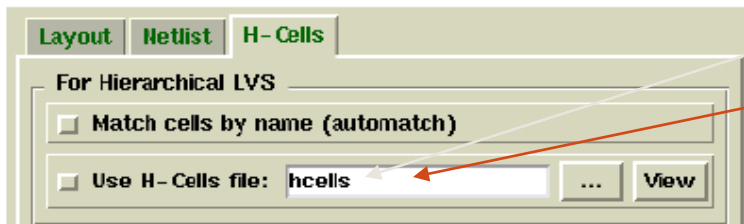
Calibre PEX inputs



- Name of layout file (count4.gds)
- GDSII file format
- Check to generate new layout file
- Name of top cell (count4)

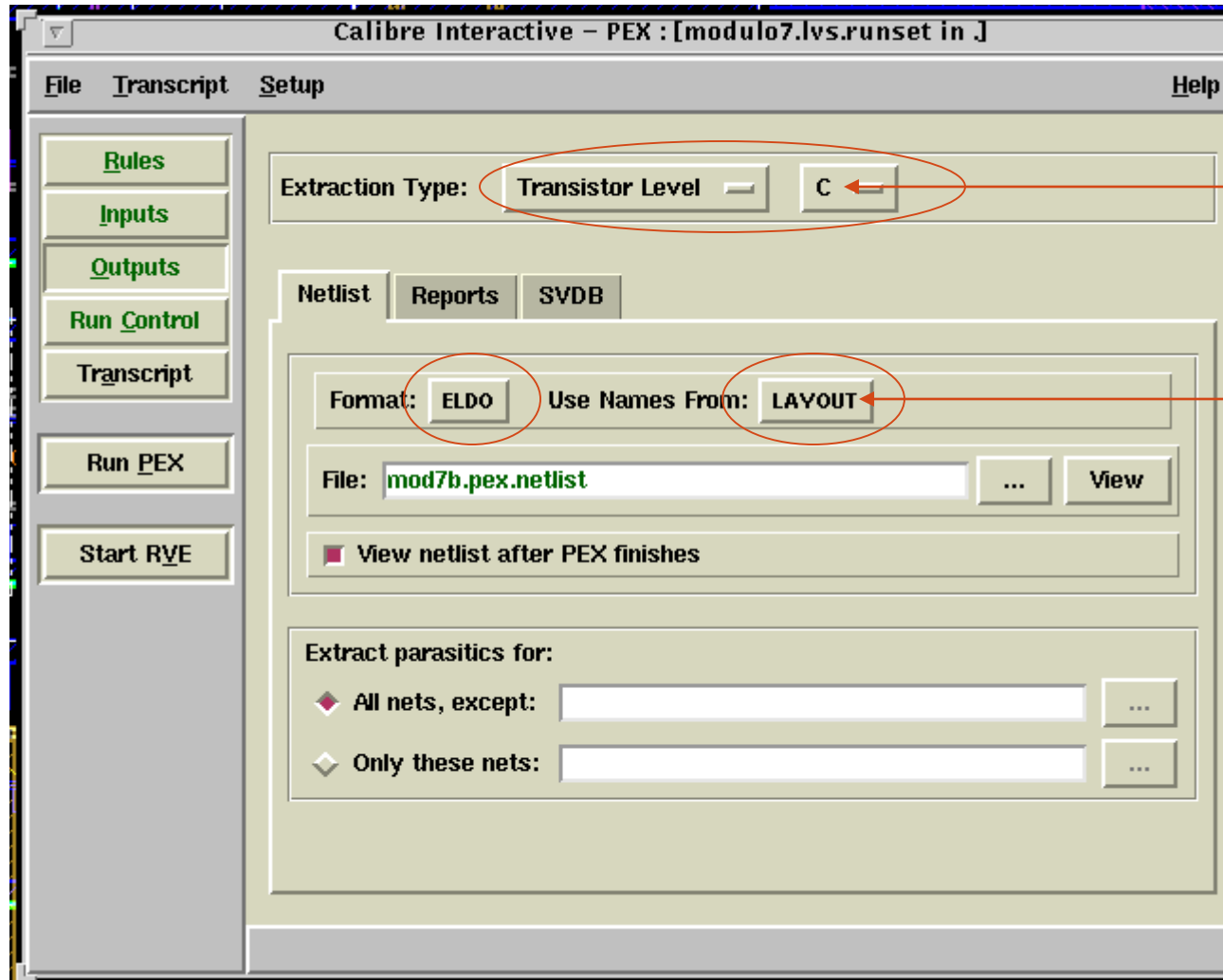


- Source(SPICE) netlist created in DA-IC
- Top-level cell name in SPICE netlist



- Hierarchical cells file:
\$ADK/technology/adk.hcell

Calibre PEX netlist output



Lumped capacitance

Use net names from LAYOUT

Designate GND and VDD nets

