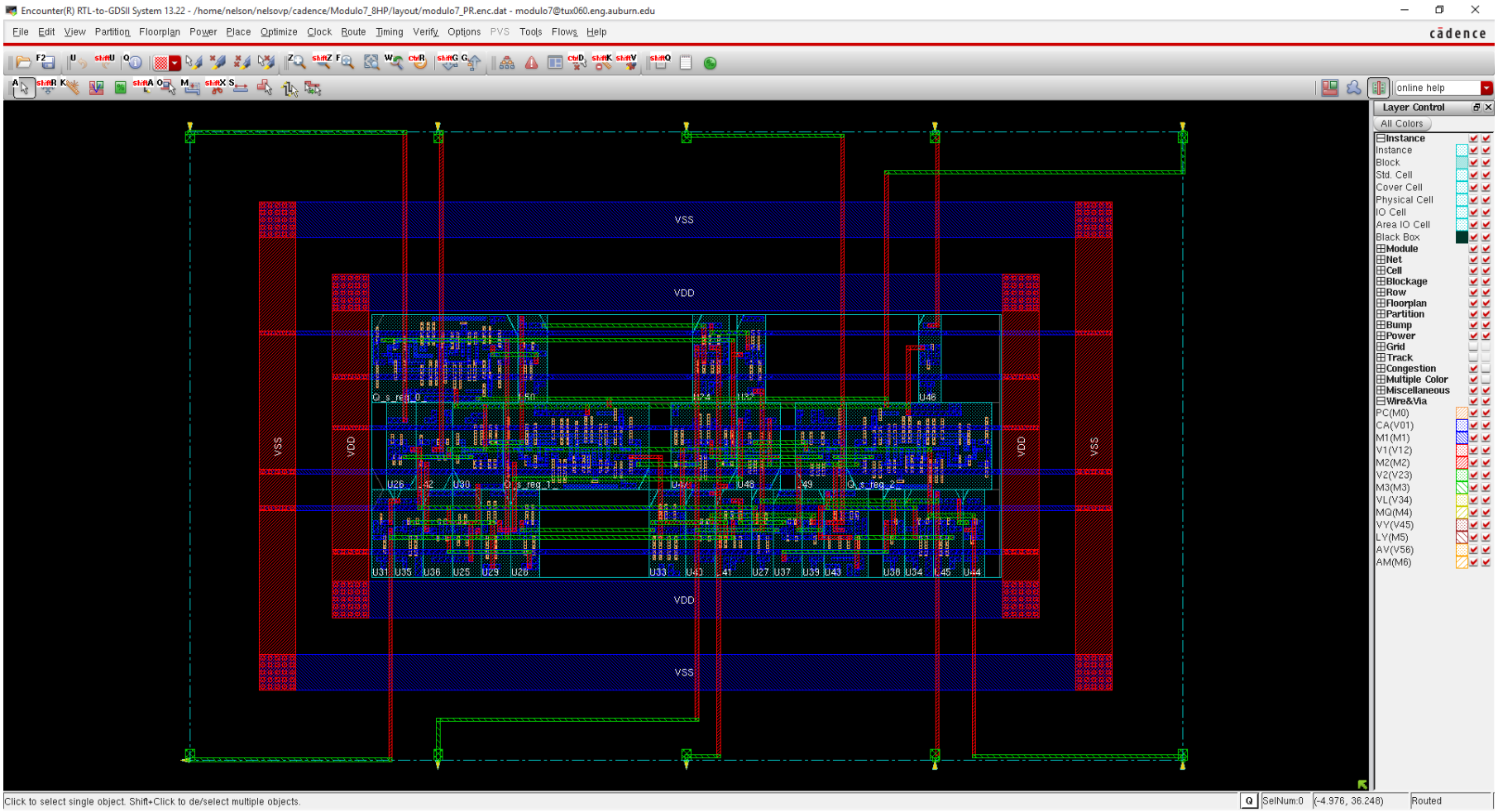
ASIC Physical Design
CMOS Processes

Smith Text: Chapters 2 & 3
Weste – "CMOS VLSI Design"
Global Foundries: "BiCMOS_8HP8XP_Training.pdf"
"BiCMOS_8HP_Design_Manual.pdf"

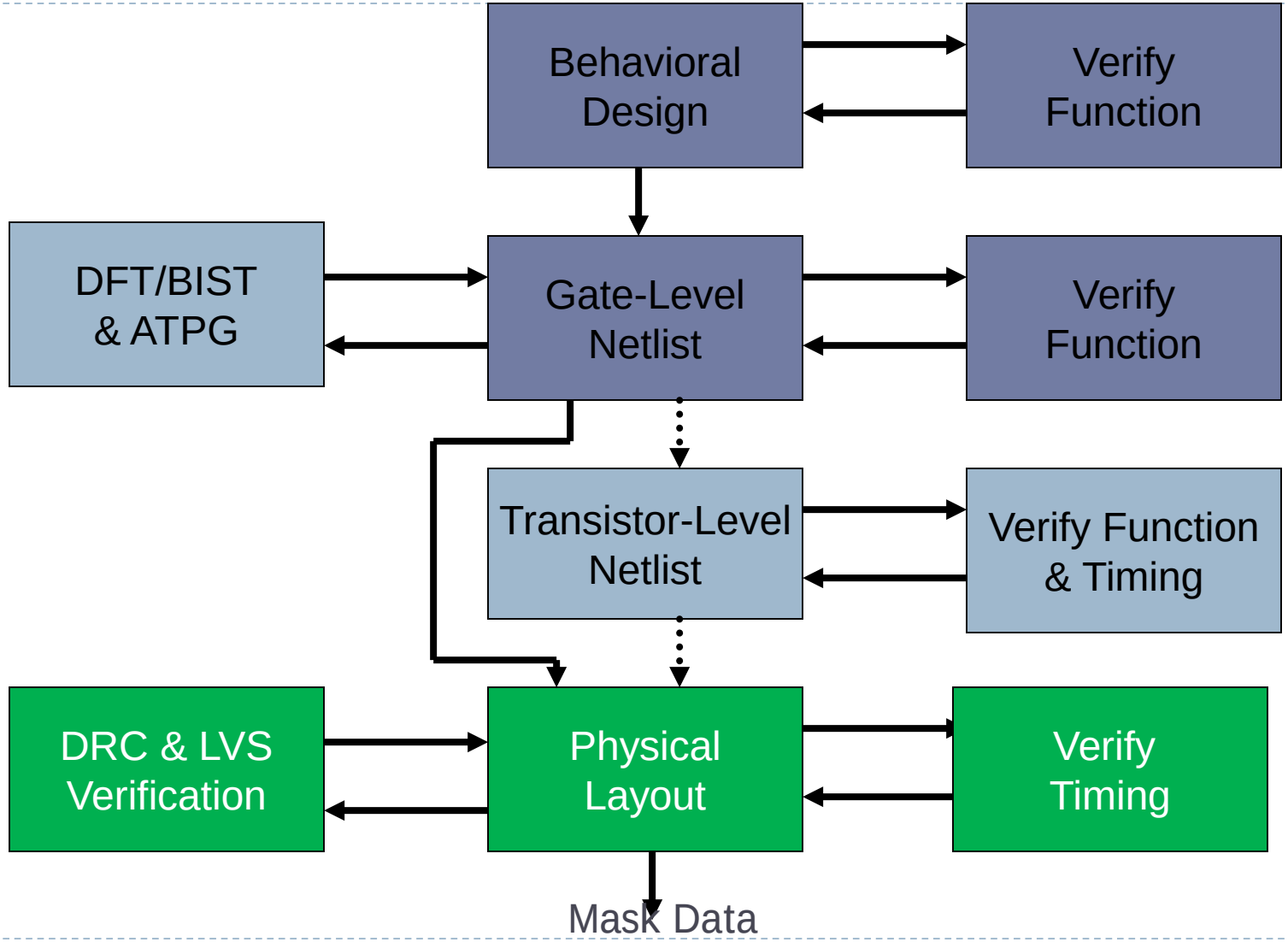
Physical design process overview

- CMOS transistor structure and fabrication steps
- Standard cell layouts
- Creation, verification & characterization of a standard-cell based logic circuit block
- Creation of a chip from circuit blocks

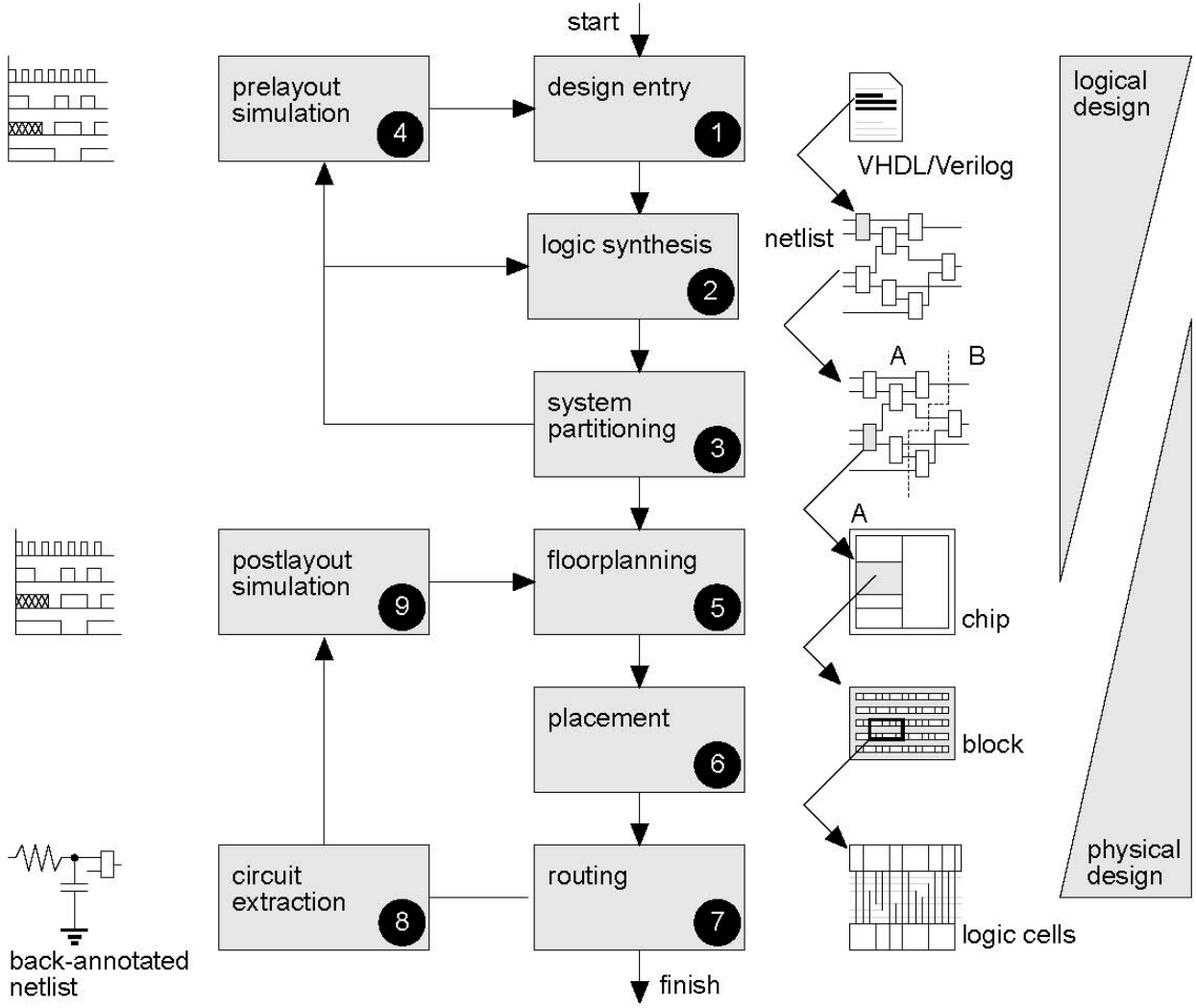
ASIC layout


Encounter(R) RTL-to-GDSII System 13.22 - /home/nelson/nelsovp/cadence/Modulo7_8HP/layout/modulo7_PR.enc.dat - modulo7@tux060.eng.auburn.edu
File Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools Flows Help
cadence
online help
Layer Control
All Colors
Instance
Instance
Block
Std. Cell
Cover Cell
Physical Cell
IO Cell
Area IO Cell
Black Box
Module
Net
Cell
Blockage
Row
Floorplan
Partition
Bump
Power
Grid
Track
Congestion
Multiple Color
Miscellaneous
Wire&Via
PC(M0)
CA(V01)
M1(M1)
V1(V12)
M2(M2)
V2(V23)
M3(M3)
VL(V34)
MQ(M4)
VY(V45)
LY(M5)
AV(V56)
AM(M6)
VSS
VDD
VSS
VDD
VDD
VSS
VDD
Click to select single object. Shift+Click to de/select multiple objects.
SelNum:0
(-4.976, 36.248)
Routed

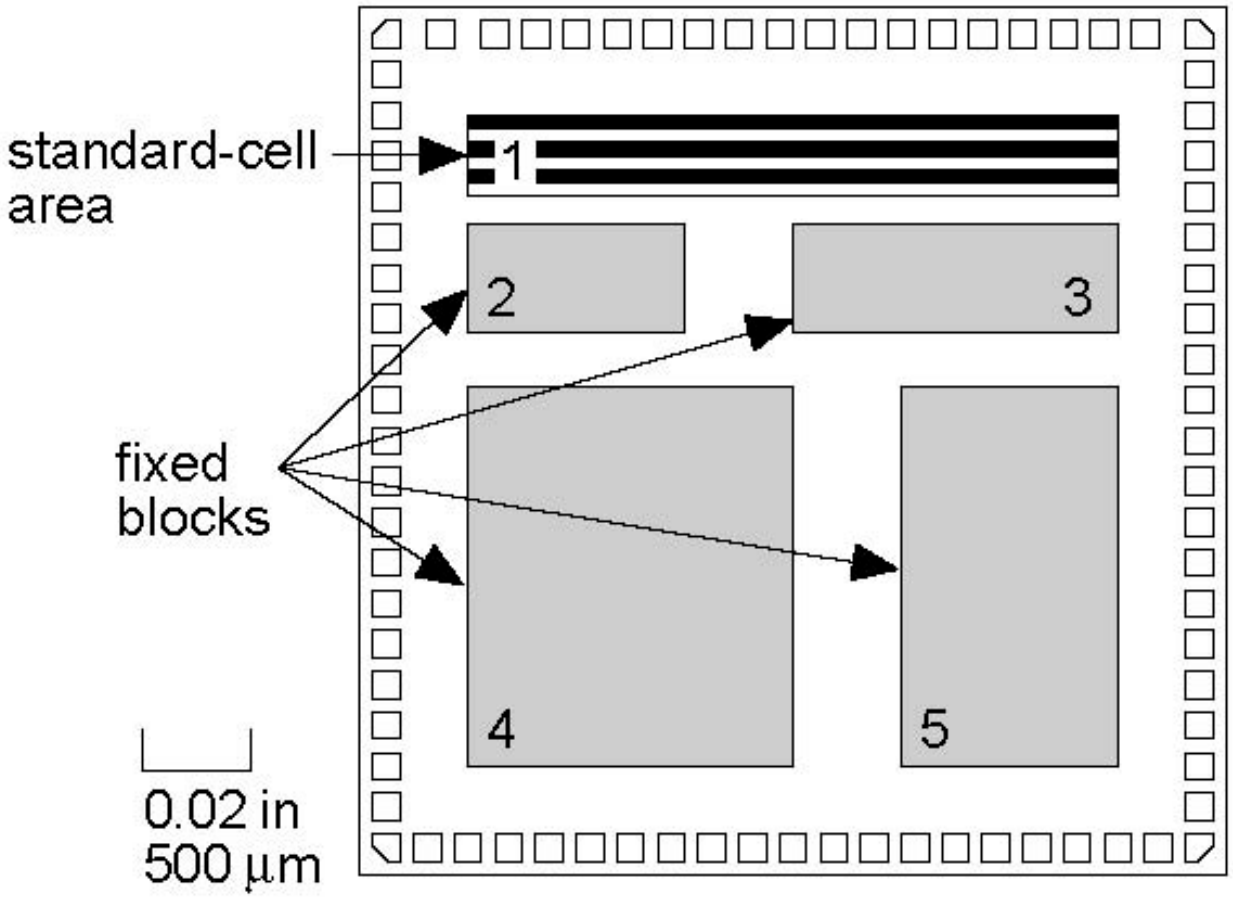
ASIC Design Flow



ASIC Design Flow



IC “Floorplan”



CMOS standard cell layout (generic)

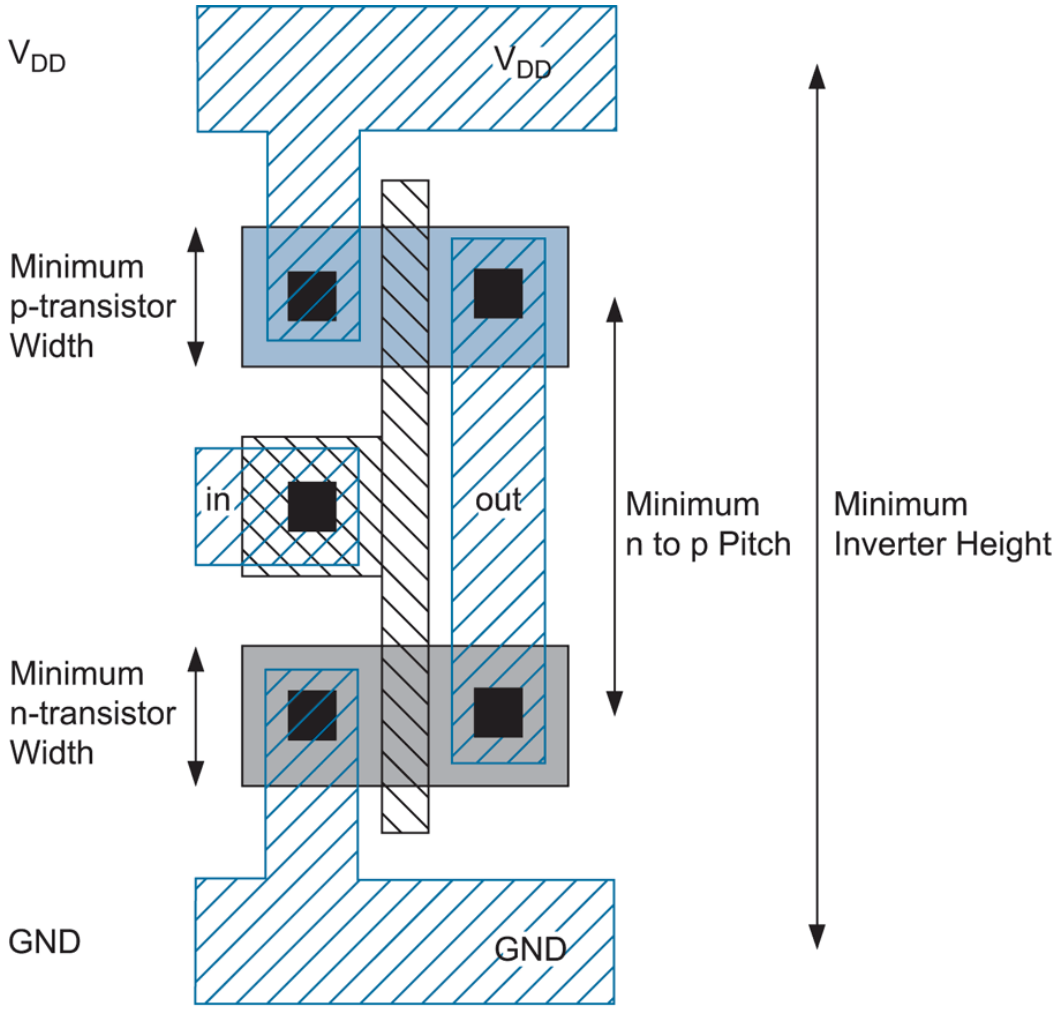
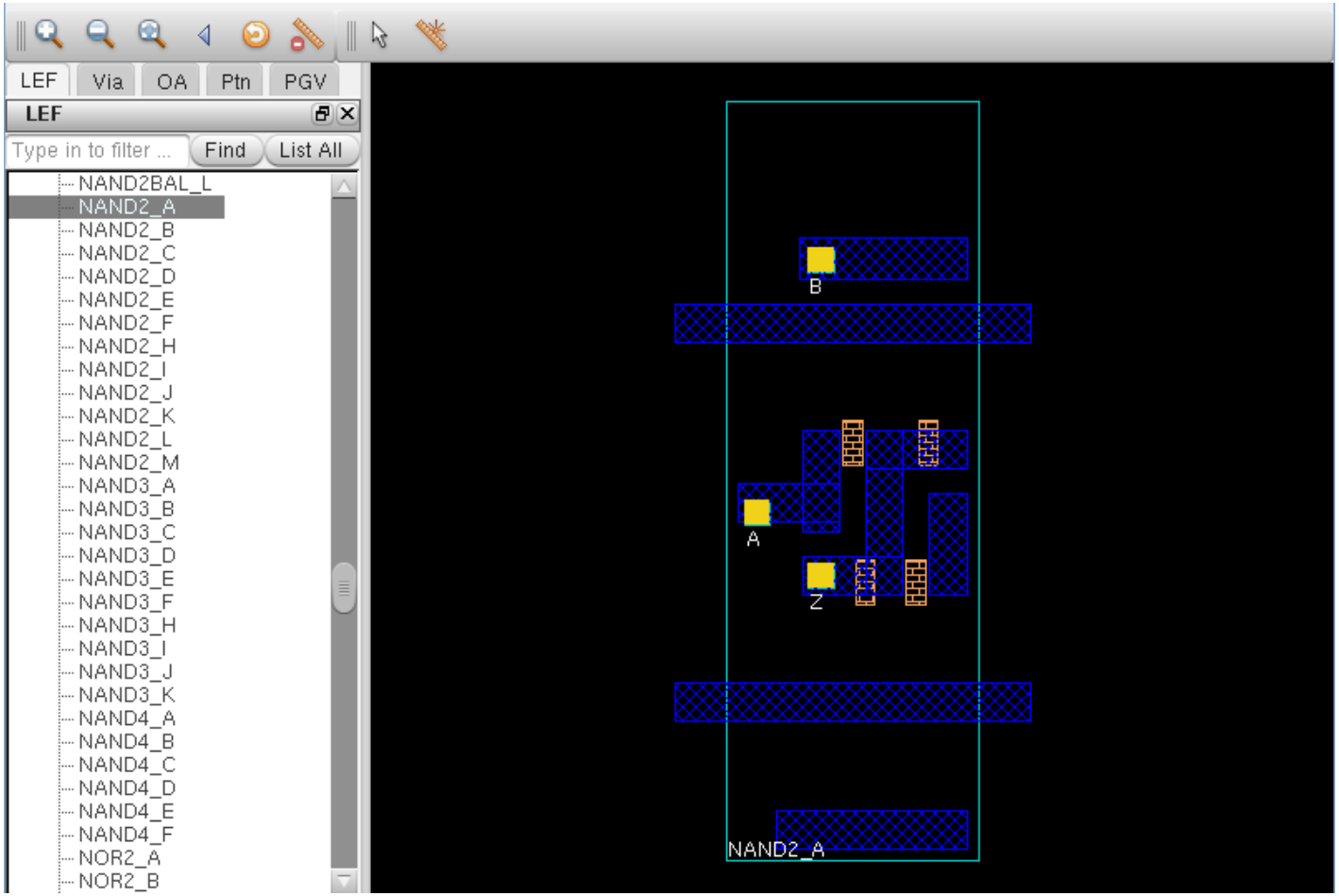


FIG 3.30 Minimum inverter height

Source: Weste "CMOS VLSI Design"

BiCMOS8HP NAND2_A Cell (LEF file)

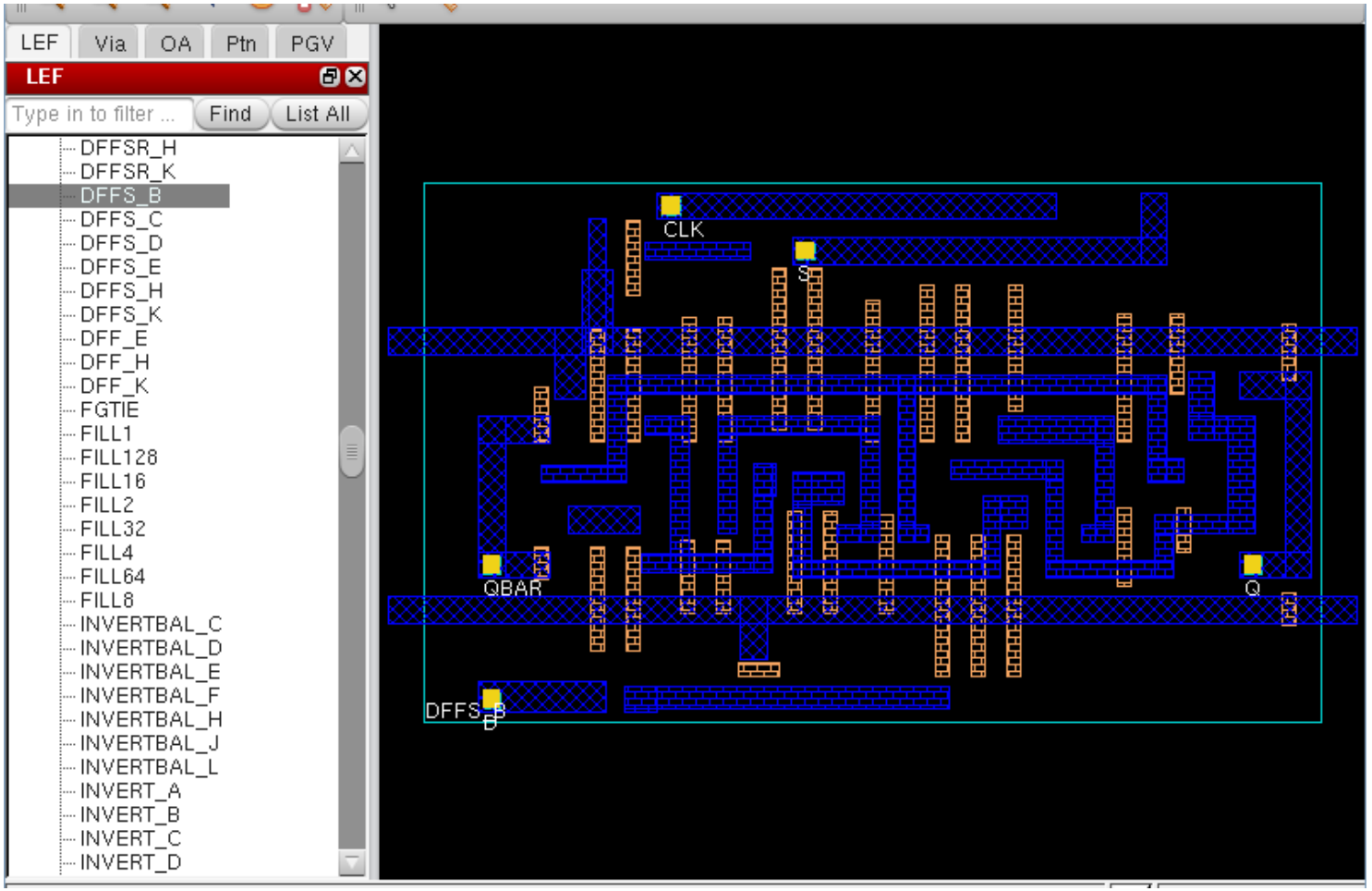
Yellow – "Pins" Orange = Poly Blue = Metal1



Cadence Encounter "Cell Viewer" Tool

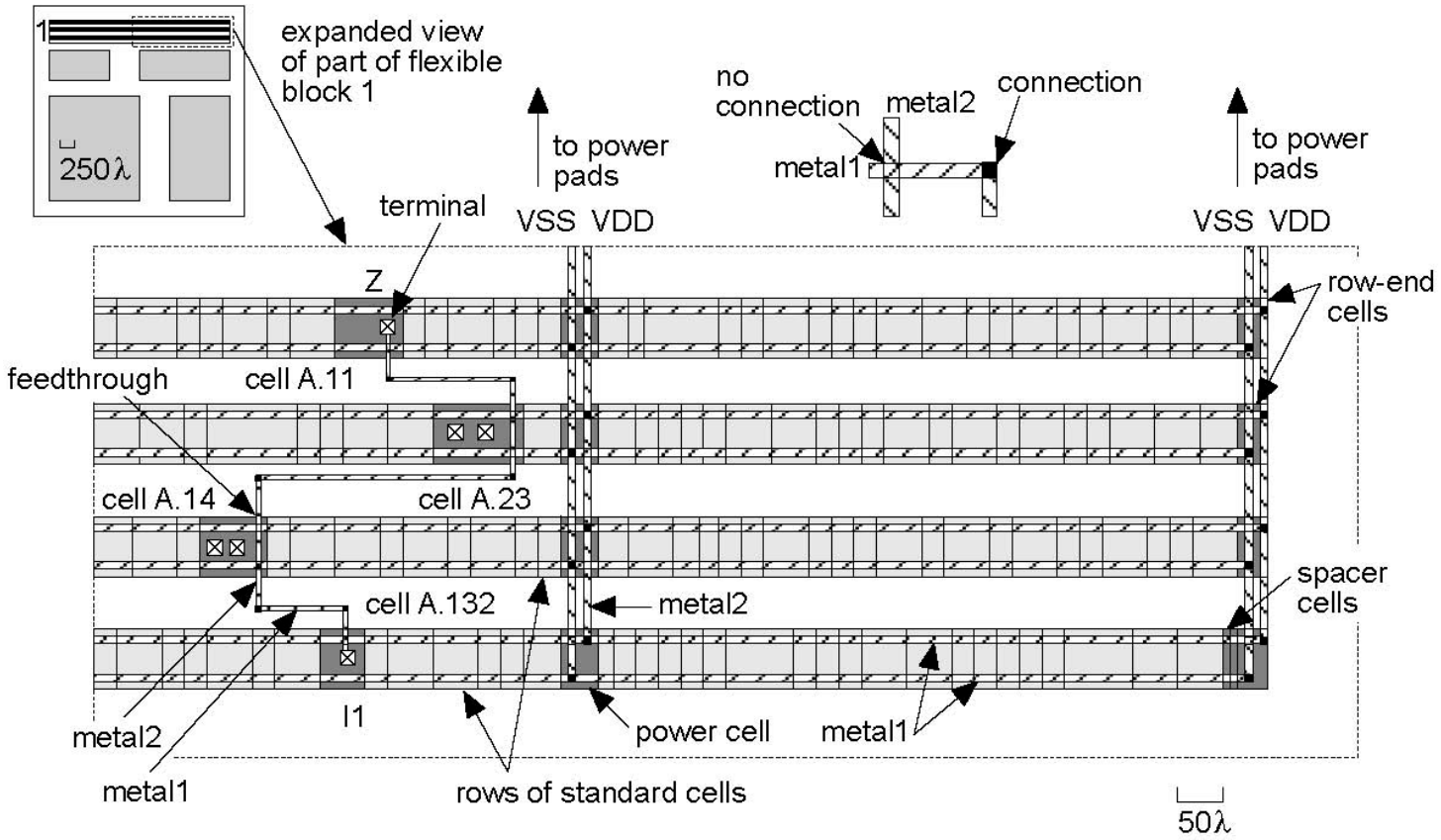
BiCMOS8HP DFFS_B Cell (LEF file)

Yellow – "Pins" Orange = Poly Blue = Metal1

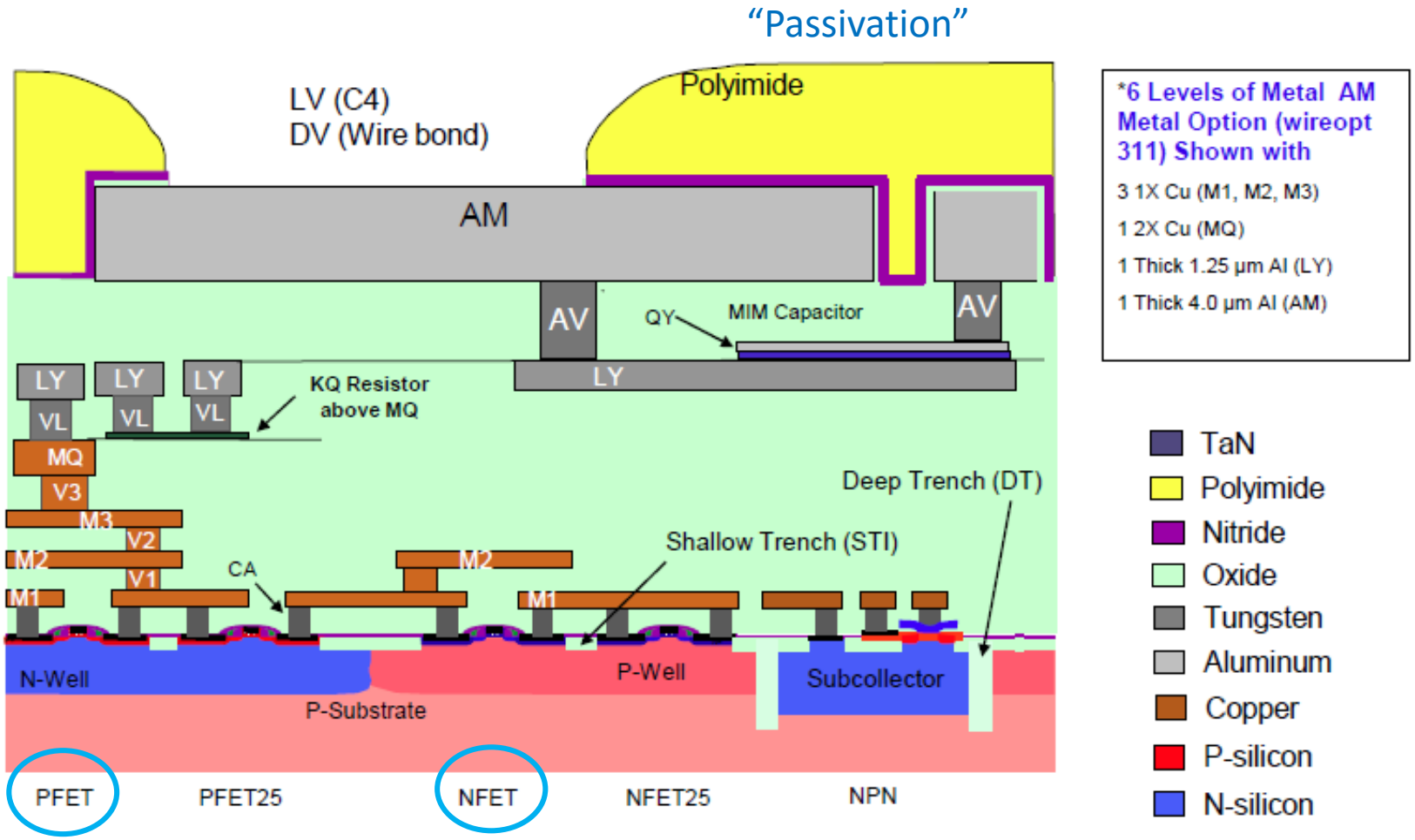


Cadence Encounter "Cell Viewer" Tool

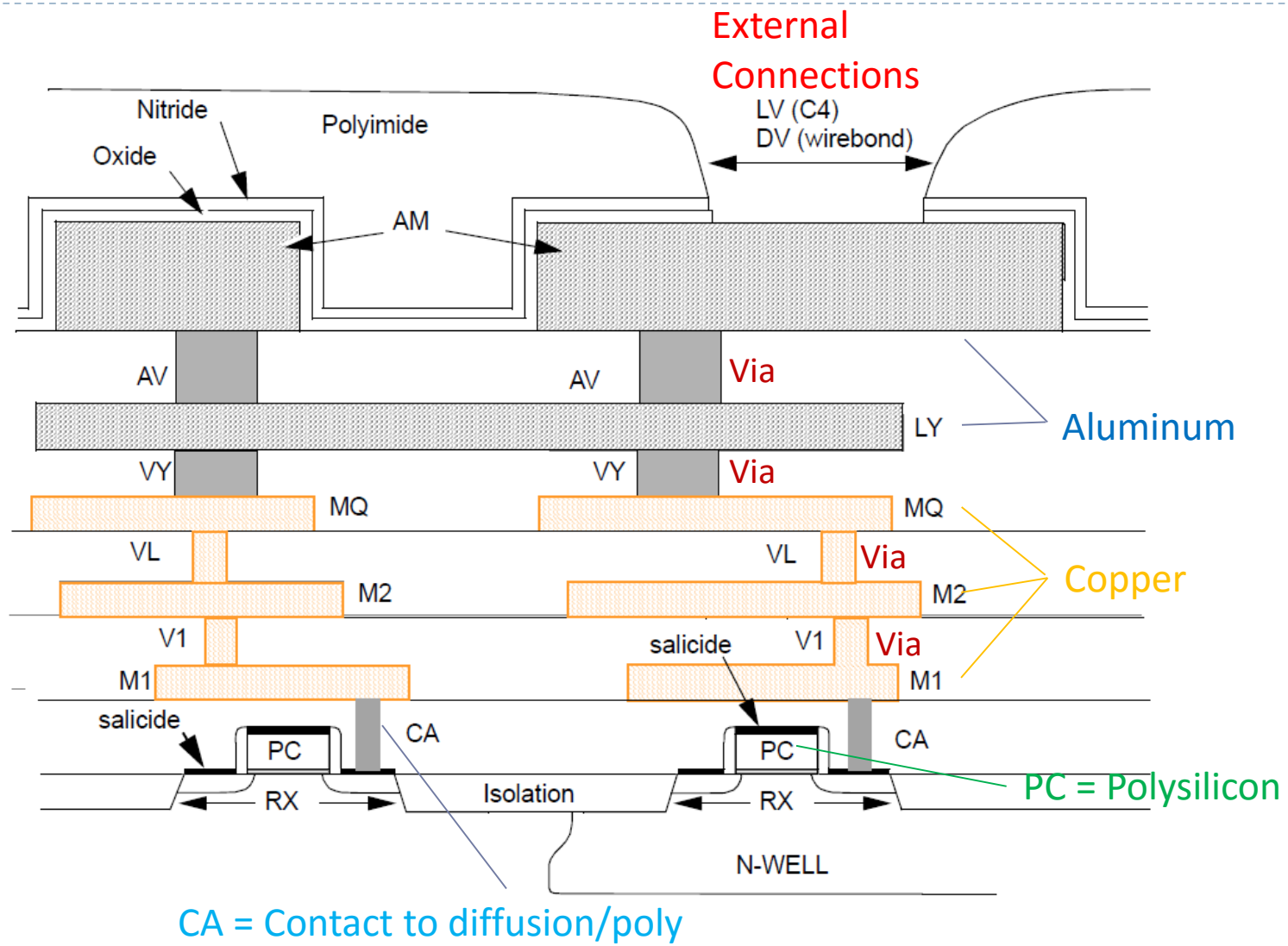
Standard Cell-Based Block



Global Foundries BiCMOS8HP process cross-section



BiCMOS8HP process cross-section



BiCMOS8HP metallization options: AM

- **Number of metal levels: 5, 6, or 7**
- **2 to 4 "1X thin" (0.32 µm) Cu layers (M1-M4)**
  - M1 and M2 (Cu) required
  - M3 and M4 (Cu) optional
- **1 "2X thick" (0.55 µm) Cu layer (MQ) - Required**
- **2 Last analog Al metal layers for high Q inductors (LY and AM) – Required**

Analog Metal (RF wiring)

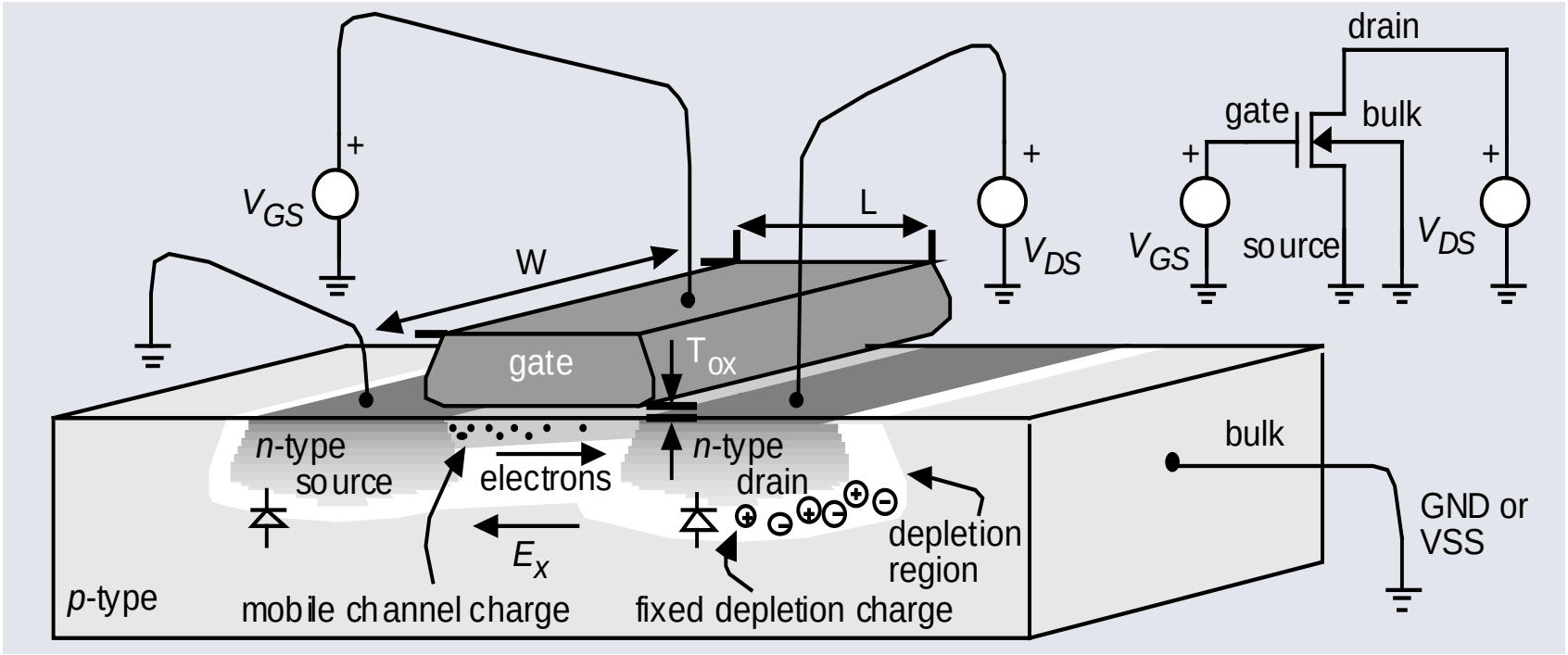
M1-M2-M3-M4-MQ-LY-AM

(M3-M4 Optional)

	BEOL Wiring Options						
# Levels of Metal	5	6	7				
Wiring Code	211	311	411				
Last Metal	AM	AM	AM				
LY	LY	LY	LY				
2X Level	MQ	MQ	MQ				
1X Level			M4				
		M3	M3				
	M2	M2	M2				
	M1	M1	M1				

Level	Metallurgy	Pitch (µm)	Thickness (µm)
M1	Cu	0.32	0.29
Mx	Cu	0.40	0.32
Vx	Cu	0.40	0.35
VL	Cu	0.80	0.65
MQ	Cu	0.80	0.55
VY	W	3.24	4.1
LY	Al	3.04	1.25
AV	W	3.24	4.1
AM	Al	2.8	4.0

Basic N-channel MOS transistor



CMOS Inverter Cross-Section

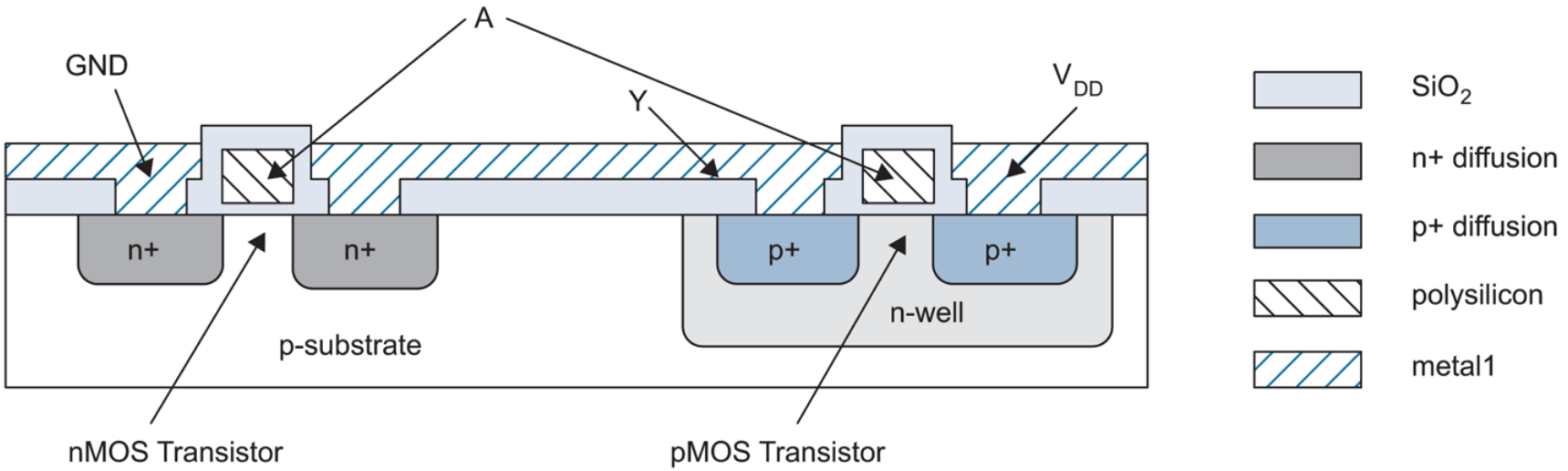


FIG 1.33 Inverter cross-section

Source: Weste "CMOS VLSI Design"

Inverter cross-section with well and substrate contacts

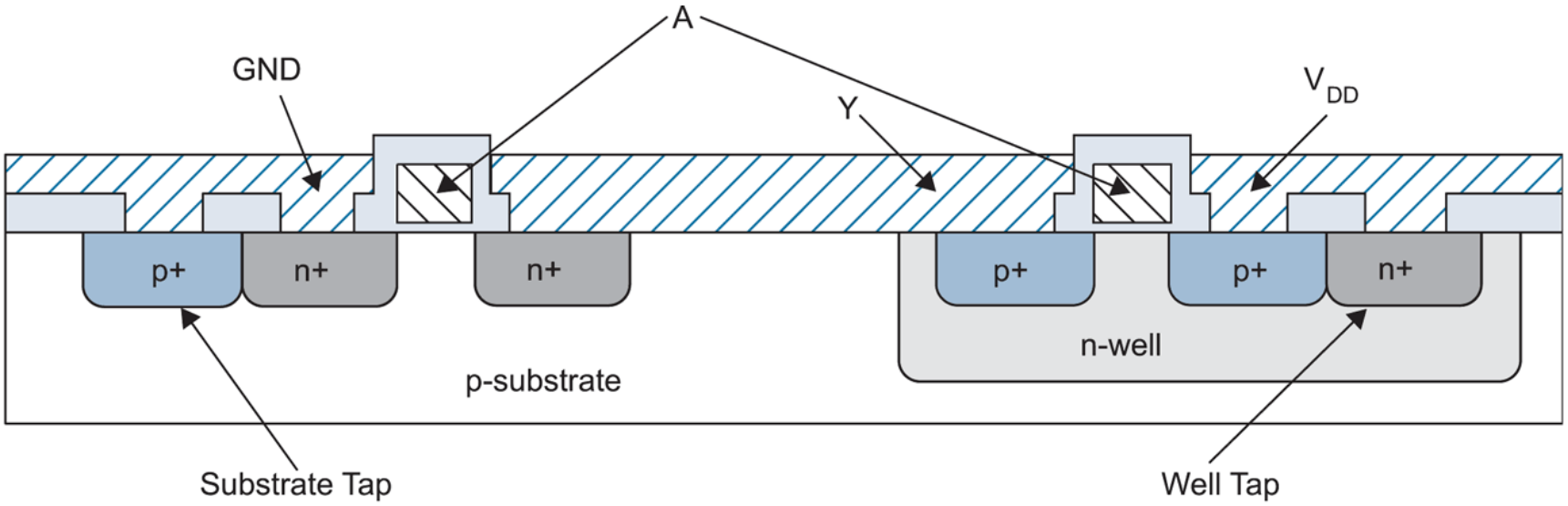
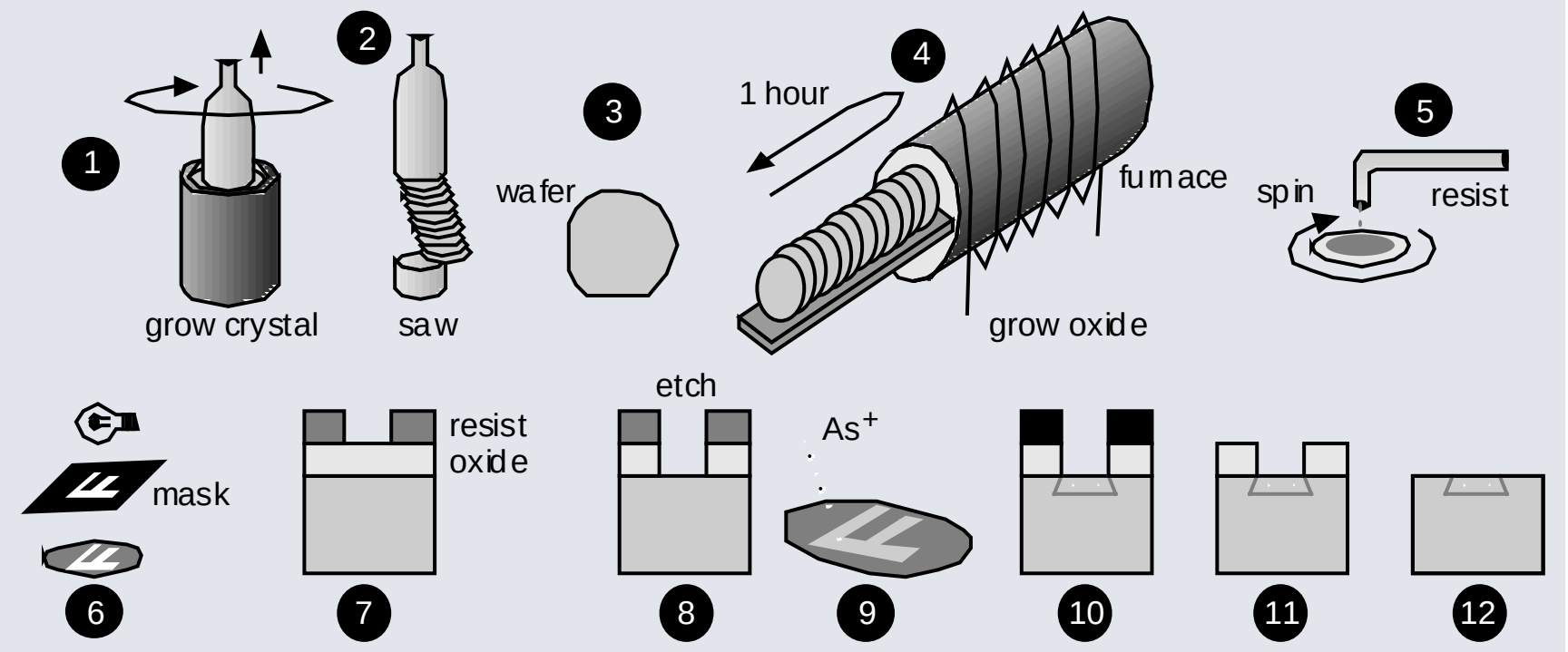


FIG 1.34 Inverter cross-section with well and substrate contacts. Color version on inside front cover.

Source: Weste "CMOS VLSI Design"

IC fabrication process



4. Grow oxide SiO2
5. Apply photoresist
6. UV light exposes resist
7. Remove exposed resist

8. Etch exposed oxide
9-10. Implant ions in exposed substrate
11. Strip resist
12. Etch oxide

CMOS Process steps

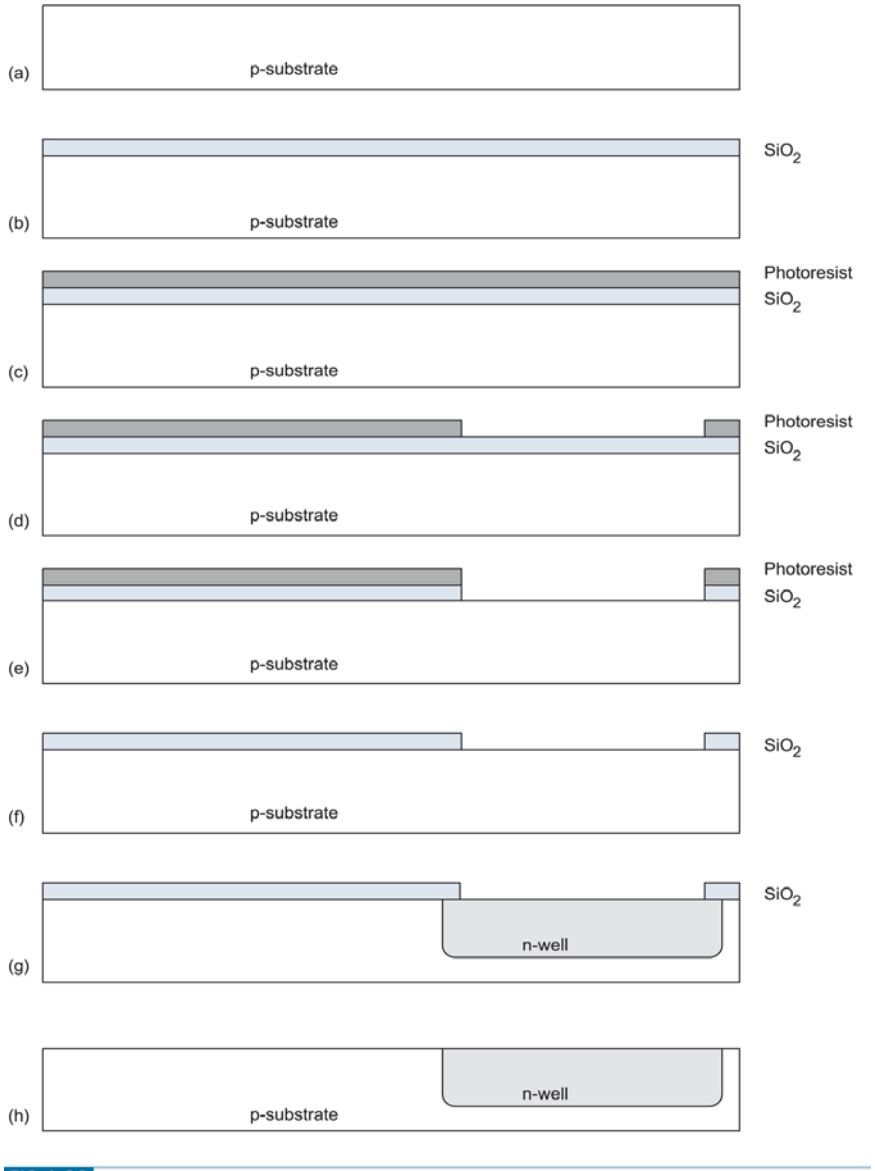


FIG 1.36 Cross-sections while manufacturing the n-well

P-substrate

SiO2 layer

Photoresist

Expose and etch

Etch SiO2

Remove photoresist

Implant n-well

Remove SiO2

Source: Weste “CMOS VLSI Design”

CMOS Process steps

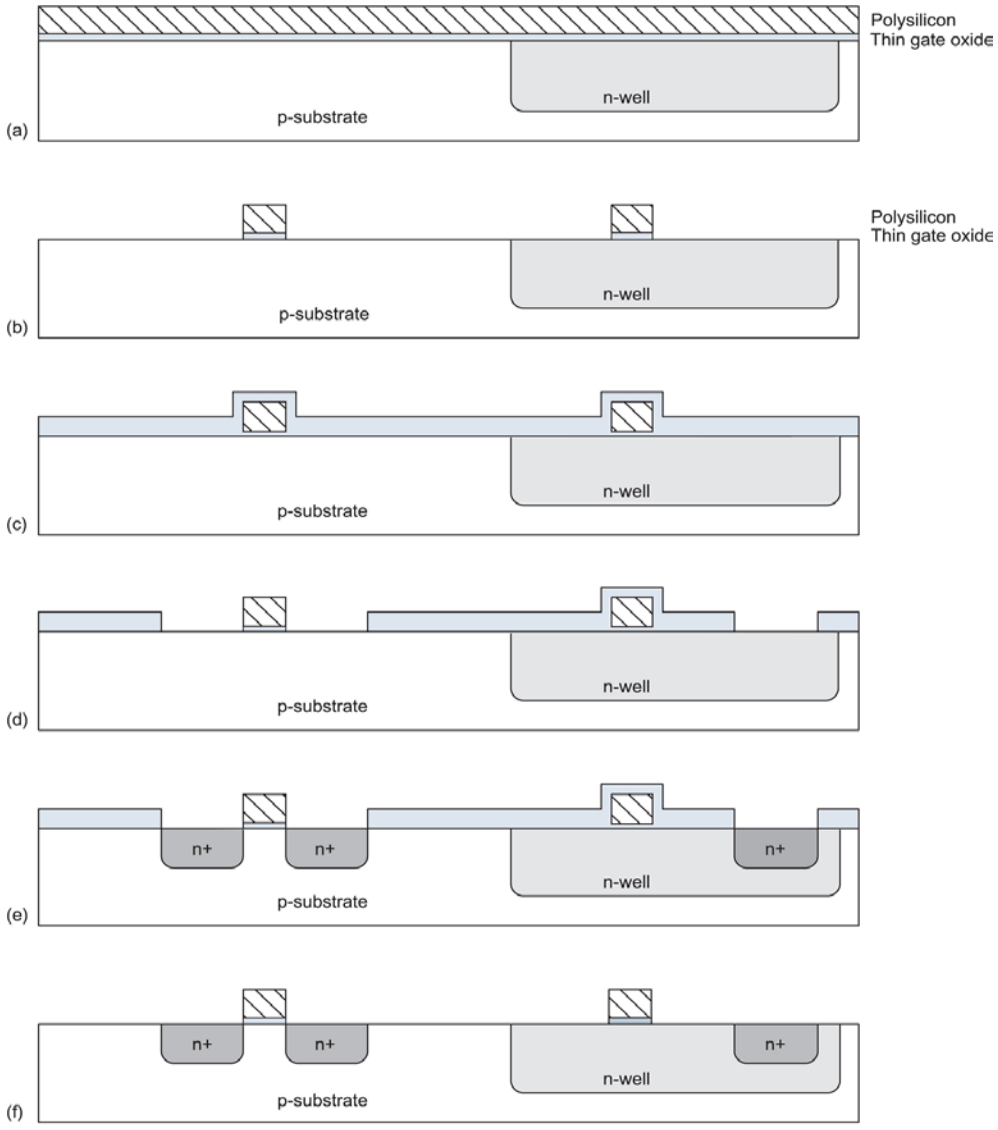


FIG 1.37 Cross-sections while manufacturing polysilicon and n-diffusion

Deposit poly

Etch

Deposit SiO2

Etch

Diffusion

Remove SiO2

Source: Weste “CMOS VLSI Design”

Inverter mask set

Generated by IC layout tools

"Layout" is a set of patterns for each layer.

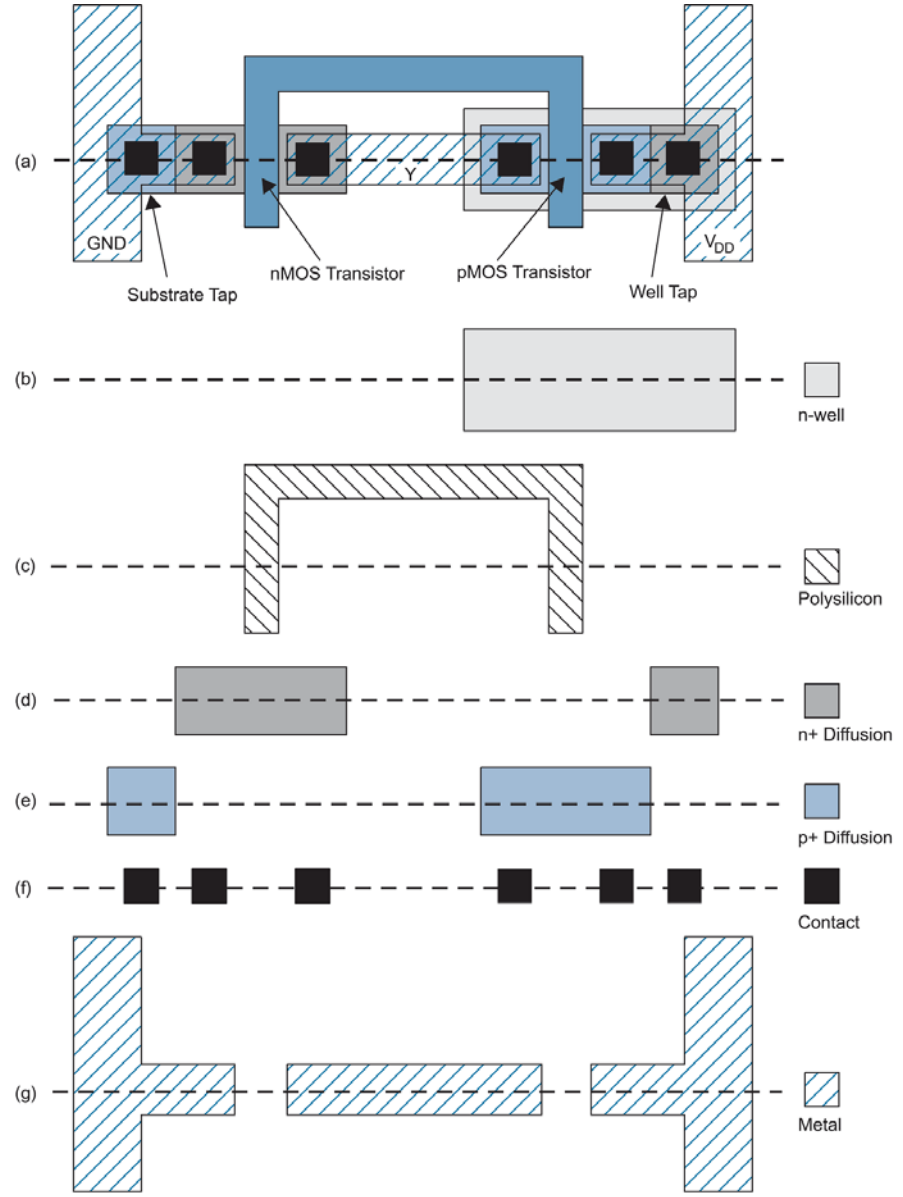


FIG 1.35 Inverter mask set. Color version on inside front cover.

Source: Weste "CMOS VLSI Design"

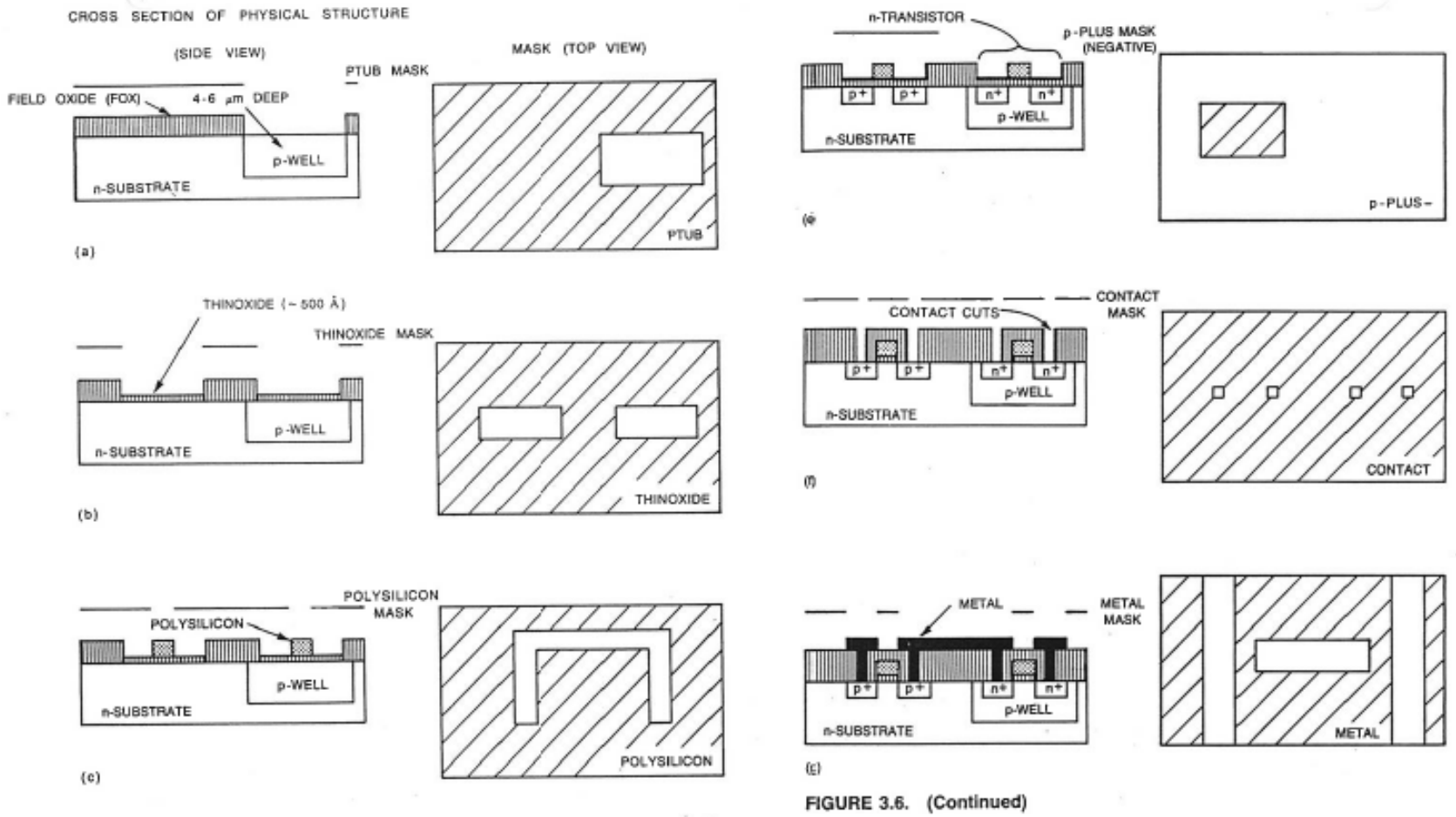
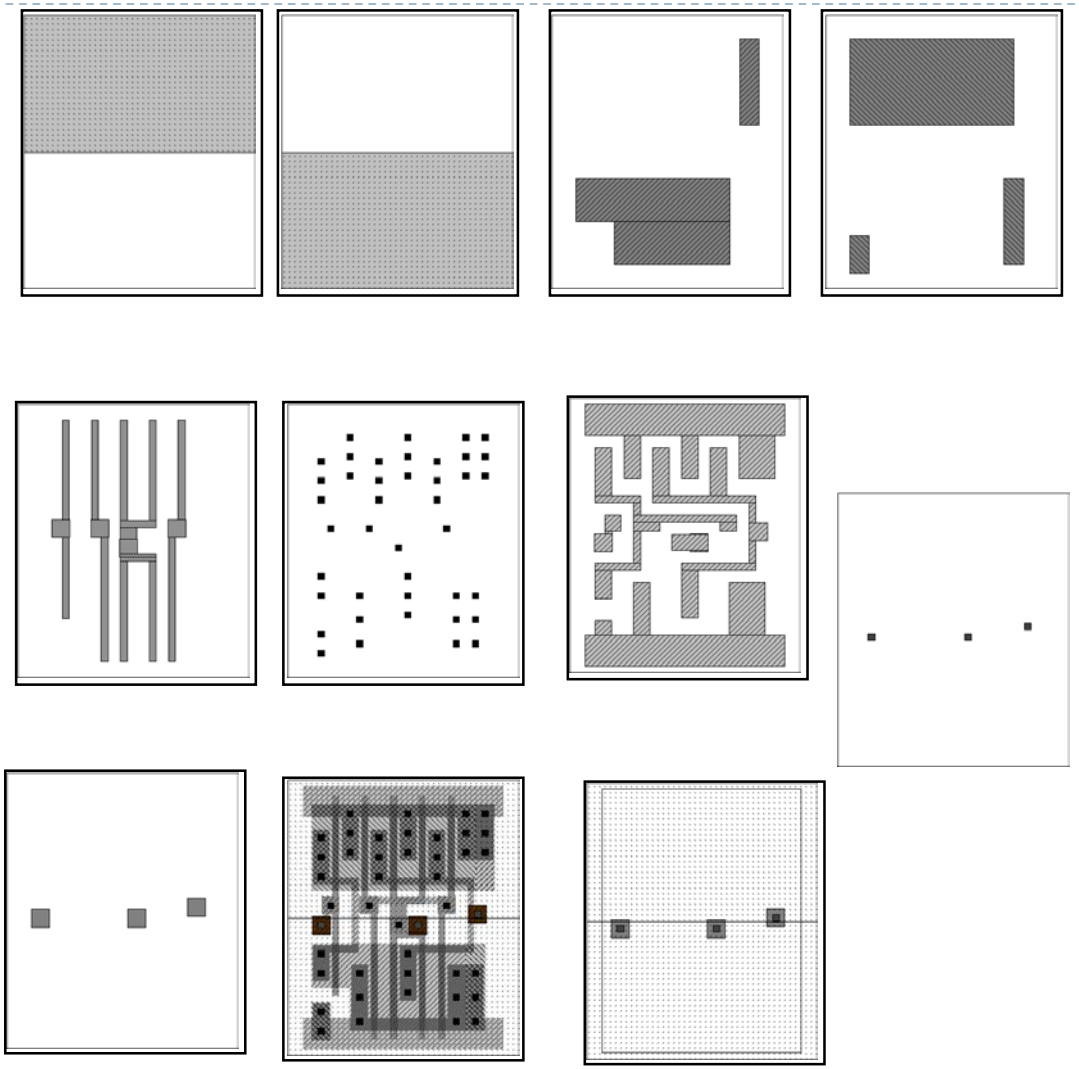


FIGURE 3.6. (Continued)

Inverter mask set

Standard Cell Mask Set (Submitted to foundry)



Source: Smith, Figure 2.7

MOSIS fabrication processes (www.mosis.org)

- **TSMC Fabrication Processes**

  28, 40, 65, 90, 130, 180 and 350 nanometer processes.

  Tiny2 program is also available on 65 and 180nm processes.

- **GlobalFoundries Fabrication Processes**

  14 nm, 28 nm, 40 nm, 55 nm, 0.13 µm,0.18 µm, 9HP (90 nm), 8HP (0.13 µm), 8XP (0.13 µm), 7WL (0.18 µm), 7RF SOI (0.18 µm) 7SW (0.18 µm) 9WG (90 nm), 9WG (90 nm), and TinyChip processes.

- **ON Semiconductor Fabrication Processes**

  0.7 µm high voltage CMOS, 0.5 µm CMOS, and 0.35 µm high voltage CMOS.

- **ams AG Fabrication Processes**

  180 and 350 nanometer processes - CMOS and high voltage CMOS and SiGe-BiCMOS.

- **AIM Fabrication Processes**

  AIM Photonics Fabrication

(Older) MOSIS fab processes (http://www.mosis.org)

AMI bought by ON Semiconductor: http://www.onsemi.com/
TSMC (Taiwan Semiconductor): http://www.tsmc.com

Table 3.1 MOSIS design rule options

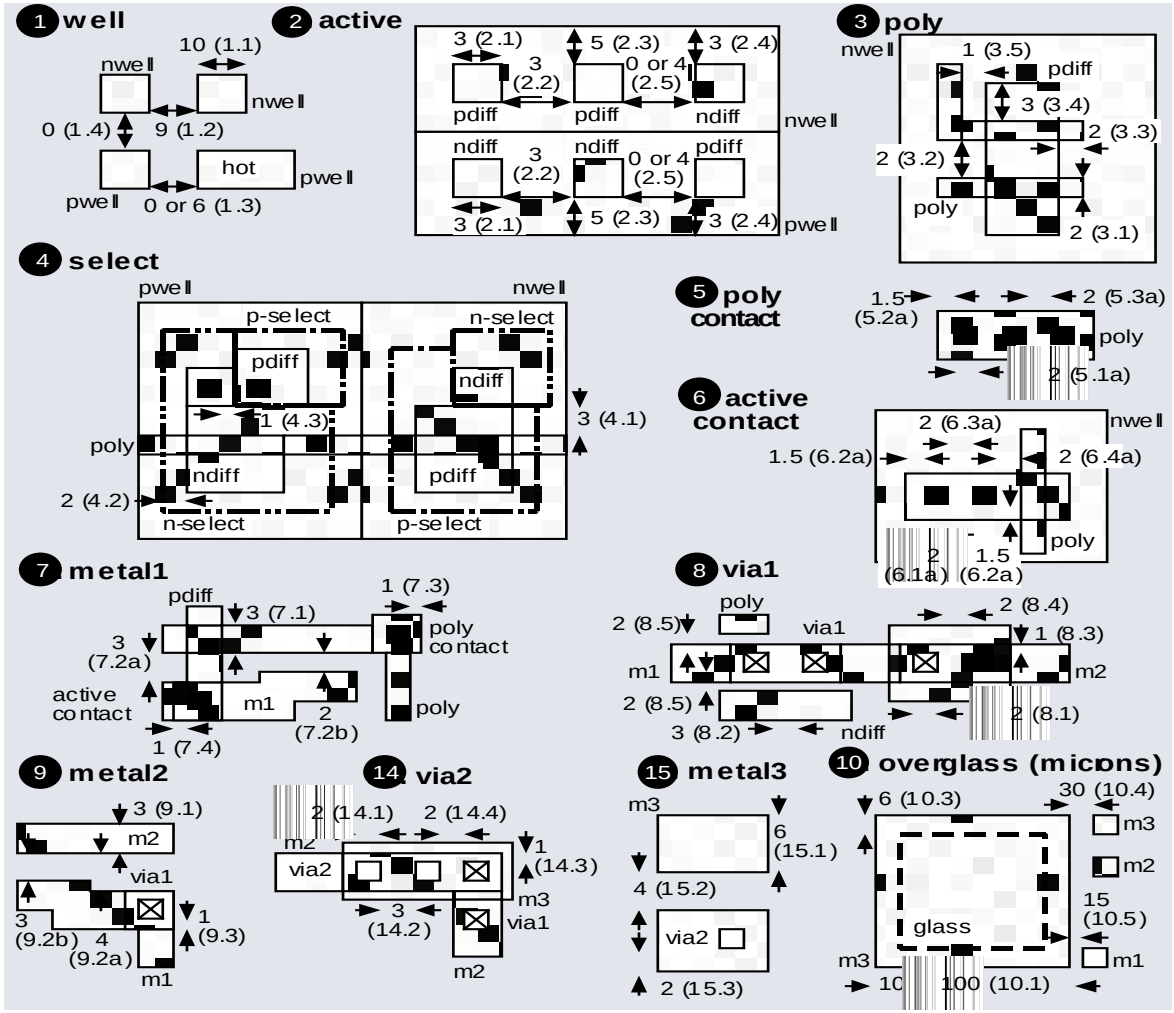
Vendor	Feature Size (μm)	Interconnect Layers	Stacked Vias	SCMOS	SUBM	DEEP
Orbit	2.0	2 metal	No	λ = 1.0 μm		
AMI=ON	1.5	2 metal, 2 poly	No	λ = 0.80 μm	λ = 0.80 μm	
AMI=ON	0.5	3 metal, 1–2 poly	Yes	λ = 0.35 μm	λ = 0.30 μm	
TSMC	0.35	4 metal, 1–2 poly	Yes		λ = 0.20 μm	
TSMC	0.25	5 metal	Yes		λ = 0.15 μm	λ = 0.12 μm
TSMC	0.18	6 metal	Yes		λ = 0.10 μm	λ = 0.09 μm

Mentor Graphics ASIC Design Kit

Scalable CMOS

Source: Weste "CMOS VLSI Design"

Scalable CMOS process design rules



Source: Smith, Figure 2.11

MOSIS Design Rules

Table 3.2 MOSIS design rules

Layer	Rule	Description	SCMOS	SUBM	DEEP
Well	1.1	Width	10	12	12
	1.2	Spacing to well at different potential	9	18	18
	1.3	Spacing to well at same potential	6	6	6
Active (diffusion)	2.1	Width	3	3	3
	2.2	Spacing to active	3	3	3
	2.3	Source/drain surround by well	5	6	6
	2.4	Substrate/well contact surround by well	3	3	3
	2.5	Spacing to active of opposite type	4	4	4
Poly	3.1	Width	2	2	2
	3.2	Spacing to poly over field oxide	2	3	3
	3.2a	Spacing to poly over active	2	3	4
	3.3	Gate extension beyond active	2	2	2.5
	3.4	Active extension beyond poly	3	3	4
	3.5	Spacing of poly to active	1	1	1
Select	4.1	Spacing from substrate/well contact to gate	3	3	3
	4.2	Overlap of active	2	2	2
	4.3	Overlap of substrate/well contact	1	1	1.5
	4.4	Spacing to select	2	2	4
Contact (to poly or active)	5.1, 6.1	Width (exact)	2x2	2x2	2x2
	5.2b, 6.2b	Overlap by poly or active	1	1	1
	5.3, 6.3	Spacing to contact	2	3	4
	5.4, 6.4	Spacing to gate	2	2	2
	5.5b	Spacing of poly contact to other poly	4	5	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/ active contacts	3	3	3
	6.8b	Spacing of active contact to poly contact	4	4	4
Metal1	7.1	Width	3	3	3
	7.2	Spacing to metal1	2	3	3
	7.3, 8.3	Overlap of contact or via	1	1	1
	7.4	Spacing to metal for lines wider than 10 λ	4	6	6

Smith text: Tables 2.7-2.9

MOSIS Design Rules

Table 3.2 MOSIS design rules (continued)

Layer	Rule	Description	SCMOS	SUBM	DEEP
Via1–Via(*N*-1)	8.1, 14.1, …	Width (exact)	2x2	2x2	3x3
	8.2, 14.2, …	Spacing to via on same layer	3	3	3
	8.4	Spacing to contacts (if no stacked vias)	2	2	n/a
	8.5	Spacing of via1 to poly or active edge	2	2	n/a
	14.4	Spacing of via2 to via1 (if no stacked vias)	2	2	n/a
Metal2–Metal(*N*-1)	9.1, …	Width	3	3	3
	9.2, …	Spacing to same layer metal	3	3	4
	9.3, …	Overlap of via	1	1	1
	9.4, …	Spacing to metal for lines wider than 10 λ	6	6	8
Metal3 (3-layer process)	15.1	Width	6	5	n/a
	15.2	Spacing to metal3	4	3	n/a
	15.3	Overlap of via2	2	2	n/a
	15.4	Spacing to metal for lines wider than 10 λ	8	6	n/a
Metal5 (5-layer process)	26.1	Width	n/a	4	4
	26.2	Spacing to metal5	n/a	4	4
	26.3	Overlap of via4	n/a	1	2
	26.4	Spacing to metal for lines wider than 10 λ	n/a	8	8
Metal6 (6-layer process)	30.1	Width	n/a	5	5
	30.2	Spacing to metal6	n/a	5	5
	30.3	Overlap of via5	n/a	1	2
	30.4	Spacing to metal for lines wider than 10 λ	n/a	10	10
Overglass Cut	10.1	Width of bond pad opening	60 µm		
	10.2	Width of probe pad opening	20 µm		
	10.3	Metal overlap of overglass cut	6 µm		
	10.4	Spacing of pad metal to unrelated metal	30 µm		
	10.5	Spacing of pad metal to active or poly	15 µm		

Smith text: Tables 2.7-2.9

MOSIS Design Rules

Table 3.3 Micron design rules for 90nm process

Layer	Rule	Description	90 nm rule (μm)
Well	1.1	Width	0.75
	1.2	Spacing to well at different potential	1.5
	1.3	Spacing to well at same potential	1.0
Active (diffusion)	2.1	Width	0.15
	2.2	Spacing to active	0.20
	2.3	Source/drain surround by well	0.25
	2.4	Substrate/well contact surround by well	0.25
	2.5	Spacing to active of opposite type	0.30
Poly	3.1	Width	0.09
	3.2	Spacing to poly over field oxide	0.15
	3.2a	Spacing to poly over active	0.15
	3.3	Gate extension beyond active	0.15
	3.4	Active extension beyond poly	0.15
	3.5	Spacing of poly to active	0.10
Select	4.1	Spacing from substrate/well contact to gate	0.25
	4.2	Overlap of active	0.20
	4.3	Overlap of substrate/well contact	0.10
	4.4	Spacing to select	0.30
Contact (to poly or active)	5.1, 6.1	Width (exact)	0.12
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.15
	5.4	Spacing to gate	0.10
Metal1	7.1	Width	0.13
	7.2	Spacing to well metal1	0.13
	7.3, 8.3	Overlap of contact or via	0.01
	7.4	Spacing to metal for lines wider than 0.5 μm	0.40
Via1–Via5	8.1, 14.1, …	Width (exact)	0.13
	8.2, 14.2, …	Spacing to via on same layer	0.13

(continued)

Smith text: Tables 2.7-2.9

MOSIS Design Rules

Table 3.3	Micron design rules for 90nm process (continued)		
Layer	**Rule**	**Description**	**90 nm rule (μm)**
Metal2–Metal6	9.1, …	Width	0.15
	9.2, …	Spacing to same layer metal	0.15
	9.3, …	Overlap of via	0.01
	9.4, …	Spacing to metal for lines wider than 1.0 μm	0.40
Via6		Width	0.20
		Spacing	0.20
Metal7		Width	0.40
		Spacing to metal7	0.40
		Overlap of via6	0.10
		Spacing to metal7 for lines wider than 1.0 μm	0.50

Smith text:
Tables 2.7-2.9

MOSIS Design Rules

Table 3.3	Micron design rules for 90nm process (continued)		
Layer	**Rule**	**Description**	**90 nm rule (μm)**
Metal2–Metal6	9.1, …	Width	0.15
	9.2, …	Spacing to same layer metal	0.15
	9.3, …	Overlap of via	0.01
	9.4, …	Spacing to metal for lines wider than 1.0 μm	0.40
Via6		Width	0.20
		Spacing	0.20
Metal7		Width	0.40
		Spacing to metal7	0.40
		Overlap of via6	0.10
		Spacing to metal7 for lines wider than 1.0 μm	0.50

Smith text:
Tables 2.7-2.9