ELEC 5250/6250 Project 9 – Design for Testability

Due: Monday, Nov. 12, 2018

Modify your modulo-6 counter circuit to incorporate **full-scan design**, and then redo the block layout and analysis as follows. The report is to be submitted electronically, addressing the following items.

1. Use *DFTadvisor* to convert your circuit from non-scan to full-scan design. Submit the new Verilog netlist model. Discuss how the full-scan version differs from the original.

2. Use *FastScan* to generate a complete test set for the modified counter circuit. Submit and discuss the statistics from the ATPG and fault simulation, showing the number of test vectors and the number of faults detected vs. total number of assumed faults.

3. Study the generated test procedure and one of the generated test patterns. Describe how the tester will use that information to apply that pattern and check the results.

4. Generate a new block layout for the modified counter circuit, and provide evidence that the design passes both connectivity and geometric checks. Then measure and compare the areas of the non-scan and full-scan block layouts, and report the change in area, i.e. the "area overhead" due to the use of full-scan design.

5. Examine the propagation delay of the worst-case clock loop in the newly generated layout, and compare that to the delay from the non-scan layout, i.e. the "performance overhead".