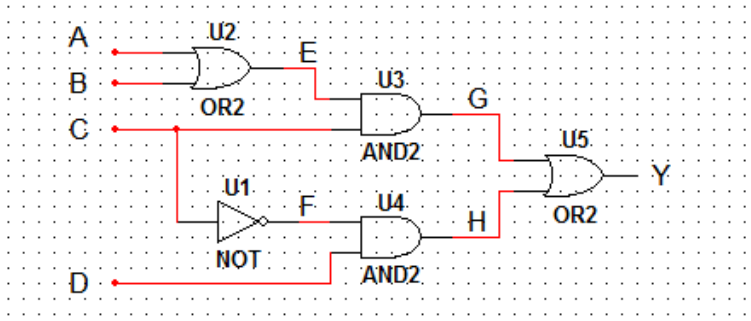
ELEC 5250/6250 Project 9 – ATPG and Fault Simulation

Due: Monday, Nov. 5, 2018

Design a test to get as close as possible to 100% fault coverage for the following circuit.



1. Considering all stuck-at faults in this circuit, collapse the fault set by finding equivalent and dominating faults, and list a minimal set of faults that should be tested. Detection of the faults in this collapsed set should ensure detection of any faults in the circuit.

2. Use the D algorithm, or any other method, to derive a set of test vectors that will detect the faults in your collapsed fault set. If a fault is determined to be untestable, indicate how you determined that.

3. Use the fault simulation capability of *FastScan* to verify that your set of test vectors detects all of the faults in the circuit.

4. Use the ATPG capability of *FastScan* to generate a test for the above circuit, and compare the generated test set to the one you created manually. Specifically, point out how many test vectors *FastScan* generated and the fault coverage of that test set.

NOTE: *FastScan* requires a Verilog netlist of the circuit. You should create this netlist by instantiating gates from the BICMOS8HP library.