ELEC 5250_6250 Project 7
Due: Monday, October 29

ELEC 5250 Students: Do this assignment with the modulo-6 counter circuit.
Then do the divider circuit for practice ***(do not submit)***
ELEC 6250 Students: First practice with the modulo-6 counter ***(do not submit)***.
Then do the assignment with the divider circuit.

Submit your project report <u>electronically</u> as a Word or PDF document.

1. If necessary to make corrections, use Synopsys *Design Compiler (DC)* to resynthesize your circuit(s). You will need the Verilog netlist and constraints files produced by DC to proceed with physical design.
2. Use the *Innovus* graphical user interface menus to produce a layout for the modulo-6 counter. Note any changes that you observe from step to step in the layout process, write a summary of those changes, and capture the final layout as an image for your report.
3. As the final step in the layout process, verify the layout connectivity and geometry to ensure no structural errors. Copy into your report the key statements from the connectivity and geometric verification reports that show no errors.
4. Building on your experience in Steps 2 and 3, and the course slides, create script files to perform the modulo-6 counter layout and compare the results to those produced from the GUI. For your report, insert your script files, an image of the final layout, and the connectivity/geometry verification results.
5. ELEC 6250: Modify your scripts and repeat Step 4 for your divider circuit. Then continue with the following steps for the divider circuit.
6. In your scripts for Step 4 (ELEC 5250) or Step 5 (ELEC 6250), include three timing checks and optimization steps: (1) before clock tree synthesis, (2) after clock tree synthesis, (3) after final routing. Then find and examine the timing reports and provide the following information
    a. A description of the “clock tree”.
    b. The worst-case “clock loop” (flip-flop to flip-flop) path and delay.
7. Identify and describe difference(s) between the worst-case delay reported by Synopsys DC and the post-route timing information in Step 6(b) above.
8. Identify and describe any differences in the Verilog netlist produced by DC, and the final Verilog netlist saved by *Innovus*.
9. Determine the area of the “core” and the I/O bounding box in the final layout, and compare them to the area predicted by Synopsys DC.
10. Examine the final SDF file produced by *Innovus* and describe any significant differences from the SDF file produced by Synopsys DC.
11. Repeat the timing simulation that you did of the netlist produced by DC, but this time using the Verilog netlist and SDF file produced by *Innovus*, and note any differences in functionality and/or path delays.