ELEC 5250/6250 Project #5 – Synthesis

Due Friday, October 5, 2018

A. ALL ELEC 5250 and 6250/6256 Students:

For the Modulo-6 counter designed previously:

1. Use Synopsys Design Compiler (DC) to synthesize a gate-level netlist of standard cells (CMOS8HP Library), producing Verilog netlist files.

2. Using your previously-designed testbench, repeat the behavioral simulation performed previously, but using the synthesized netlist, and verify that the synthesized circuit produces the same results as the behavioral model. If the results do not agree, comment on the differences. Submit your simulation results for the synthesized Verilog netlist.
   - ***Refer to Slide 6 of the "Post-Synthesis Simulation" slides for location and use of the Verilog models of the gates in the 8HP standard cell library.***
   - We will perform "timing simulation" with the VITAL models and SDF file information in a future project.

3. Produce an area report from the DC results. Indicate the total "area" reported by DC for the synthesized circuit and compare the synthesized circuit with your hand-designed schematic from the initial semester project, comparing the types of gates used, the number of gate instances, and the number of "equivalent gates". Comment on any "unexpected" or unusual results in the synthesized circuit from what you expected.

4. Produce a delay report from the DC results. Determine the longest path delay in the circuit. Use this information to adjust at least two "constraints", rerun the synthesis, compare the results to see if any improvement was made, and note any change in the total area of the synthesized circuit. Given the clock period constraint, what was the worst timing "slack", and through which modules does this path go?

B. ELEC 6250/6256 Students (ELEC 5250 students can submit for extra credit)

Repeat steps 1-4 of part A for the recently-designed divider circuit. However, during synthesis, maintain the design hierarchy and then determine the total number of modules produced and the total number of flip-flops in each module of the circuit. Comment on whether these counts are what you expected. In step 4, we would expect to see some improvement of the worst case path in the circuit.

For parts A and B, ***send via EMAIL*** a report containing the synthesized netlists from step 1, annotated simulation listings from step 2, and a short report summarizing your comparison of the simulation results and the information in steps 3 and 4.
(Do not print hard copies of all this information.)